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Characterization of 4H-SiC Lateral MOSFETs Up to 773 K

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Abstract. Experimental analysis of 4H-SiC lateral MOSFETs characteristics up to 773K is shown. The reduction of threshold voltage, V_{TH}, and the increase of the field effect channel mobility, μ_{CH}, with temperature cause an increase of MOSFET current up to 623K. However, when scattering with lattice vibration starts to be predominant, μ_{CH} decreases with an abrupt drop at 773K, reducing MOSFET current. Channel resistance, R_{CH}, decreases with the temperature up to the range between 523 K and 573 K, implying possible thermal instability effects. However, when the temperature increases over this range, the thermal scattering predominates and R_{CH} again increases, ensuring thermal stability of MOSFETs.

Introduction

Electron devices capable of operating at high temperature condition are required for harsh environment applications. To this aim, wide band-gap semiconductors are the most suitable [1]. 4H-SiC CMOS technology is emerging among others, such as JFET [2, 3] and BJT ones [4], thanks to the ease of manufacturing and the possibility of easily achieving complementarity, necessary requirement for integrated circuits, ICs, design. However, there is still a lack of knowledge about electrical behaviour of single lateral NMOSFETs and PMOSFETs under high temperature operation, which is a starting point to understand and to improve technology performances and applications. Experimental characteristics of 4H-SiC lateral MOSFETs have been shown up to 773K [5, 6], however they are limited to devices with wide channel width, i.e. W=100μm and W=150μm, which are unusual for ICs design. Also, sensors based on diode connected MOSFETs have been shown up to 873K [7], but the analysis is not supported by key physical parameters, like threshold voltage, V_{TH}, and channel mobility, μ_{CH}. Moreover, in [8] experimental characteristics of 4H-SiC lateral MOSFETs have been analyzed in a limited temperature range, i.e. up to 573K, and the effects of interface state defects are evaluated through numerical simulation tools. However, in [5-8] no considerations regarding thermal stability of devices through the extracted channel resistance have been provided. In this paper, we experimentally investigate the I-V characteristics of 4H-SiC lateral MOSFETs up to 773K, through the extraction of physical parameters like V_{TH} and μ_{CH}. Moreover, thermal stability analysis has been done through the extracted channel resistance.

Device Structure and Experimental Set-Up

Lateral MOSFETs have been fabricated in 4H-SiC CMOS Fraunhofer IISB's Technology [9]. A 10^{15} cm^{-3} Nitrogen doped epitaxial layer is grown on a SiC n-type 350 μm 4° off-axis (0001) substrate. Aluminum and Nitrogen ion implantation, followed by a 1973 K, 30 min, thermal annealing in Argon environment is performed for p-type and n-type doped regions. Resulting in a p-well with a doping

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concentration of 10^{17} cm^{-3} and in a n-well with 10^{16} cm^{-3}, whereas source and drain regions have a $5 \cdot 10^{19}$ cm^{-3} doping concentration. The gate oxide is thermally grown at 1300°C and a post-oxidation annealing in NO environment is performed at 1300°C to reduce the interface state density. It results in a 55 nm SiO_2 thick gate oxide with an oxide capacitance, C_{OX}, of 62.8 nF/cm^2. A 500 nm n-type PolySilicon is deposited for the gate electrode, and a further 400nm-thick oxide is deposited to gate electrode isolation. NiAl and Ti/Al are used for n-type and p-type contact materials. $SiO_2/Si_3N_4/SiO_2$ stack is deposited by plasma enhanced chemical vapor deposition (PECVD) to isolate metals layers. These are made by Ti/Pt to allow high temperature operation [10]. Fabricated NMOSFET and PMOSFET have both channel width, W=24µm, and channel length, L=6 µm.
Measurements have been performed in ambient atmosphere by heating the devices with a 630W G.Maier Elektrotechnick GmbH hotplate and measuring with a Keithley SCS-4200, a SUSS PM5 probe station and with Signatone Corporation manipulators equipped with Tungsten high temperature probe tips.

Results and Discussion

High Temperature Characteristics.

I-V-T characteristics have been performed in T ∈ [298;773] with a ΔT=50K. The output characteristics, at $|V_{GS}|$=20V, of lateral NMOSFET and PMOSFET are shown in Fig.1.a)-b), respectively, whereas trans-characteristics, at $|V_{DS}|$=0.1V, are in Fig. 1.c)-d), both devices have W=24µm and L=6µm.

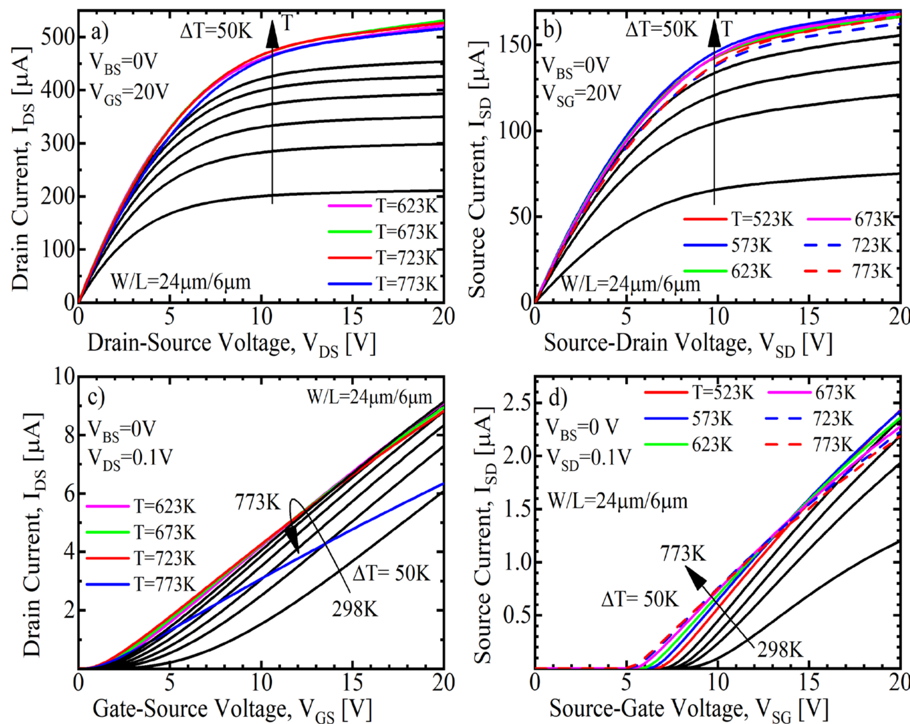

Fig. 1. Output characteristics, $|V_{GS}|$=20V, of a) NMOSFET and b) PMOSFET, and trans-characteristics, $|V_{DS}|$=0.1V of c) NMOSFET and d) PMOSFET. Both with L=6µm and W=24µm, V_{BS}=0V, and T ∈ [298;773] with ΔT=50K.

NMOSFET current increases with temperature by 100% up to 573K and for $V_{GS}=V_{DS}$=20V. Then, it increases by only 3.6% in T ∈ [623;723] K (see Fig.1.a)) and at T=773K it decreases, as can be also observed in I_{DS}-V_{GS} characteristics of Fig. 1.c). Similarly, as shown in Fig.1.b), PMOSFET current increases up to T=573K by 125% at $V_{SG}=V_{SD}$=20V, then it reduces at T=773K by -2.67%.

To explain MOSFET electrical behavior, key physical parameters, like threshold voltage and channel mobility have been extracted and their temperature behavior linked to MOSFET ones.

Threshold Voltage.

V_{TH} has been extracted, for both NMOSFET and PMOSFET, from the trans-characteristics of Fig.1.c)-d) with the extrapolation in linear region method [11]. Both MOSFETs show a non-linear reduction with temperature increase, as shown in Fig. 2. The non-linearity can be explained through V_{TH} equation [12]:

$$V_{TH} = \varphi_{ms} + 2\psi_B + \frac{\sqrt{4\varepsilon_{SiC} q N_A \psi_B}}{C_{ox}} + \frac{qQ_f}{C_{ox}} + \frac{qD_{it}(T)}{C_{ox}} \quad (1)$$

where φ_{ms} is the work function difference between the n-type Polysilicon and SiC, ψ_B the difference between the Fermi potential with respect to the midgap, ε_{SiC} the 4H-SiC dielectric permittivity, q the elementary charge, N_A p-well doping concentration, Q_f the fixed charge, and $D_{it}(T)$ the temperature dependent interface defects. The high density of SiO_2/4H-SiC interface defects and their temperature dependence introduce non-linearity [13-15], being directly linked to V_{TH} through Eq.1.

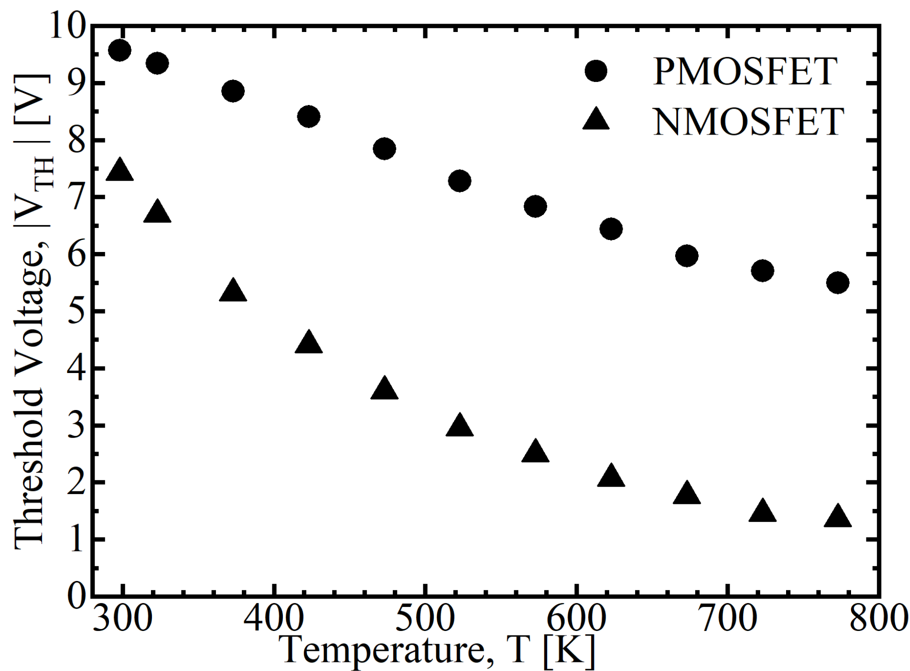

Fig. 2. V_{TH} – T dependence for NMOSFET and PMOSFET in T ∈ [298;773] with ΔT=50K.

Channel Mobility

μ_{CH} has been extracted from trans-characteristics of Fig.1.c)-d) according to:

$$\mu_{CH} = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}=0.1V} \frac{L}{V_{DS} C_{ox} W} \quad (2)$$

Both NMOSFET and PMOSFET show an increase of field effect channel mobility peak up to T=523K, then it starts to decrease (see Fig.3). Indeed, it increases up to $\mu_{CH,\,N\,peak}$=21.75cm^2/Vs and $\mu_{CH,\,P\,peak}$=8.25cm^2/Vs for NMOSFET and PMOSFET, respectively, whereas a minimum value is observed at T=773K, with $\mu_{CH,\,N\,peak}$=14.28cm^2/Vs and $\mu_{CH,\,P\,peak}$=6.78cm^2/Vs. This behaviour can be explained in this way: the reduction of interface trapped charge with temperature causes a reduction of Coulomb scattering, allowing the channel mobility increase [16], but when the thermal scattering starts to be dominant the channel mobility decreases [12].

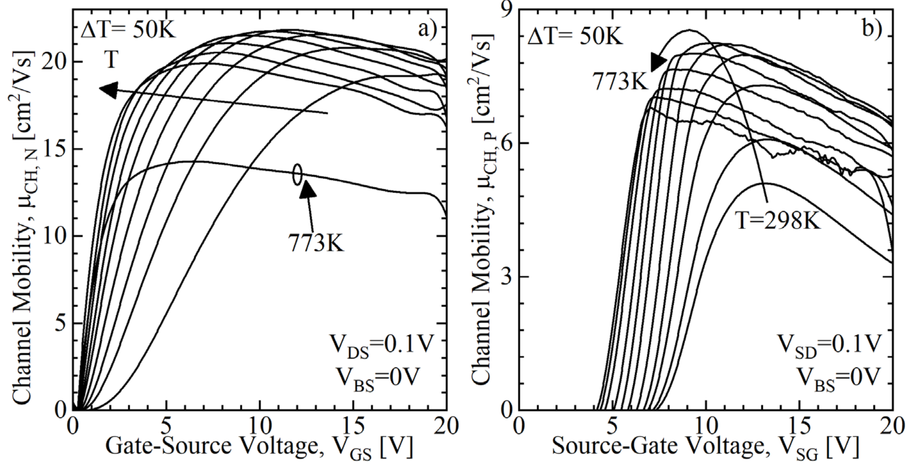

Fig. 3. Extracted channel mobility for a) NMOSFET and b) PMOSFET, at $|V_{DS}|$=0.1V in T ϵ [298;773] K.

The combined effect of V_{TH}-reduction and μ_{CH}-increase with temperature causes a MOSFETs current increase up to T=623K. However, when the reduction of channel mobility, due to thermal scattering starts to dominate, $|I_{DS}|$ reduces, as can be seen at T=773K of Fig.1.c)-d).

Channel Resistance.

The current thermal behaviour explains channel resistance, R_{CH}, temperature behaviour, which is shown in Fig.4. R_{CH} has been extracted for both NMOSFET and PMOSFET from the output characteristics of Fig.1.a)-b) at $|V_{DS}|$=0.1V, by subtracting parasitic series resistance contribution, due to the implanted regions and contact resistance [17]. n-Channel resistance reaches a minimum at T=573K of 11.5kΩ, whereas p-Channel resistance minimum of 36kΩ is at T=523K. such reduction implies an increase of the current with temperature, in those applications where a bias voltage is applied, and therefore a possible self-heating effect can induce a thermal instability of the devices. However, the further increase of resistance at higher temperatures, as shown in Fig.4, reduces the thermal-run-away of the current, allowing a thermally stable device.

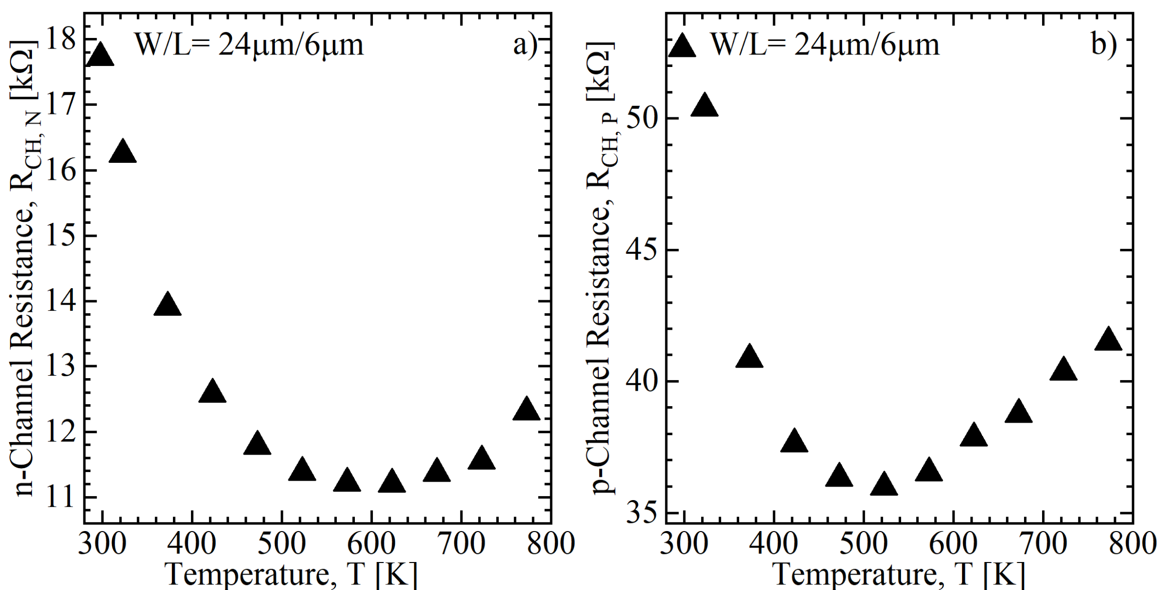

Fig. 4. R_{CH}-T of a) NMOSFET and b) PMOSFET in Tϵ [298;773] K, at $|V_{GS}|$=20V and $|V_{DS}|$=0.1V.

Summary

Experimental analysis of 4H-SiC lateral MOSFET is shown between 298K and 773K. The MOSFET current temperature behavior can be related to the V_{TH} and μ_{CH} temperature dependence. The current increases up to T=623K and it stays almost constant in T ∈ [623; 723] K. However, $|I_{DS}|$ starts to abruptly decrease when scattering carriers with lattice vibration becomes predominant on channel mobility, which abruptly decreases. Analysis of $R_{CH} - T$ behavior shows that possible self-heating problems could be due to decrease of R_{CH} with temperature. However, the R_{CH} increase at higher temperature guarantees the thermal stability of MOSFETs.

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