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Short-Circuit Reliability Analysis of SG-MOSFETs Versus Planar 4H-SiC MOSFETs

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Abstract. This work investigates the short-circuit (SC) reliability of Split-Gate (SG) versus planar 4H-SiC MOSFETs through TCAD simulations. While SG-MOSFETs effectively reduce gate-drain capacitance and improve switching performance, SG-MOSFETs exhibit enhanced short-circuit failure effects. Structural optimization—such as thicker drift regions, extended gate lengths, and narrowed JFET widths—can improve SC withstand time (SCWT). However, SG-MOSFETs suffer from intensified electric field crowding and enhanced drain-induced barrier lowering (DIBL), leading to greater post-SC leakage and thermal instability. Results suggest SG-MOSFETs require careful field and oxide engineering to ensure reliability under fault conditions.

Introduction

Silicon carbide (SiC) MOSFETs are widely adopted for high-power and high-frequency applications due to their superior thermal conductivity, breakdown voltage, and switching efficiency [1, 2]. However, their robustness under short-circuit (SC) conditions remains a critical reliability concern. [3-6] has gained particular attention. During SC events, the device must withstand large current surges under high drain bias without undergoing catastrophic failure. The short-circuit withstand time (SCWT) is a standard metric for assessing device survival under fault scenarios. Planar SiC VDMOSFETs are mature and reliable, but recent efforts have focused on Split-Gate (SG) MOSFETs [7], which reduce parasitic gate-drain capacitance (C_{gd}) and gate charge (Q_{gd}) , thus lowering switching loss.

Although prior studies report similar SCWT for SG and planar structures [8, 9], the impact of SG-induced electric field redistribution, especially at oxide corners—has not been fully characterized. Additionally, physical factors such as gate length and JFET width may affect both conduction loss and SC robustness. This study uses TCAD to compare SG and planar 4H-SiC MOSFETs under SC conditions, focusing on how design parameters impact SCWT, peak current, and failure mechanisms. The analysis reveals SG-specific vulnerabilities, particularly in oxide stress and DIBL-induced leakage, highlighting the need for structural and electrostatic optimization.

Methodology

To assess the short-circuit behavior of SG and planar 4H-SiC MOSFETs, two-dimensional TCAD simulations were conducted using Synopsys Sentaurus. A half-bridge circuit was modeled, in which one MOSFET was pulsed to create SC conditions while the other remained off. Gate voltage ranged from 0 to 15 V, and drain voltage was set at 600 V or 1000 V.

Key physical models included drift-diffusion transport, Shockley–Read–Hall and Auger recombination, and avalanche generation to accurately simulate high-field, high-temperature effects. It should be noted that the TCAD 2D electrothermal simulations employed in this study provide a

qualitative indication of the temperature increase within the device. While they effectively capture relative trends and mechanisms, they may not fully represent the complex 3D thermal dissipation paths present in a packaged device.

Both SG and planar device structures were constructed with variable parameters: drift layer thickness, gate length, and JFET width. The drift region was uniformly doped at 5×10^{15} cm^{-3}. Short-circuit performance was evaluated by extracting transient peak drain current, maximum lattice temperature, and SC withstand time (SCWT). Gate charge curves were analyzed to calculate Q_{gd} , and the high-frequency figure of merit (HF-FOM) [10] was used to assess switching efficiency. Electric field and conduction band profiles under SC stress were also examined to assess field crowding and DIBL-induced reliability concerns.

Results and Discussion

The simulated SC responses of planar and SG-MOSFETs reveal how structural differences influence device robustness. Emphasis was placed on the interaction between parasitic capacitances, conduction paths, and electrothermal effects that define SCWT. Fig. 1 presents the schematic cross-sections of both device types. The planar VDMOSFET employs a continuous polysilicon gate overlapping the JFET region, which inherently results in higher C_{gd} and Q_{gd}. In contrast, the SG-MOSFET introduces a split-gate structure that reduces the gate-to-drain overlap, thereby lowering C_{gd} and improving switching performance.

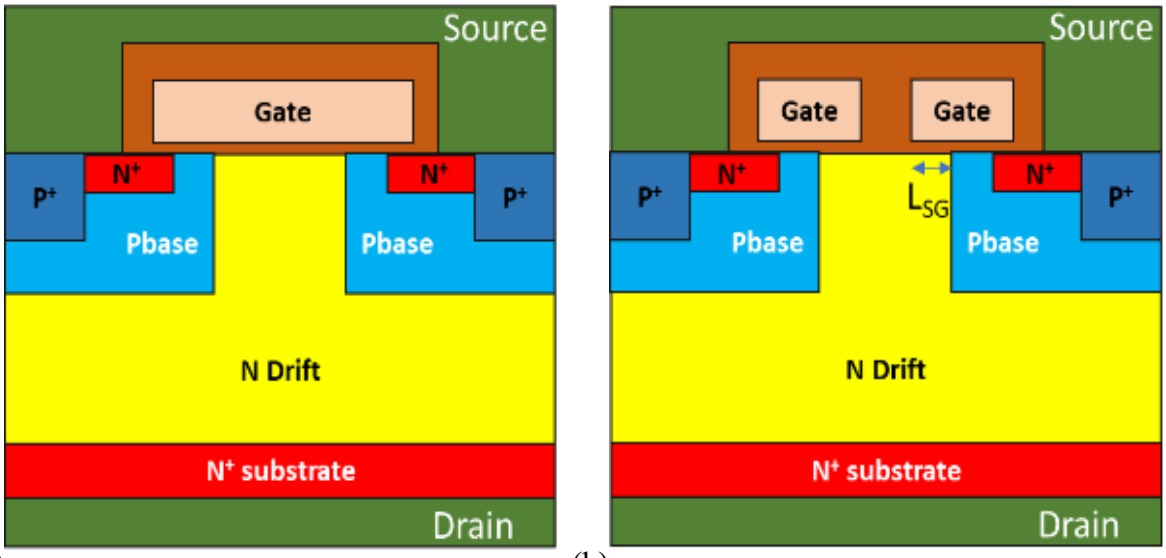


Fig. 1. Cross-sections of (a) planar VDMOSFET and (b) SG-MOSFET.

As shown in Fig. 2, increasing the drift region thickness significantly affects SC behavior. A thicker drift layer introduces greater series resistance, which limits the peak drain current during SC and delays thermal buildup. This extends SCWT by reducing the rate of self-heating. For instance, devices with a 15 µm drift layer show lower current peaks and slower temperature rise compared to those with 10 µm, resulting in several microseconds of additional SCWT. However, this improvement comes with increased $R_{on,sp}$, highlighting a trade-off between fault tolerance and conduction loss. Designers must therefore balance SC reliability against efficiency requirements when adjusting drift thickness.

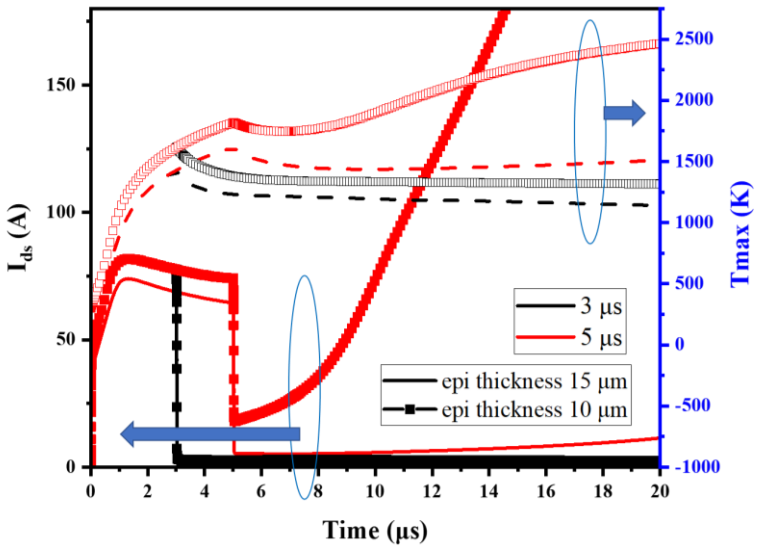


Fig. 2. Simulated SC drain current and maximum lattice temperature versus time for different epitaxial thicknesses.

Fig. 3 explores how gate length impacts $R_{on,sp}$ and HF-FOM in SG-MOSFETs. Shorter gates reduce C_{gd} and Q_{gd}, improving switching speed and lowering HF-FOM. However, they also weaken carrier accumulation in the JFET region, increasing $R_{on,sp}$ and degrading conduction efficiency.

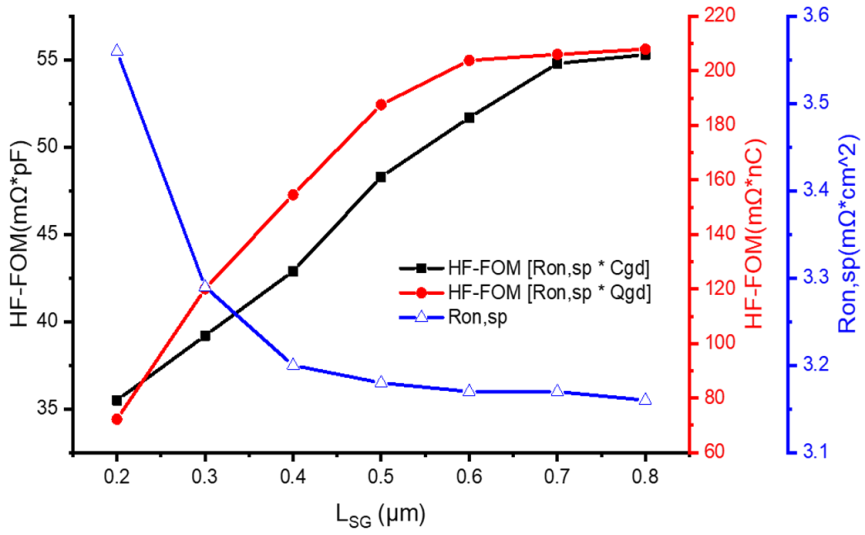


Fig. 3. Simulated $R_{on,sp}$ and HF-FOM relationship for different extended gate lengths.

Fig. 4 shows that narrowing the JFET width effectively reduces peak drain current during SC events, resulting in extended SCWT. For example, reducing the JFET width from 2.2 μm to 1.4 μm nearly doubles the SCWT, as the narrower current path limits surge current and delays thermal failure. However, excessive narrowing increases $R_{on,sp}$ and can degrade overall conduction performance. Moreover, tighter current confinement enhances electric field stress near the oxide interface, raising concerns about long-term reliability. These results indicate that while reducing JFET width is a viable strategy for improving SC tolerance, it must be balanced against static and dynamic performance penalties.

As shown in Fig. 5, reducing JFET width below 1.4 μm causes a sharp rise in $R_{on,sp}$ due to severe conduction constriction. While this improves SCWT, the gain is offset by degraded conduction efficiency. These findings emphasize that JFET scaling must avoid extremes, moderate narrowing is beneficial, but excessive reduction compromises both electrical and thermal stability.

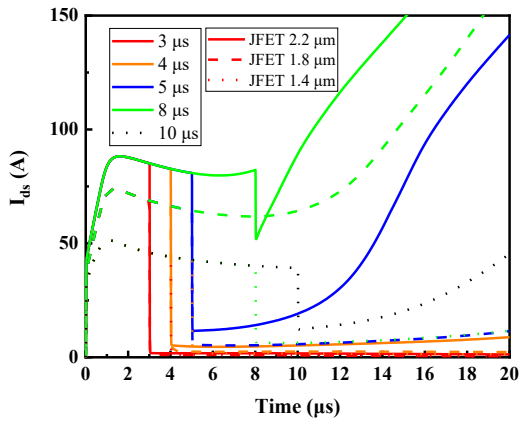


Fig. 4. Simulated SC drain current versus time with different JFET widths of SG-MOSFET. (V_{ds} = 1000V).

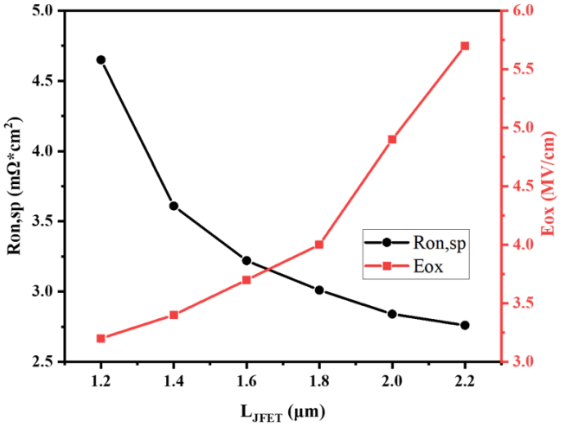
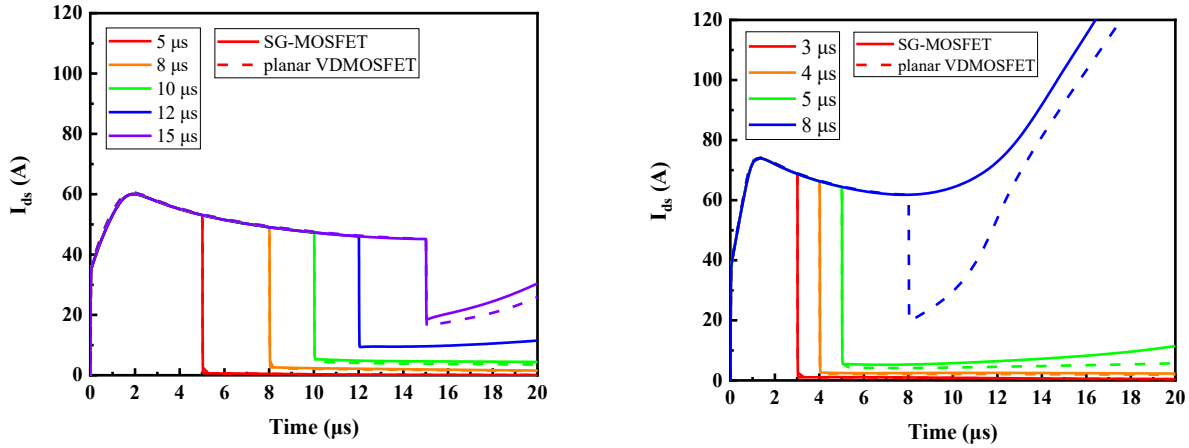


Fig. 5. Simulated relationship between JFET width, $R_{on,sp}$, and reverse oxide electric field.

Fig. 6 compares the SC current waveforms of SG and planar MOSFETs under identical bias conditions. Both exhibit similar SCWT, confirming that the split-gate structure does not compromise baseline SC survivability. However, post-SC behavior reveals critical differences. The SG-MOSFET demonstrates a more abrupt thermal runaway once failure initiates. This is attributed to its altered field distribution and lower Q_{gd}, which while beneficial for switching, result in faster energy accumulation and less thermal buffering during SC events. These results suggest that while SCWT remains comparable, the failure of SG-MOSFETs are more abrupt and thermally aggressive than the planar MOSFET.



(a) (b)

Fig. 6. Simulated SC drain current versus time comparison between planar VDMOSFET and SG-MOSFET. (a) V_{ds} = 600 V (b) V_{ds} = 1000 V.

Fig. 7 presents the electric field distribution under SC conditions at 1000 V. The planar MOSFET shows a relatively uniform field profile, with peak intensity near the drain junction. In contrast, the SG-MOSFET exhibits strong field crowding at oxide corners adjacent to the split gate. This localized enhancement raises the maximum oxide field ($E_{ox,max}$), increasing the likelihood of oxide degradation and triggering early failure mechanisms. The elevated field also intensifies susceptibility to DIBL, further contributing to leakage current growth and thermal instability. These results explain the more rapid failure escalation observed in SG-MOSFETs post-SCWT.

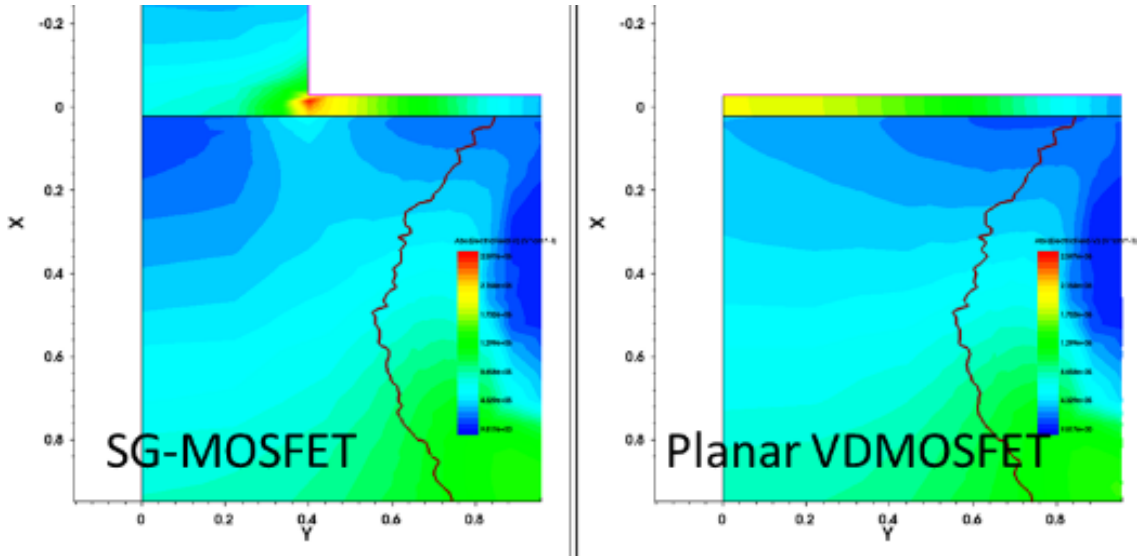


Fig. 7. Simulated electric field distributions under SC conditions (V_{ds} = 1000 V).

Fig. 8 shows conduction band profiles under SC stress. In the planar MOSFET, the conduction band maintains a stable barrier between source and drain, which helps limit leakage current even at high drain bias. In contrast, the SG-MOSFET exhibits a more pronounced band lowering near the JFET region—indicative of stronger DIBL effects. This band lowering accelerates leakage current growth beyond the SCWT threshold, compounding thermal stress and promoting rapid thermal runaway. While the split-gate design improves switching performance, it inherently compromises electrostatic control, making SG-MOSFETs more vulnerable under extreme SC conditions.

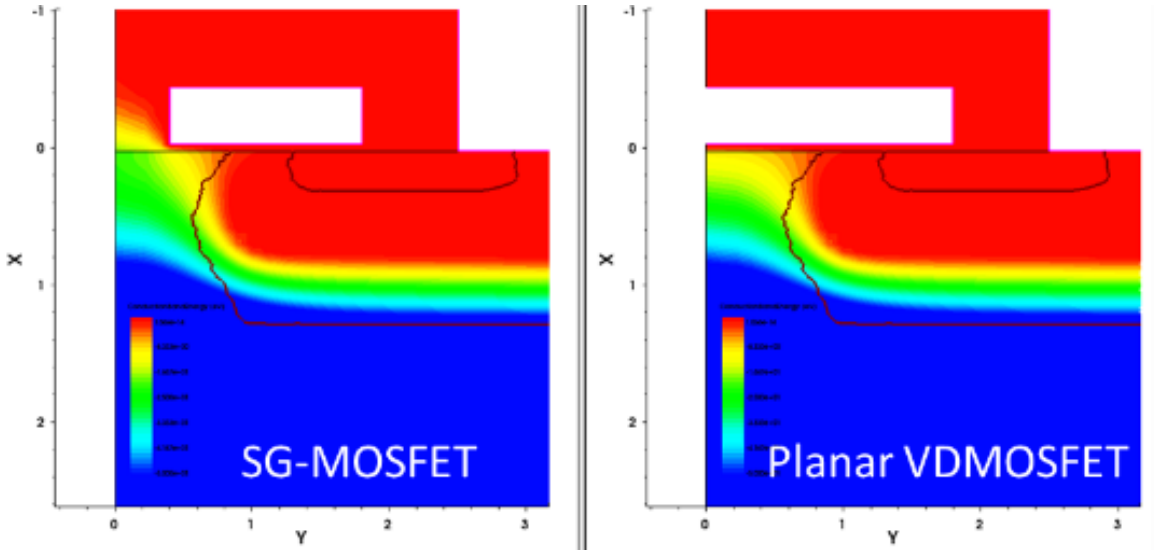


Fig. 8. Simulated conduction band energy profiles (V_{ds} = 1000 V).

Conclusion

This study presents a comparative TCAD analysis of SG- and planar 4H-SiC MOSFETs under short-circuit stress. While both achieve similar SCWT, SG-MOSFETs are more prone to post-SC degradation due to intensified oxide field and DIBL. Structural tuning—such as increased drift thickness, optimized gate length, and moderately narrowed JFET width—can effectively reduce Qgd, limit peak SC current, and improve HF-FOM. However, these benefits must be balanced against increased electric field stress and conduction losses. Future design strategies should prioritize field control near oxide corners to enhance SG-MOSFET reliability in high-stress environments.

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