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Impact of Active Cell Geometry on the Static Performance of 10-kV 4H-SiC JBS (Junction Barrier Schottky) Diodes

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Abstract. This study investigates the influence of active cell geometry on the static performance of 10-kV 4H-Silicon Carbide (SiC) Junction Barrier Schottky (JBS) diodes. Two types of diodes were fabricated and characterized, one with a hexagonal cell and the other with a stripe cell. While forward conduction characteristics were comparable, the reverse leakage current of the hexagonal cell was more than two orders of magnitude lower than that of the stripe cell at 8 kV. 3D TCAD simulations revealed that this discrepancy stems from strong electric field concentrations both at the bottom corners of the P^+ junctions and at the center of the Schottky contact in the stripe structure. These localized fields reduce the Schottky barrier height and enhance electron injection. In contrast, the hexagonal cell exhibited a more uniform electric field distribution in both regions, effectively suppressing leakage current. These findings underscore the critical role of active cell geometry in achieving robust reverse blocking performance in ultra-high-voltage SiC JBS diodes by clarifying the physical mechanisms contributing to leakage current behavior.

Introduction

Silicon carbide (SiC) has emerged as a leading material platform for next-generation high-voltage power semiconductor devices, owing to its outstanding material properties such as wide bandgap, high critical electric field, high thermal conductivity, and excellent radiation hardness [1]. These attributes allow SiC devices to operate with significantly lower conduction and switching losses compared to their silicon counterparts, making them highly suitable for demanding applications that require compactness, efficiency, and reliability [2]. In particular, SiC is widely adopted in power conversion systems for electric grids, renewable energy infrastructure, and defense systems where voltage ratings often exceed the limits of conventional silicon-based technology [3]. For applications operating at voltages beyond 10 kV, it becomes especially important to minimize reverse leakage current and maintain robust blocking capability to ensure reliable and long-term operation.

Key design parameters that influence the reverse blocking performance of SiC devices include epitaxial layer doping and thickness, edge termination structures such as JTE or floating field rings, and the geometry of the active cell layout [4-7]. Among these, the active cell geometry is a particularly critical factor, as it affects both forward and reverse behavior by shaping the electric field distribution and carrier injection dynamics under bias. Therefore, a well-optimized cell structure is essential for achieving low leakage current without degrading forward conduction characteristics.

In this study, we investigate the effect of active cell layout on the static performance of 10-kV 4H-SiC junction barrier Schottky (JBS) diodes. Devices were designed and fabricated with two different active cell structures, one with a hexagonal pattern, which exhibits an enclosed geometry, and the other with a stripe pattern. Their forward and reverse characteristics were experimentally evaluated, and 3D TCAD simulations (Synopsys Sentaurus) were performed to analyze the electric field distribution in each structure.

The results demonstrate that the hexagonal layout effectively reduces field concentration and suppresses reverse leakage current while maintaining comparable forward conduction behavior.

Device Design and Simulation

To investigate the impact of active cell geometry on the static performance of ultra-high-voltage SiC JBS (Junction Barrier Schottky) diodes, two types of devices were designed and fabricated, one employing a hexagonal cell layout and the other a stripe cell layout. Both structures were configured with identical design parameters for a fair comparison, specifically setting the P^+ region width (L_{pp}) to 2.0 µm and the Schottky contact width (L_{sch}) to 3.0 µm. Fig. 1 illustrates the top and cross-sectional views of each design, extracted directly from the GDS layout.

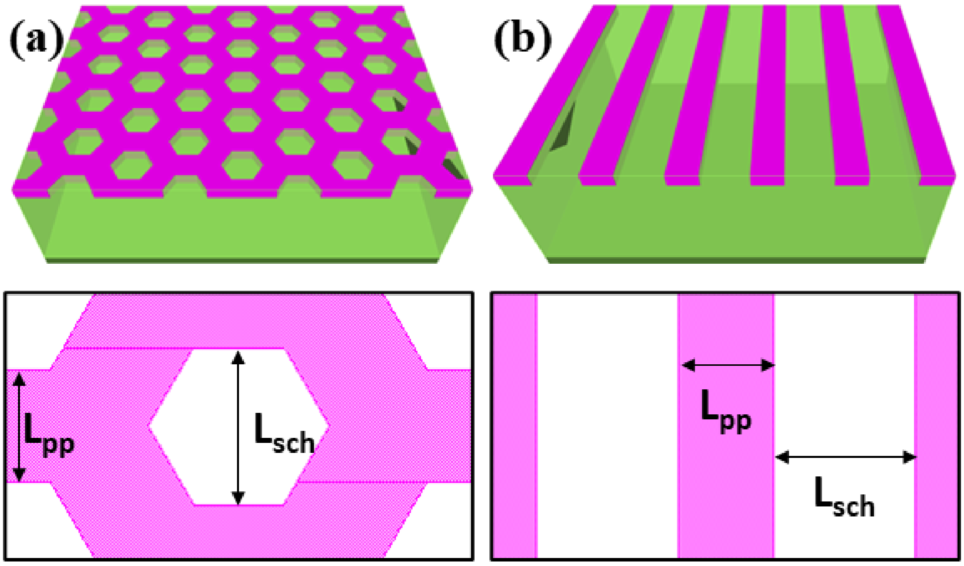

Fig. 1. Schematic top and cross-sectional views of 10-kV SiC JBS diodes with two different active cell geometries, (a) hexagonal and (b) stripe layouts. Both designs share identical cell dimensions, with the P^+ region width (L_{pp}) set to 2.0 µm and the Schottky region width (L_{sch}) set to 3.0 µm.

The devices were fabricated on a 6-inch, n-type 4H-SiC wafer with an epitaxial drift layer engineered for 10 kV blocking capability. A Surface region was first formed through nitrogen ion implantation at room temperature. This step was performed prior to the P^+ region formation to locally increase the carrier concentration beneath the Schottky contact for improved current spreading, and to suppress excessive lateral straggle of the subsequent P^+ implantation, thereby enabling precise definition of the Schottky contact width (L_{sch}). The P^+ regions were then formed via high-temperature aluminum ion implantation, followed by high-temperature activation annealing. A Ni metal layer was deposited on both the front and back sides of the wafer, and Rapid Thermal Process (RTP) was carried out to simultaneously form a P^+ ohmic contact on the front side and an N^+ ohmic contact on the back side. Subsequently, Ti was deposited on the front side as part of the top metal stack, forming a Schottky contact with the n-type drift layer in regions not implanted with aluminum ions. Finally, metal layers were deposited on both the front and back sides to complete the device fabrication.

To analyze the underlying physical mechanisms responsible for differences in device behavior, 3D TCAD simulations were performed using Synopsys Sentaurus. Both the hexagonal and stripe designs were modeled with full 3D structures incorporating the same design dimensions used in the fabricated devices. Fig. 2 shows the simulated geometries of the hexagonal and stripe designs, while Fig. 3 presents the doping profile used for the P^+ junction regions. The implantation model used in the simulation was pre-calibrated using actual SIMS (Secondary Ion Mass Spectrometry) data obtained from fabricated devices, in order to closely replicate the realistic junction depth and dopant concentration profile of the P^+ implantation. The simulations were configured to evaluate forward and reverse characteristics, with particular focus on electric field distribution and current conduction paths under reverse bias conditions.

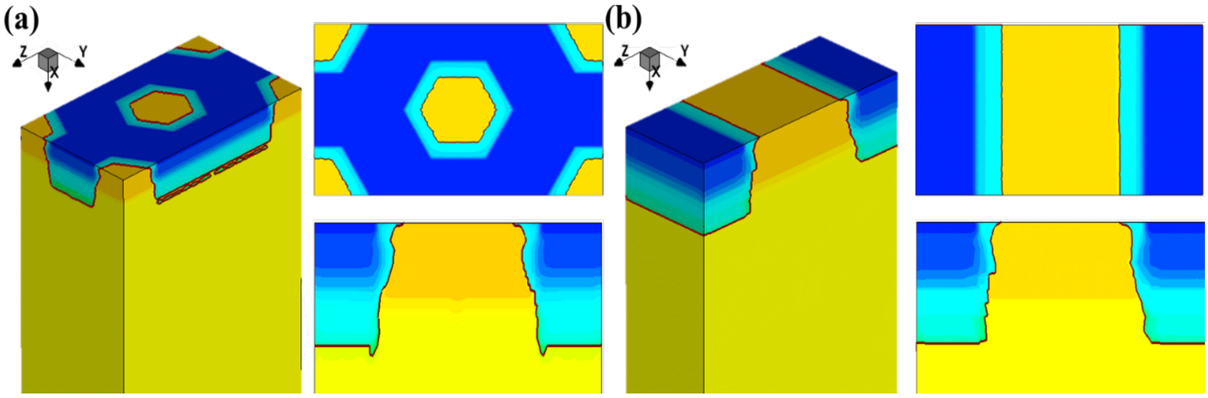

Fig. 2. Simulated geometries of 10-kV SiC JBS diodes with (a) hexagonal and (b) stripe active cell designs. Each set shows the 3D isometric view (left), top view (top right), and cross-sectional view (bottom right) of the modeled structure used in the TCAD simulation.

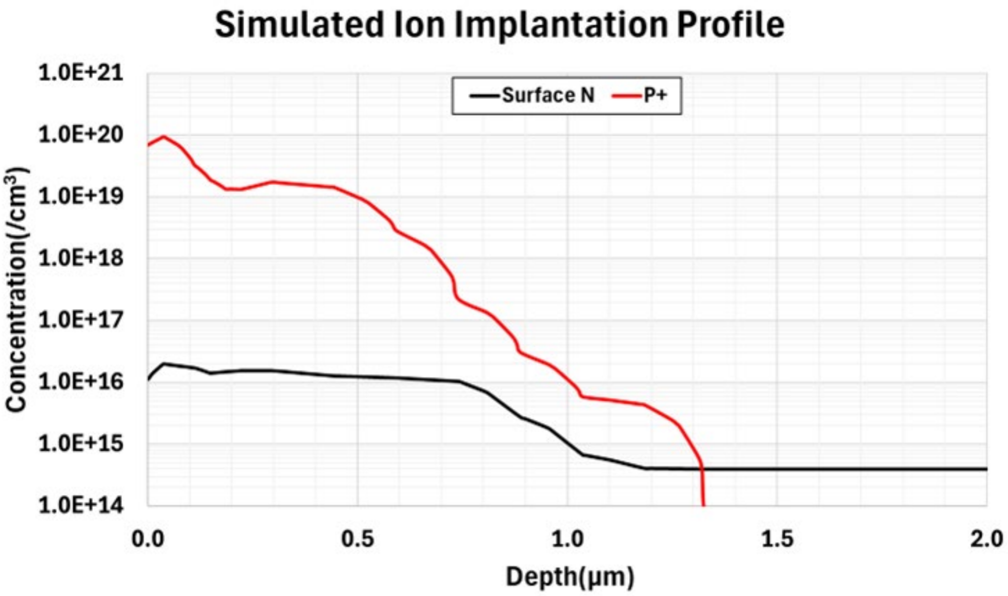

Fig. 3. Simulated Surface N and P^+ ion doping profile used in the TCAD simulation.

Results and Discussion

The electrical characteristics of the fabricated 10-kV SiC JBS diodes with hexagonal and stripe active cell designs were experimentally evaluated under both forward and reverse bias conditions. Fig. 4 shows the forward I–V characteristics, which represent the average response of approximately 20 devices for each structure. At a forward current of 0.5 A, the forward voltage drop was measured to be 3.70 V for the hexagonal cell and 3.48 V for the stripe cell, corresponding to a difference of 0.22 V. While this indicates a slight increase in conduction loss for the hexagonal design, both structures still maintain comparable forward behavior within typical operating margins for 10 kV-class SiC diodes. This result confirms that the impact of active cell geometry on forward conduction behavior was effectively minimized within the tested current range.

In contrast, a significant difference was observed in reverse leakage characteristics, as illustrated in Fig. 5. Due to limited reverse yield, representative single-device measurements are shown. Under a reverse bias of 8 kV, the leakage current was measured to be 4.0×10^{-8} A for the hexagonal cell and 1.0×10^{-5} A for the stripe cell. This demonstrates that the hexagonal design achieves more than two orders of magnitude reduction in leakage current compared to the stripe layout, highlighting the importance of cell geometry in optimizing reverse blocking performance for ultra-high-voltage applications.

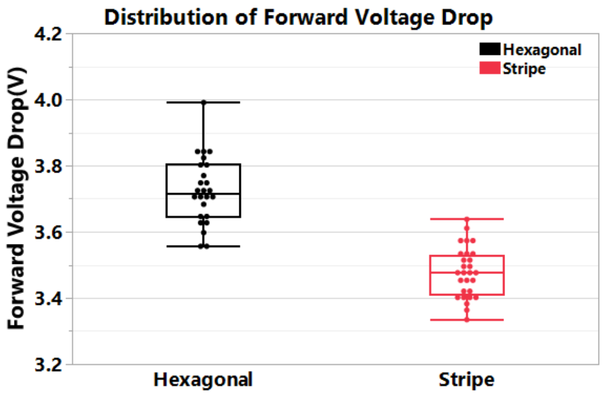

Fig. 4. Statistical comparison of forward voltage drop for hexagonal and stripe active cells. Box plots reflect approximately 20 wafer-level measurements per structure, with median voltage drop values of 3.70 V for the hexagonal design and 3.48 V for the stripe design.

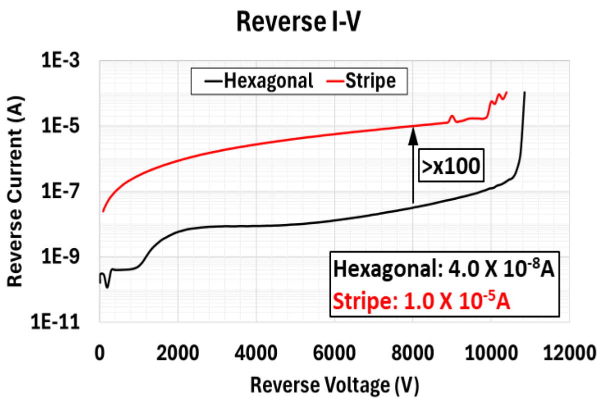

Fig. 5. Representative reverse I–V characteristics of 10-kV SiC JBS diodes based on single-device measurements. At a reverse bias of 8 kV, the leakage current was 4.0×10^{-8} A for the hexagonal design and 1.0×10^{-5} A for the stripe design, showing a difference of more than two orders of magnitude.

To investigate the physical mechanisms behind this discrepancy, 3D TCAD simulations were carried out for both designs. Fig. 6 shows the electric field distributions under reverse bias conditions. The left-hand side presents isometric views of the electric field distribution, while the top and bottom images on the right provide surface plots of the electric field at critical locations, the bottom of the P^+ junction (ABCD plane) and the surface center of the Schottky region (A′B′C′D′ plane), respectively. The simulation results clearly reveal that the electric field is more uniformly distributed in the hexagonal design, while strong field crowding is observed at the P^+ junction corners and Schottky surface in the stripe structure.

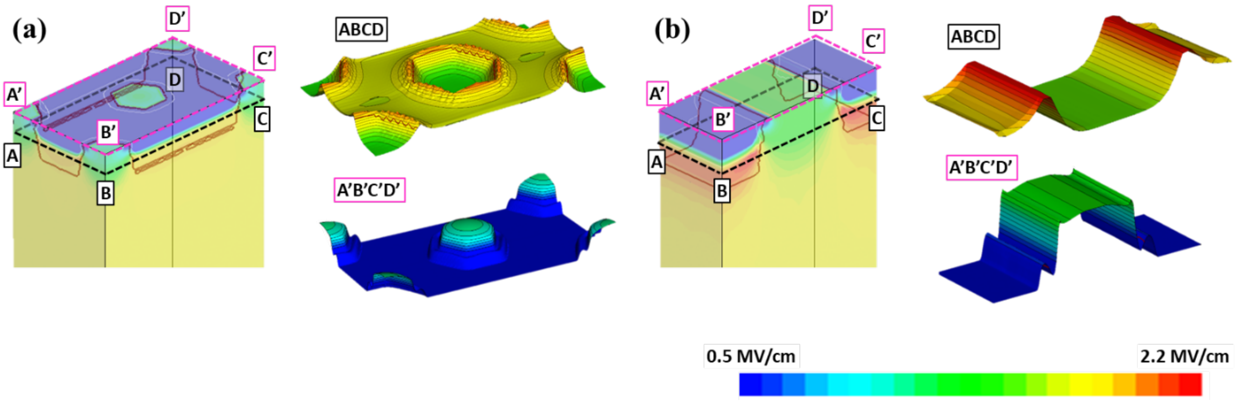

Fig. 6. Simulated electric field distributions under reverse bias conditions for 10-kV SiC JBS diodes (a) Hexagonal active cell design and (b) Stripe active cell design. Each subfigure shows a 3D isometric view (left), an electric field surface plot at the bottom of the P^+ junction (ABCD plane, top right), and a surface field plot near the surface region (A′ B′ C′ D′ plane, bottom right).

Quantitative analysis of the electric field profiles is provided in Fig. 7, which compares the 1D vertical electric field distribution along the drift depth at representative high electric field locations. The peak electric field at the P^+ junction bottom corner was 2.02 MV/cm for the hexagonal cell and 2.25 MV/cm for the stripe cell. Similarly, at the surface center of the Schottky region, the local electric field was 1.13 MV/cm for the hexagonal design and 1.43 MV/cm for the stripe. These results indicate that the stripe geometry induces stronger electric field peaks at both the P^+ junction corner and the Schottky surface center. This increased field concentration may lead to enhanced electron tunneling or field-assisted thermionic emission, effectively narrowing the barrier width.

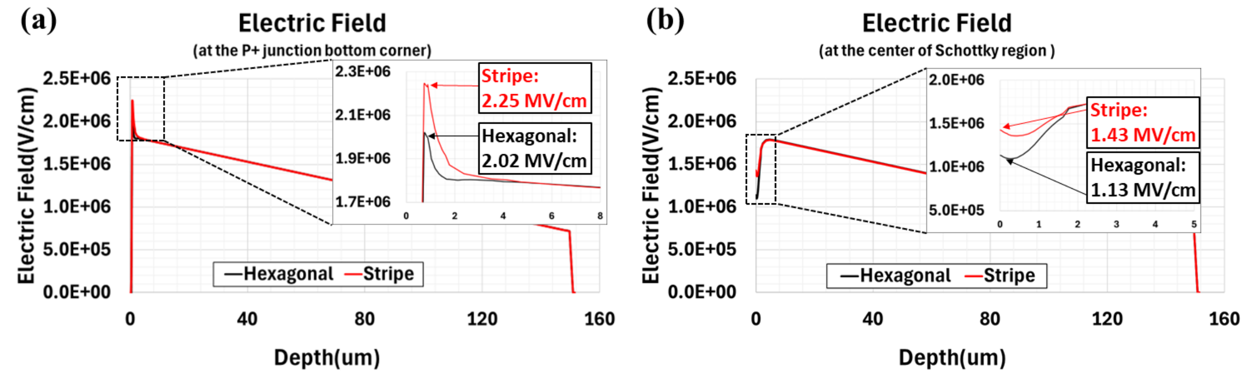

Fig. 7. Simulated 1D vertical electric field distributions along the drift depth for the hexagonal and stripe JBS diode structures under reverse bias. (a) Electric field at the P^+ junction bottom corner and (b) Electric field at the surface center of the Schottky region. The hexagonal design exhibits lower peak electric field values at both locations compared to the stripe design.

These field-enhanced mechanisms are likely to facilitate increased electron injection from the Schottky contact into the drift layer through tunneling or field-assisted thermionic emission, which aligns with the elevated leakage current observed in the stripe device. In contrast, the hexagonal cell structure results in a more uniform electric field distribution and inherently provides better shielding of the Schottky surface by the surrounding P^+ regions due to its enclosed layout [8].This shielding effect reduces the electric field intensity at the Schottky interface, thereby suppressing Schottky barrier lowering and limiting unwanted carrier injection. As a result, the hexagonal design achieves significantly lower reverse leakage current with minimal impact on forward conduction performance. A summary of the key simulation and measurement results is presented in Table 1, clearly illustrating the relationship between active cell geometry, electric field behavior, and reverse leakage characteristics.

Table 1. Summary of measured electrical characteristics and simulated peak electric fields for hexagonal and stripe JBS diode designs.

Active Cell	Forward Voltage Drop [V, measured]	Reverse Leakage Current [A, measured]	Peak Electric Field at P^+ junction bottom corner [MV/cm]	Peak Electric Field at Schottky surface [MV/cm]
Hexagonal	3.70	4.0×10^{-8}	2.02	1.13
Stripe	3.48	1.0×10^{-5}	2.25	1.43

Summary

This study investigated the effect of active cell geometry on the electrical performance of 10-kV 4H-SiC junction barrier Schottky (JBS) diodes by comparing hexagonal and stripe cell layouts. Both structures were designed with identical process parameters and fabricated on 6-inch 4H-SiC wafers. Experimental measurements revealed that while forward characteristics were similar between the two designs, the hexagonal cell exhibited significantly reduced reverse leakage current, over two orders of magnitude lower than that of the stripe cell at 8 kV reverse bias. To understand this improvement, 3D TCAD simulations were conducted, showing that the hexagonal design suppresses peak electric field intensity both at the P^+ junction corner and Schottky surface center. This reduction in electric field mitigates Schottky barrier lowering and minimizes electron injection under reverse bias. These results suggest that the hexagonal active cell layout is a promising design choice for enhancing the reverse blocking performance of ultra-high-voltage SiC JBS diodes without compromising forward conduction efficiency.

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