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Gate Leakage Imaging of Silicon Carbide Power MOSFETs under Negative-Bias Gate Stress

Andrei Konstantinov[1,a], Shagufta Naureen[1,b], Sergey Reshanov[1,c]
and Jang-Kwon Lim[2,d*]

[1]II-VI Kista AB, Electrum-207, 16440 Kista, Sweden

[2]RISE AB, Electrum-236, 16440 Kista, Sweden

[a]Andrei.Konstantinov@cohetent.com, [b]Shagufta.Naureen@coherent.com,
[c]Sergey.Reshanov@cohenent.com, [d*]Jang-Kwon.Lim@ri.se

*corresponding author

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Abstract. Visible light emission was observed for negative-bias gate stress of n-channel power MOSFETs in 4H-SiC. The emission intensity is approximately proportional to the current through the gate oxide; and its pattern follows the configuration of active MOSFET channels. We relate the emission to recombination of the electrons injected from the gate into the oxide with valence-band holes from SiC at the surface states at the SiC-to-oxide interface. The gate leakage imaging technique may be helpful for locating different types of gate oxide current crowding, which crowding might cause enhanced wear-out of the gates and early device failure.

Introduction

Reliability of gate oxides in silicon carbide power MOSFETs has significantly improved in recent years. However, it might take further effort to reach the same reliability level as that offered by silicon power devices. A significant roadblock comes from limited set of available efficient tools. Reliability-related device development techniques are often based on statistical analysis of failures under lengthy stress. An option for direct imaging the gate leakage could enhance development of reliable SiC MOSFETs. In this work we demonstrate a prospective approach based on imaging visible light emission from the gate oxide interface to SiC under negative bias gate stress conditions.

Visible light emission from the interface of gate oxide to SiC was first reported for lateral SiC MOSFETs by Macfarlane and Stahlbush from the NRL [1,2], who employed pulsed gate biasing to form an inversion channel with subsequent release of the interface-trapped electron charge. This excitation technique is similar to well-known charge pumping. Depending on the voltages of high and low gate-bias levels, visible light emission spectra correspond to either bulk recombination in SiC or to recombination at the oxide interface states. A recent series of spectral and imaging studies applied the Macfarlane-Stahlbush technique to SiC power MOSFETs; which summary can be found in [3].

In this study we report visible light emission upon negative and positive gate bias stress; we discuss emission mechanisms and potential practical applications of gate current imaging.

Results and Discussion

Power MOSFET wafers were processed at a foundry with a target rated voltage of 1200 V. The MOS-channels were formed by thermal oxidation, which was followed by a nitridation anneal and by a deposition of polysilicon gates. Imaging analysis was done after removing the backside contact to observe the emission through the SiC crystal using an inverted microscope with a cooled panchromatic CCD camera from Hamamatsu. Negative gate-to-source bias was applied to maintain a gate current of 100 μA. Low-magnification (2× objective) emission image of a power MOSFET displayed in Fig. 1(a) shows a fairly uniform gate current density. No emission comes from the gate pad or from the gate runner. The CCD readouts were proportional to the gate current for the same exposure time. High-magnification (40× objective) image shown in Fig. 1(b) reveals certain details of the active structure of the device.

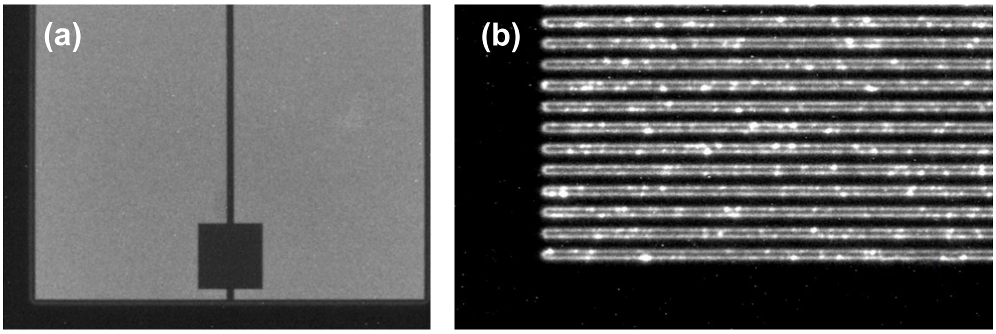

Fig. 1. Backside-imaged power MOSFET emission for negative-bias gate stress at a gate current of 100 μA at low (a) and high magnification (b).

In order to locate the regions of peak light emission, reflected-light micrograph was taken through the wafer backside. Backside reflected light image of Fig. 2(a) is complemented by two aligned inserts, showing the polysilicon gate outline and the gate emission. The peak light intensity follows the outline of the p-wells, although some emission also comes from the regions above vertical n-JFETs. Those regions are shown on a schematic cross-section in Fig. 2(b). Certain non-uniformity of emission is observed at microscopic-scale, which origin is yet unclear; it might come from step bunching of the SiC surface, or from process-related fluctuations of the p-well width.

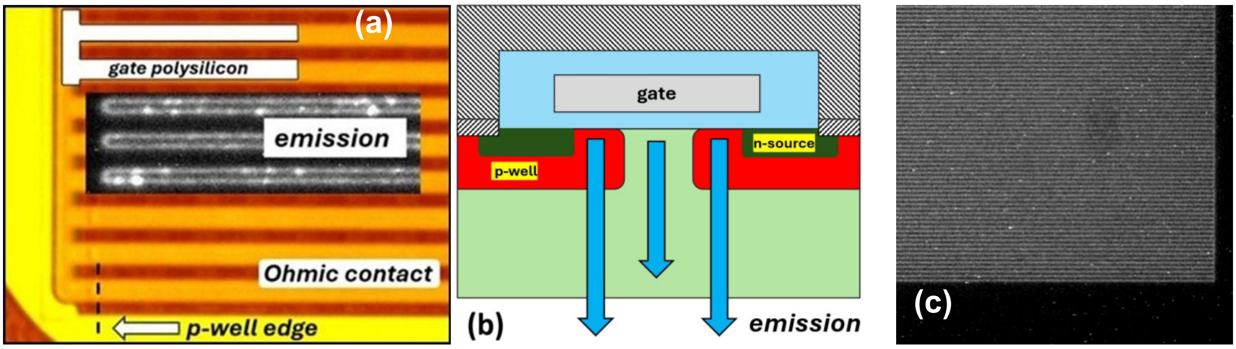

Fig. 2. Backside-imaged reflection micrograph with aligned insets for gate polysilicon configuration and for emission (a) and the cross-section of MOSFET unit cell (b); and positive gate-bias emission image for gate current of 200 μA (c).

Light emission was also observed for a positive gate bias, however, its intensity was much weaker than for the negative gate polarity. Shown in Fig. 2(c) is a medium-magnification (10× objective) image for a positive-bias at gate current of 200 μA. The CCD readout for a negative gate bias at 100 μA were 25 times higher with the same objective, implying a 50× higher emission yield per charge carrier passed through the gate oxide. At high magnification (40× objective) the image quality was very poor due to too low light intensity.

We made a comparison of the stress-induced emission with that due to the charge-pumping using the conditions reported by Macfarlane and Stahlbush [1]. A square-wave gate-to-source bias with high and low levels of +8 V and -8 V respectively was applied to the MOSFET gate with the source grounded. Alternating gate polarity results in a recombination of free carriers of the gate-induced channel with the opposite-polarity charge trapped at the surface states during the preceding half-period. Light emission could be recorded even with a relatively low pulse frequency of 100 kHz. Negative-bias stress was done after the charge pumping to compare the pattern of light emission between the two techniques. High negative DC bias was applied to the gate of a test MOSFET to drive the same current density as that used for imaging a large area power MOSFET.

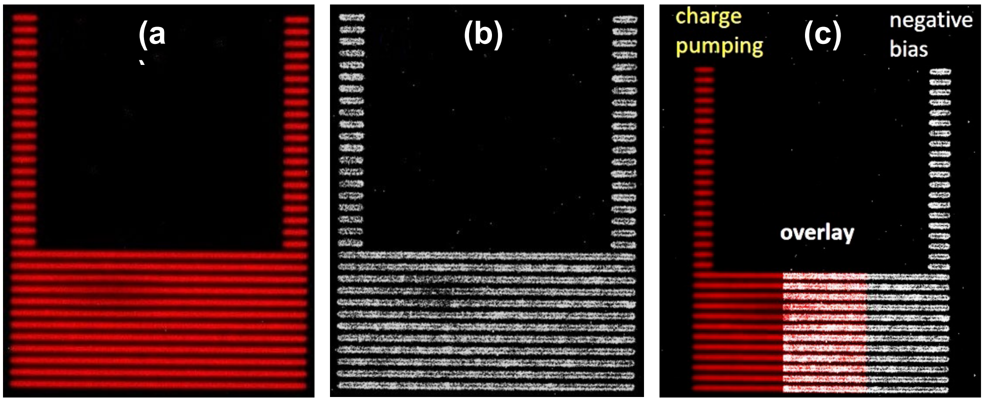

Fig. 3. Emission of a small-area test MOSFET under charge pumping (a), under negative-bias stress (b), and partial overlay of the two emission images (c).

Emission images of a small-area test MOSFET are shown in Fig. 3. The active region of the test MOSFET followed the same design rules as the high-power MOSFET. Fig. 3(a) corresponds to the charge pumping mode, and emission is assigned red color. Emission image for the negative-bias stress is shown in Fig. 3(b). A partial overlay of the two emission images is shown in Fig. 3(c), in which portions of emission in Figs. 3(a) and 3(b) were electronically removed to leave an overlay in the central area only. The charge pumping yields more uniform emission with no enhancement in the p-well regions. It is also not as grainy as that from DC stress. Overall configuration is identical; both types of emission come from the MOSFET p-wells and from the vertical JFETs.

We will now discuss the light emission mechanism. Shown in Fig. 4(a) is the band alignment of the MOSFET under the conditions of negative-bias gate stress. High-field carrier transport in silicon dioxide is governed by conduction-band electrons, which are driven by electric field from the gate to towards the interface to SiC. The holes of the SiC valence band are driven to the same interface, at which point they recombine with the electrons. Recombination results in light emission from the same interface traps as that for the charge-pumping studied in [1-3].

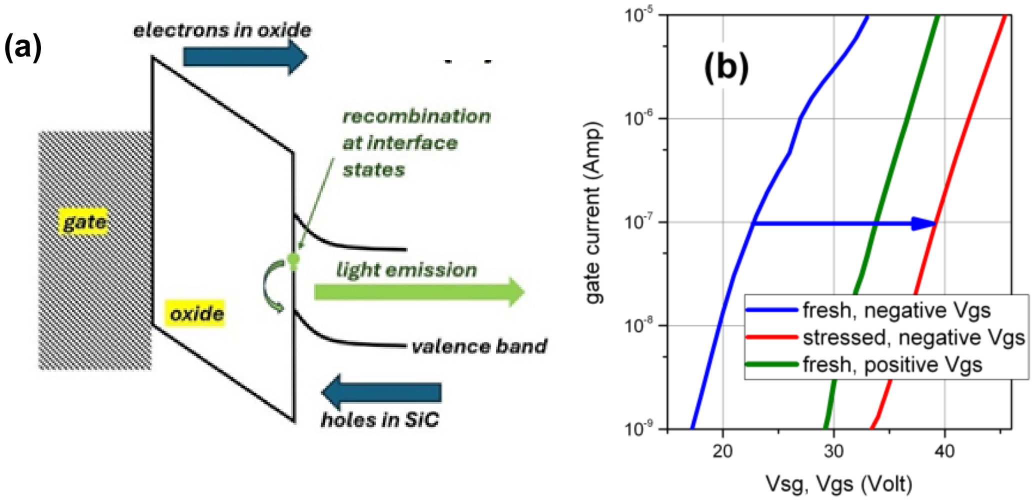

Fig. 4. Electron band diagram for negative-bias gate stress (a), gate-to-source electrical characteristics (b).

The dependence of gate current on absolute value of gate-to-source bias is plotted in Fig. 4(b) for positive and negative gate bias conditions. High negative gate bias results in a very strong charging of the oxide interface, as is seen in Fig. 4(b): prolonged negative bias results in a voltage shift of 10 – 20 Volt. Such interface charging is quite typical for the negative-bias SiC MOSFET stress as was reported in multiple publications [4,5]. The positive charge captured at or next to the interface can often be neutralized by positive gate bias, however high and/or prolonged negative gate bias may result in a permanent shift of the threshold voltage of the MOSFET.

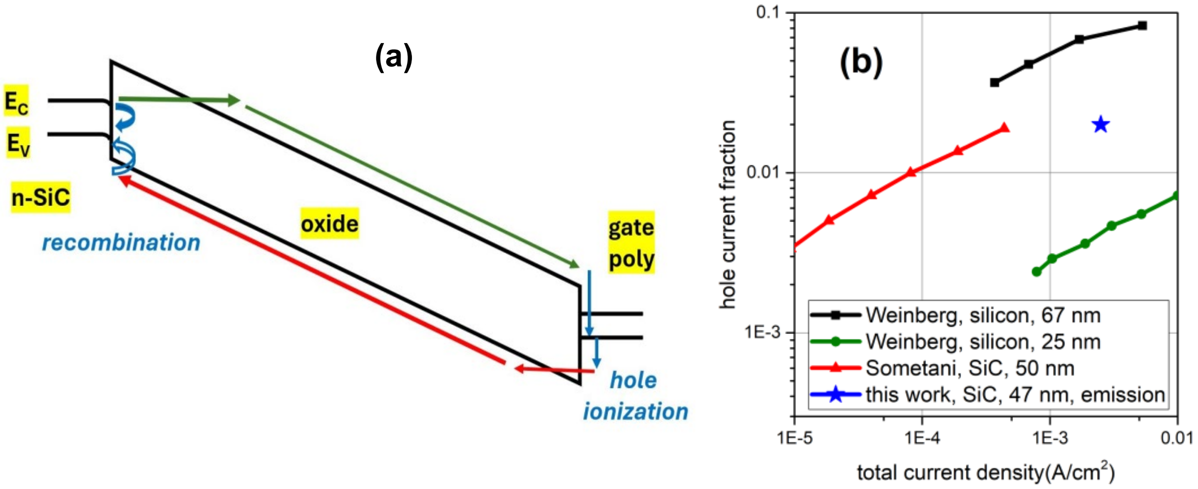

Fig. 5. Electron band diagram for positive-bias gate stress (a), and the fraction of holes in total oxide current for silicon and SiC for positive-bias gate stress (b).

For positive gate polarity the charge trapping is not as pronounced. Electrical characteristics are in this case governed by electron tunneling from the surface accumulation or inversion layer in SiC to the oxide. The carriers that tunneled though the barrier travel over the oxide to the gate, and this process should not cause any light emission unless some holes are generated on the path. Such generation of holes is well-known for silicon MOSFETs at very high electric fields in the oxide. Its dominant mechanism is related to impact ionization by hot electrons in the oxide at the anode [6], as shown schematically in Fig. 5(a).

In silicon MOSFET technology, holes generated in the gate oxide are often measured using a charge separation experiment, which utilizes a lateral n-channel MOSFET on a p-type substrate. Weineberg *et al.* [7] detected the generation of holes in the oxide by measuring the p-substrate current of a planar n-MOSFET at positive bias at the gate. The substrate current is zero if no ionization events occur in the oxide or next to the anode. The substrate current shows up as the gate-to source bias is increased to cause ionization. Plotted in Fig. 5(b) are the data of Weinberg *et al.* [7] for hole generation in silicon MOSFETs as a function of the gate current density and oxide thickness. A similar charge separation experiment was reported for 4H-SiC by Sometani *et al.* [8], the data of which are also plotted in the figure. The power MOSFET is not suitable for charge separation because the p-bodies are shorted to the source. It is nevertheless possible to roughly estimate the hole current fraction from the ratio of emission efficiency for positive and negative gate bias conditions, which number is around 0.02, as discussed above. This data point shown in Fig. 5(b) is in reasonable agreement with published results of charge separation experiments for silicon and for SiC.

Early gate leakage of a power MOSFET represents a significant reliability issue, especially if the gate current is highly localized. Gate-oxide current flow in a power MOSFET may result in wear-out of the oxide, which wear-out rate is governed by the current density. Inspection of MOSFET electroluminescence due to gate stress might therefore be a useful means of detecting crowding of the gate current, which may cause early failure. An example image from examination of a problematic design using this technique is shown in Fig. 6. The MOSFET sample under study was obtained from an external vendor. Fig. 6(a) shows a low-magnification emission image under negative gate-to-source bias for a portion of high-power MOSFET. No emission occurs from the gate pad, which is physically in the bottom part of the image. Regions of very strong emission are observed around the periphery of the active region. High-magnification emission image of the left bottom corner is shown in the insert to Fig. 6(a).

The ledged region of bright emission in the chip corner coincides with a pattern, observed through the substrate in reflected light, Fig. 5(b). Marked with a dashed line is the edge of the gate poly that yields a lighter tone due to reflection. The small dark squares are the locations of Ohmic contacts. The gate intersects a ledged pattern, which appears to be an imprint of the mask used for subcontact p+ implant. Heavy p-type doping of this ledged region is confirmed by SEM inspection that was done after removing all metals and dielectrics from the top side of the SiC MOSFET chip. The potential-contrast SEM image in Fig. 6(c) indeed shows high p-type doping in the ledged region, which brighter tone corresponds to high p-type doping. Similar gate overlaps with p+ were found next to the gate pad and to the gate runner in the middle part of the device, Fig. 6(a).

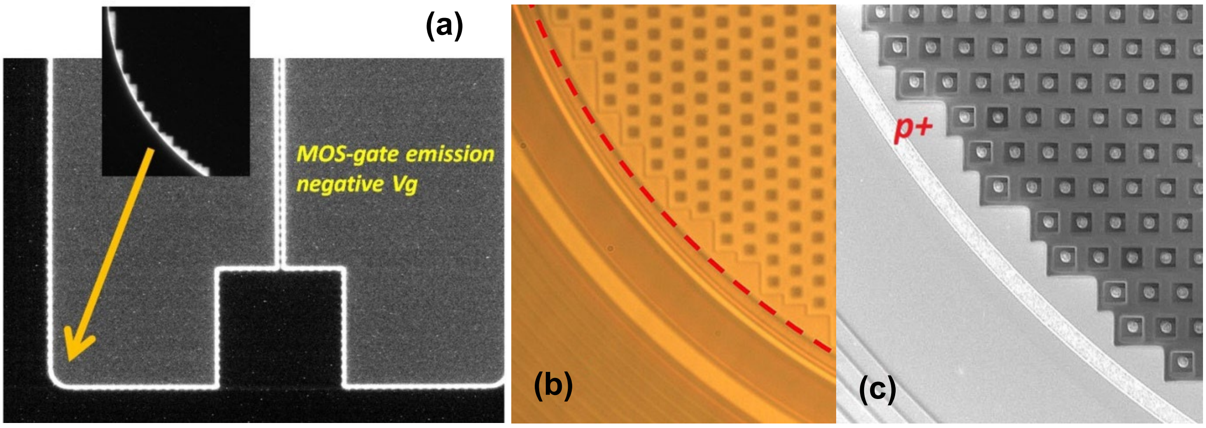

Fig. 6. Images of a MOSFET from external vendor in electroluminescence (a), in backside-reflected light (b), and in potential-contrast SEM (c).

Crowding of the gate current in the power MOSFET shown in Fig. 6 therefore occurs due to overlapping of the gate oxide with a heavily doped p-type region. Heavily doped p-type SiC has a lower barrier to hole injection into the oxide than the p-well or the n-type JFET. Deterioration of oxide quality due to heavy p-type doping might also contribute to gate current crowding.

Summary

To summarize, we demonstrated the feasibility of imaging the gate leakage pattern in a vertical 4H-SiC power MOSFET using a negative-bias gate stress. For devices having nearly uniform flow of the gate current, the emission occurs from the p-wells and from the vertical JFETs of the MOSFET structure. The emission mechanism is believed to be similar to the light emission due to charge pumping [1-3]; it is related to recombination of electrons and holes at the traps at oxide-SiC interface. Electrons passing though the oxide recombine with valence-band holes from SiC at the interface states. The new imaging technique provides a straightforward means of detecting weak spots of the gate oxide having high density of leakage current, which weak spots may compromise device reliability.

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