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Fowler-Nordheim Current at Negative Gate Bias in SiC MOSFETs

D. Scholten[1,a*], J. Ziegler[2,b], W. Feiler[2,b]

[1]Advanced Technologies and Micro Systems, Robert Bosch GmbH, Germany,

[2]Mobility Electronics, Robert Bosch GmbH, Germany

[a]dick.scholten@de.bosch.com, [b]johannes.ziegler2@de.bosch.com,
[c]wolfgang.feiler@de.bosch.com

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Abstract. We show that various commercially available silicon carbide MOSFETs exhibit significant gate leakage current at gate voltages below -20 V. With prolonged negative bias stress, this leakage current reduces by several orders of magnitude. Literature [1–4] suggests that this current is due to hole current from the silicon carbide and explain the current reduction by the discharge of neutral electron traps at the SiC/SiO_2-interface. However, measurements on n^+-doped SiC-MOSCAPs, where we avoid hole current, exhibit similar gate leakage behavior, indicating that there might be an alternative explanation. Further measurements show that the threshold voltage is not significantly impacted by the negative gate bias stress, indicating that the channel region is not involved in the gate leakage current and its reduction due to trapping effects. Devices with a floating source do not show leakage, and we therefore conclude that the origin of the gate leakage is in the source region. An analytical calculation is used to show that field enhancement at the edges of the polysilicon gate electrode, assuming a corner radius below 10 nm, may explain the onset voltage of the gate leakage current at negative bias. Alternatively, gate oxide damage from the polysilicon etching process may also explain the leakage current. The reduction of the onset voltage of the gate leakage with prolonged negative voltage gate stress, may be explained by significant electron trapping due to the high local current density at the poly-silicon gate electrode corner.

Introduction

The minimum rated gate voltage of commercial SiC MOSFETs typically ranges between -15 V and -4 V. Lower gate voltages may be employed for accelerated testing, such as in time-dependent dielectric breakdown (TDDB) with negative gate voltage, threshold voltage drift under negative gate bias, or bipolar dynamic gate switching stress. However, at very low gate voltages, typically below -15 V, several studies report significant gate leakage currents that decrease with continued negative gate voltage stress [1–4]. To evaluate the impact of the gate leakage on the accelerated reliability tests, a comprehensive understanding of its root cause is necessary. The prevailing hypothesis in these studies suggests that this current is a hole current from the silicon carbide towards the gate electrode. The reduction of hole current with continuing negative bias stress is explained by neutral near-interface traps that discharge electrons, thereby increasing the barrier height for holes.

In this paper, we investigate the location of the gate leakage and focus on the corners of the polysilicon gate electrode. Fig. 1 shows a schematic cross section of a typical planar and a typical trench MOSFET, where the edges of the poly-silicon gate electrode are indicated by the dashed circles.

We will show the gate leakage for negative gate voltage from different commercially available devices and compare that with results measured from SiC MOSCAP testing structures. To estimate the impact of the gate electrode geometry, we will present a calculation method to estimate the field enhancement factor from the radius of curvature of the poly-silicon edges.

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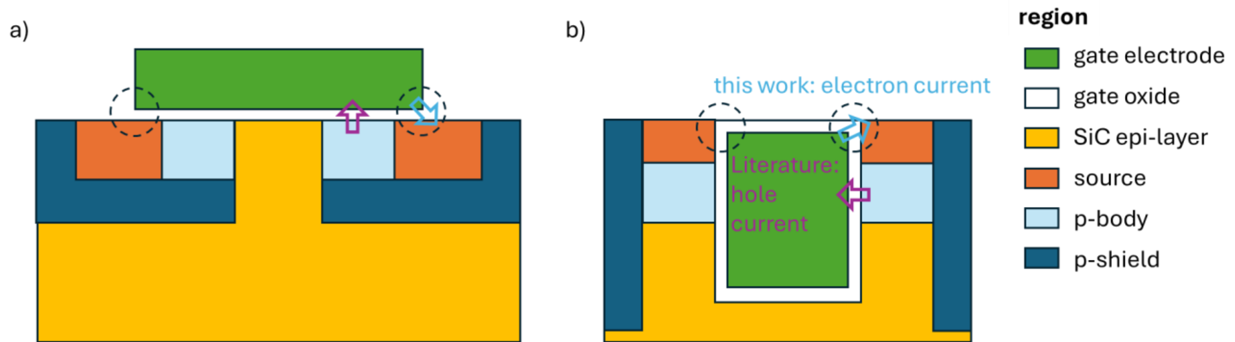

Fig. 1. Schematic cross sections of different typical SiC MOSFET cell concepts. Dashed circles indicate poly-silicon corners at the gate electrode opposite the source region. Plum and blue colored arrows indicate leakage current paths as proposed in literature and in this work. a) planar cell concept. b) trench cell concept.

Gate Voltage Ramp Measurements

We utilized commercially available SiC MOSFETs from four different vendors and applied bidirectional gate voltage ramps with varying maximum voltage values, as illustrated in Fig. 2, where the ramp order is indicated by the legend. All measurements were performed at room temperature. The onset of gate leakage with positive gate voltage ramp was significantly higher for Vendor C. Assuming that this is due to higher gate oxide thickness and desiring to have similar oxide electric fields for all vendors, we extended the voltage ramps for vendors C by 5 V.

We started by ramping up and down to a positive maximum gate voltage twice. The figure shows that the FN-current for positive gate bias is stable for all devices. The leakage current for all subsequent voltage ramps with negative gate bias shows clear reduction of current for each further gate bias ramp.

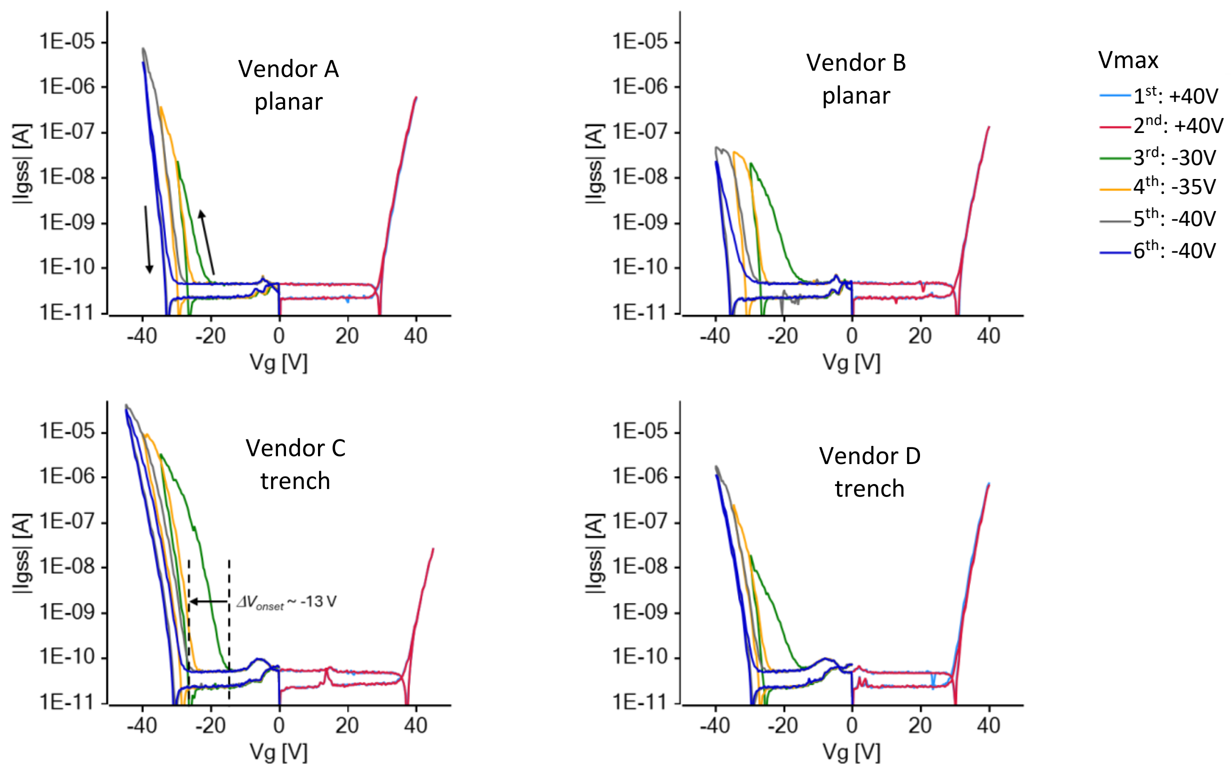

Fig. 2. Absolute value of gate leakage current during different subsequent voltage ramps measured on devices from 4 different vendors. Note that for vendor C, we used 5 V higher values for the maximum gate voltage.

The gate leakage current under negative bias appears to converge to a curve similar to the forward Fowler-Nordheim (FN) curve, but with opposite polarity, as negative voltage stress continues. We therefore propose that the gate leakage current under negative bias is an FN current characterized by an initially low barrier or a high local electric field at the barrier. Continued negative gate voltage stress shifts the onset of the current to significantly lower voltages, either by increasing the barrier or reducing the local electric field. Before and after each gate voltage ramp, we measured the threshold voltage, as shown in Fig. 3. The change in threshold voltage was significantly smaller than the shift in the onset of gate leakage. Compare for example, the shift in gate leakage onset ΔV_{onset} for the device from Vendor C of about -13 V in Fig 2 with the change in threshold voltage of <50 mV, as shown in Fig. 3. This indicates that the charging or discharging of near-interface traps in the channel region cannot account for the shift in the onset of gate leakage at negative bias.

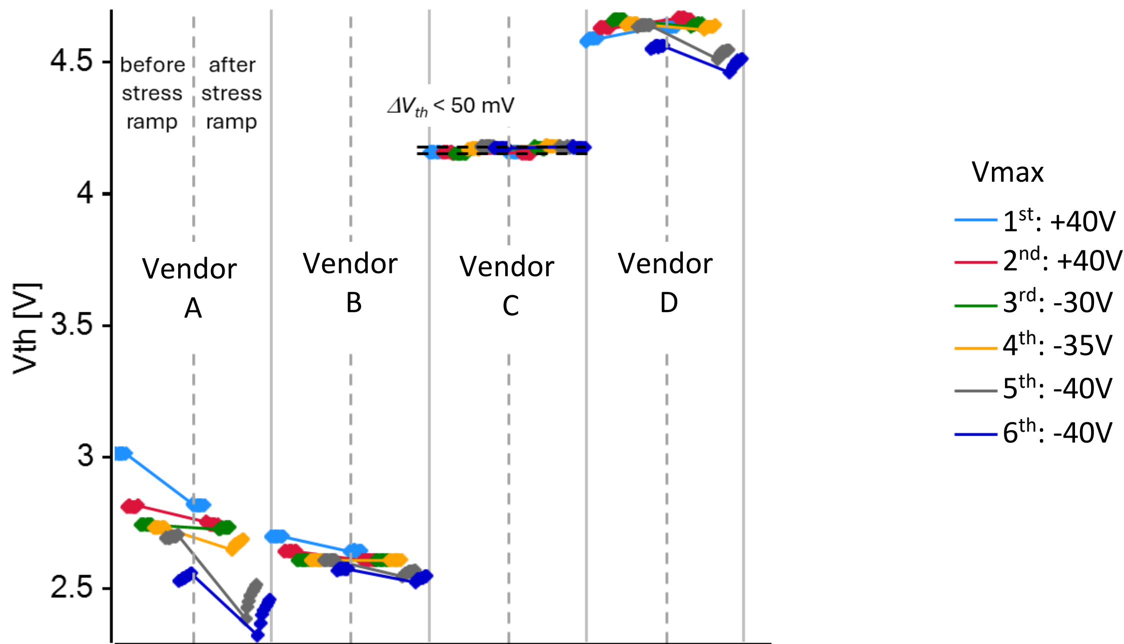

Fig. 3. Threshold voltage before and after each voltage ramp shown in Fig. 2.

Gate Leakage of a Planar MOSCAP on an n$^+$-Doped SiC Epilayer

To test if hole current causes leakage at moderate negative bias, we measured the leakage current in an n$^+$-doped SiC MOSCAP. The gate oxide thickness was 80 nm, and the substrate contained a uniform doping profile with a depth of 200 nm and an aluminum doping concentration of 8×10^{18} cm^{-3}. We ramped the voltage of the top electrode from 0 V to +70 V to -50V to 0 V and observed similar gate leakage behavior to that in commercial SiC MOSFETs, as shown in Fig. 4. We see an onset of gate leakage beyond -25 V and corresponding hysteresis, while at positive bias, we do not see significant hysteresis. At moderate negative gate bias in the range of this onset, we do not expect significant hole current from the n$^+$-doped silicon carbide, as we do not expect inversion. Without hole current we can rule out the hypothesis from literature described above.

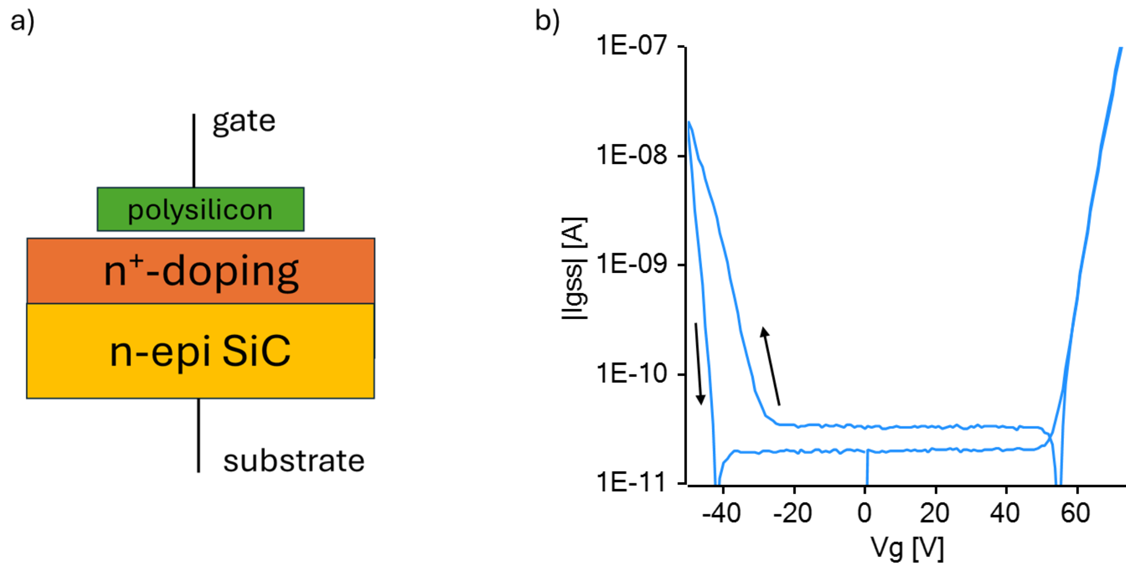

Fig. 4. Gate leakage of a planar MOSCAP on an n+-doped SiC epilayer. a) Schematic cross section of the device. b) Absolute value of gate leakage current during a voltage ramp from 0 V to +70 V to -50 V and back to 0 V.

Gate Leakage of a MOSFET with Either the Source or the Drain Terminal Floating

We measured the leakage current at negative gate bias for a device from Vendor A with either the source electrode or the drain electrode floating, as shown in Fig. 5b, demonstrating that the leakage current does not originate from the drain.

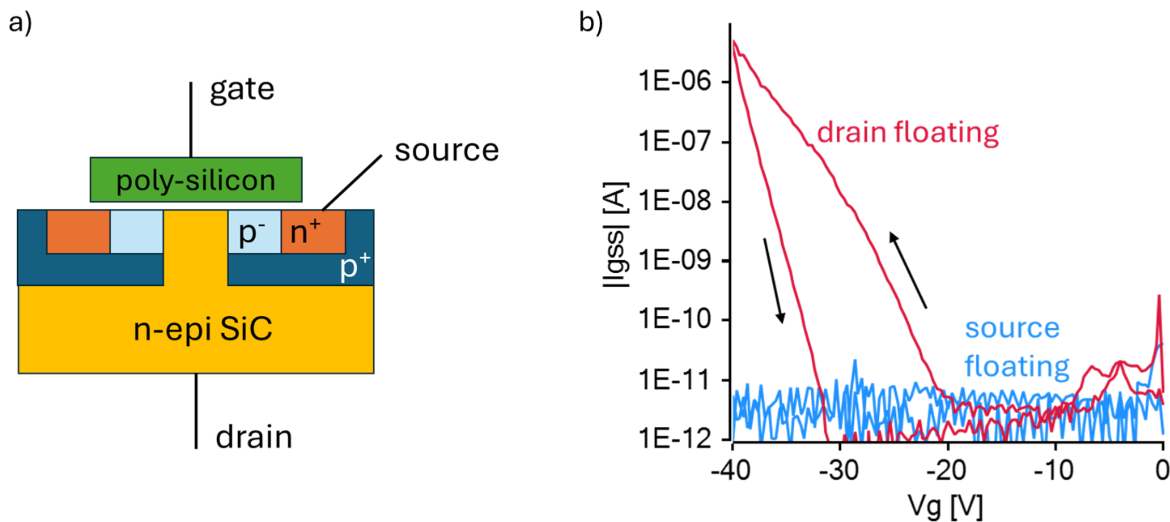

Fig. 5. Gate leakage of a MOSFET with either the source or the drain terminal floating. a) schematic cross section of the device. b) Absolute value of gate leakage current during a voltage ramp from 0 V to -40 V and back to 0 V of a device from vendor A with either drain or source electrode floating.

Analytical Calculation of the Field Enhancement Factor at the Poly-Silicon Corner

Fig. 6a, shows calculated equipotential lines for a square edge close to an infinite surface. By associating the infinite surface with the SiC/SiO_2-interface and one of the equipotential lines with the edge of the poly-silicon gate electrode, we estimate the field enhancement at a rounded corner of a SiC MOSFET gate electrode. The electric field was calculated using conformal mapping with a complex function

$$f(z) = f(x + iy) = u + iv. \quad (1)$$

We use the Schwarz-Christoffel Transformation,

$$f(z) = \sqrt{e^z + 1} + \frac{1}{2}\log\left[\frac{\sqrt{e^z + 1} - 1}{\sqrt{e^z + 1} + 1}\right] \tag{2}$$

adapted from [5], to map the equipotential lines of the electric field of an infinite parallel plate capacitor in two dimensions to a similar capacitor that has a 90° bend in the top plate away from the bottom plate, as depicted in Fig. 6a by the black line inside the superimposed poly-silicon area.

The field line roughly corresponding to the minimum radius of curvature of all the equipotential lines, is indicated in the figure by the line exiting from the poly-silicon corner. We calculated the radius of curvature of this field line by the following formula.

$$R = \left| \frac{\left(1 + \left(\frac{dv}{du}\right)^2\right)^{\frac{3}{2}}}{\frac{d^2v}{du^2}} \right| \tag{3}$$

Fig. 6b displays the radius of curvature of the field line from Fig. 6a versus the field enhancement factor, defined as the field at the corner relative to the field between parallel plates far from the corner. Note that at large radii of curvature, the field enhancement factor decreases below 1 due to the increased distance between the corner and the plane compared to the region distant from the corner.

Based on the presented data, we propose the following hypothesis: With a corner radius of approximately 3 nm, the onset of FN current is expected to occur roughly twice as early as in the case of parallel plates. Typical polysilicon etching or reoxidation processes can cause corner radii well below 10 nm, which aligns with our simplified model explaining the early onset. Although some manufacturers seem to use polysilicon reoxidation to increase the distance between the SiC-interface and the poly-silicon corner by up to 50%, a corner radius well below 10 nm would still cause significant gate leakage as indicated by the steep slope of the field enhancement factor below 10 nm radius shown in Fig. 6b.

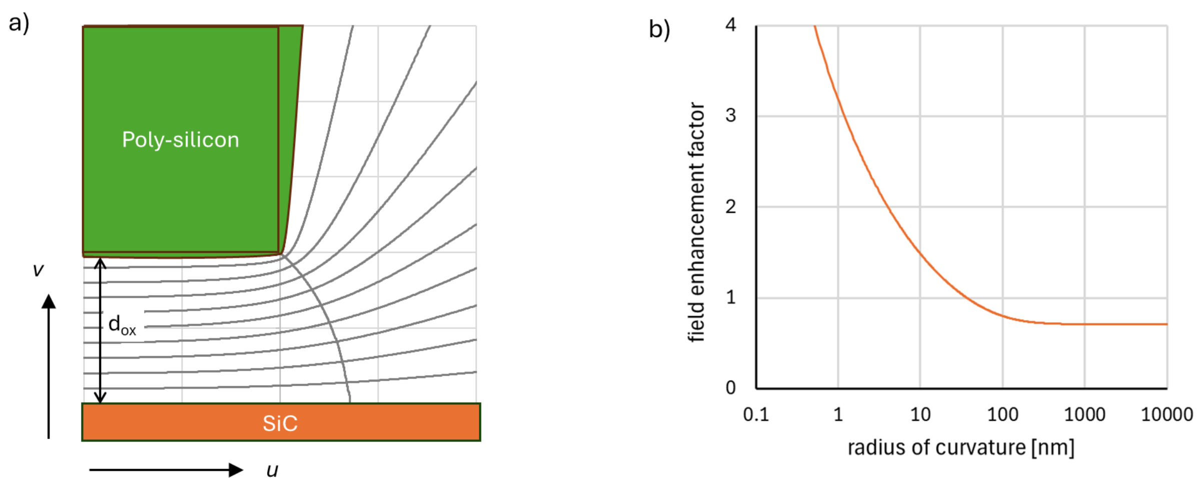

Fig. 6. a) Edge of poly-silicon electrode in a planar SiC-MOSFET superimposed with calculated equipotential lines using conformal mapping with the Schwarz-Christoffel Transformation. b) Calculated field enhancement factor at the corner of the poly-silicon against the radius of curvature.

Oxide Damage at the Edge of the Polysilicon Electrode

Etching polysilicon to define the extent of the electrode might cause damage to the oxide surface not masked by the polysilicon [6]. Oxide damage at the corner of the polysilicon might lower the barrier for electron emission from the gate electrode and thus explain the leakage current at negative gate bias, possibly in combination with geometric field enhancement.

Leakage Current Reduction with Prolonged Gate Bias Stress

Due to the anticipated high electron current density at the poly-silicon corners, we also assume that local electron trapping is significantly enhanced, leading to a reduction of the electric field at the corners and consequently a decrease in FN current with continued electron current stress. The leakage current is therefore self-limiting. The trapping rate might also be enhanced due to the oxide damage at the edge of the polysilicon as explained in the previous section.

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