Key Engineering Materials
ISSN: 1662-9795, Vol. 1057, pp 95-101
doi:10.4028/p-4rcL7P
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Submitted: 2025-09-26
Revised: 2025-12-20
Accepted: 2026-03-08
Online: 2026-05-21

Body Diode Performance of the 4H-SiC 3.3 kV Semi-SJ MOSFET

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Keywords: superjunction, semi-superjunction, planar MOSFET, body diode, reverse recovery.

Abstract. This study investigates static and dynamic behavior of a 3.3 kV semi-Superjunction (SJ) MOSFET, compared with a conventional planar MOSFET. The semi-SJ was designed using a cost-effective trench side-wall implantation and SiO_2 refill fabrication method and evaluated through TCAD simulations. The optimized semi-SJ MOSFET designs, reduces R_{ON} by 19% and increases BV by 500 V compared with the planar MOSFET, while maintaining a comparable reverse recovery charge (Q_{RR}). The proposed semi-SJ design demonstrated the best $R_{ON}\times Q_{RR}$ figure of merit (17.8 mΩ·μC), outperforming the conventional planar MOSFET design (19.7 mΩ·μC).

Introduction

The 4H-SiC MOSFETs are widely adopted in industrial and automotive applications due to their superior efficiency and performance compared with Si IGBTs [1]. In the 3.3 kV voltage class, further improvements in device performance can be achieved through Superjunction (SJ) technology, which lowers on-state resistance (R_{ON}) while enabling higher breakdown voltage (BV) [2]. However, the introduction of alternating n- and p-pillars increases output capacitance [3-5], make it essential to assess SJ devices not only in terms of static performance but also dynamic behaviour such as reverse recovery.

In inverter and converter systems, the intrinsic body diode of the MOSFET can replace an external freewheeling diode, offering system-level cost benefits [6,7]. A drawback, however, is that third-quadrant operation of the body diode may induce bipolar degradation, such as stacking fault expansion driven by electron–hole recombination [8]. While recent advances in 1.2 kV and 3.3 kV devices have helped mitigate this concern [6], reverse recovery remains an important performance factor. Schottky diodes have been shown to suppress reverse recovery effectively, with reductions in turn-on losses of up to 45% reported for the 3.3 kV class [7], but this improvement comes at the expense of an additional device component. Moreover, experimental studies on trench MOSFETs with full and semi-SJ structures, fabricated through multi-epitaxy and p-implantation, indicate that SJ concepts can increase reverse recovery charge (Q_{RR}) compared to conventional non-SJ devices [4,5].

This work investigates the body diode and reverse recovery behavior of a 3.3 kV semi-SJ MOSFET compared with a conventional planar MOSFET using TCAD. The proposed device is designed using a cost-effective trench etching and side-wall implantation method, without requiring multiple epitaxy steps and with only two additional implantation schedules compared with the planar process [2,9].

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Design Description

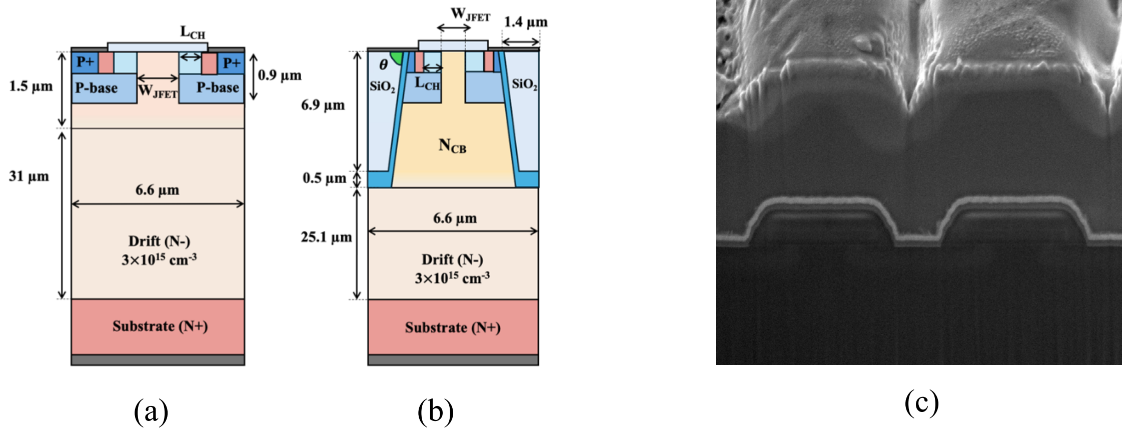

Fig. 1. Schematic of the (a) planar and (b) semi-SJ designs; (c) SEM image of the fabricated planar MOSFET active area.

The proposed semi-SJ design (Fig.1 (b)) is based on the fabricated 3.3 kV planar MOSFET, with dimensions and SEM of the active area shown in Fig. 1 (a) and (c). The planar MOSFET features a 32.5 µm epitaxial layer doped at 3×10^{15} cm^{-3} and a simulated 1.5 µm JFET region at 8×10^{15} cm^{-3}. All structures feature a 6.6 µm cell pitch, 50 nm gate-oxide, and 0.7 µm channel length (L_{CH}). The JFET width (W_{JFET}) is 1.8 µm in the planar device and adjusted to 1.4 µm in both semi-SJ designs. Additionally, the deep trench opening and depth are 2.8 µm and 6.9 µm, incorporating 0.25 µm sidewall and 0.5 µm bottom p-implants. The trench dimensions are based on the process developed in [9] with the tilt angle (θ) of 6°. The semi-SJ also includes an n-type charge-balance layer (N_{CB}), varied between 2×10^{16} cm^{-3} and 3×10^{16} cm^{-3} as an optimization parameter.

On-State and Off-State Performance

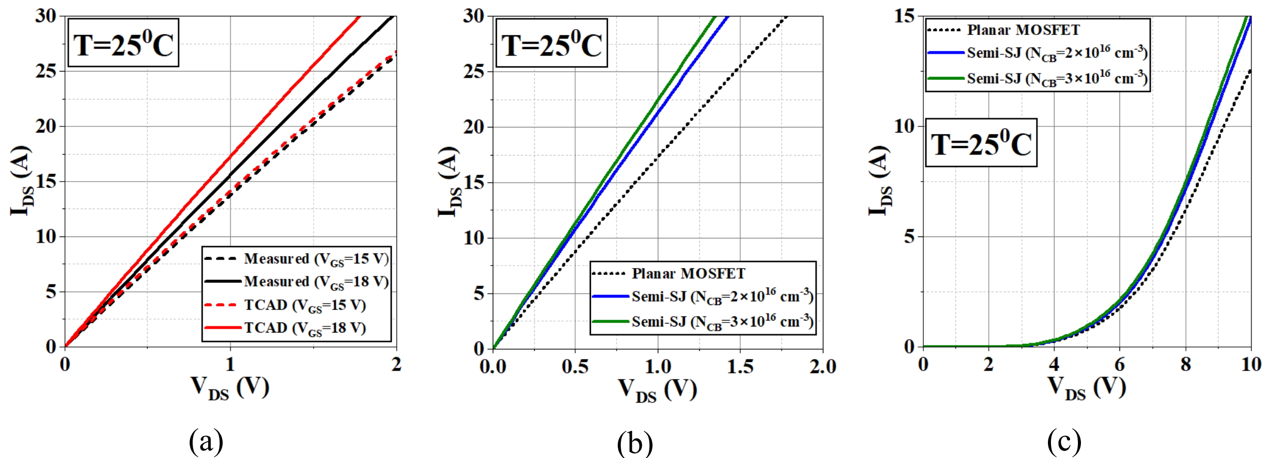

Fig. 2. (a) Measured and simulated on-state characteristics of the conventional planar MOSFET; simulated planar and semi-SJ MOSFET: (b) on-state comparison and (c) transfer comparison.

The room-temperature on-state characteristics of the conventional 3.3 kV planar MOSFET are shown in Fig. 2 (a) for VGS = 18 V and 15 V, with the simulated TCAD results. The conventional planar device achieves R_{ON} of 64 mΩ (measured) and 57 mΩ (simulated). Compared to the simulated planar MOSFET, the semi-SJ designs achieve R_{ON} of 46 mΩ (-19 %) and 44 mΩ (- 23 %) for N_{CB}=2×10^{16} cm^{-3} and 3×10^{16} cm^{-3}, respectively, as shown in Fig. 2 (b). All simulated designs were calibrated to a

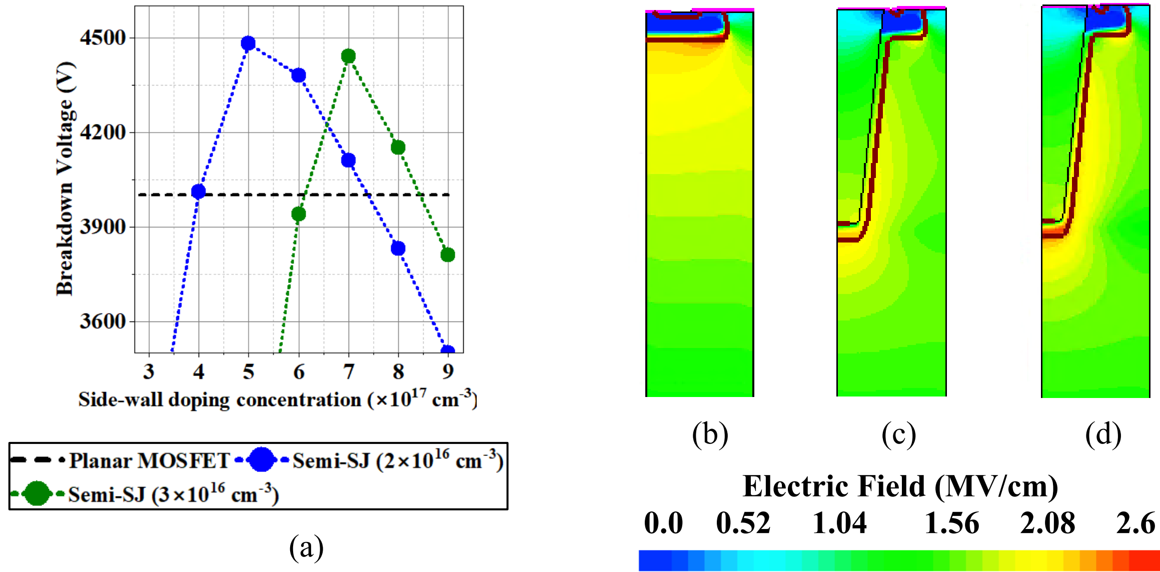

Fig. 3. (a) Side-wall p-type doping concentration versus BV; EF distribution at 3.3 kV: (b) planar, (c) semi-SJ (N_{CB}=2×10^{16} cm^{-3}, 5×10^{17} cm^{-3} side-wall), (d) semi-SJ (N_{CB}=3×10^{16} cm^{-3}, 7×10^{17} cm^{-3} side-wall).

measured threshold voltage (V_{TH}) of 3 V at 9 mA, with transfer characteristics shown in Fig. 2 (c).
The side-wall implantation doping concentration as a function of breakdown voltage (BV) for the semi-SJ designs is shown in Fig. 3 (a). The simulated off-state performance of the conventional planar MOSFET is 4 kV, which is denoted as the dashed line in Fig. 3 (a). In comparison, the semi-SJ design with the N_{CB}=2×10^{16} cm^{-3} achieves BV of 4.5 kV when the side-wall doping concentration is 5×10^{17} cm^{-3}, while the design with N_{CB}=3×10^{16} cm^{-3} achieves BV of 4.4 kV when the side-wall doping concentration is 7×10^{17} cm^{-3}. Additionally, the semi-SJ MOSFET with N_{CB}=2×10^{16}cm^{-3} maintains BV above 4 kV over a wider implantation range (4×10^{17}– 7×10^{17} cm^{-3}), while the N_{CB}=3×10^{16} cm^{-3} design has a slightly narrower implantation window (6×10^{17}– 8×10^{17} cm^{-3}).
The electric field (EF) distributions of planar and semi-SJ designs are shown in Fig. 3(b)–(d). The trench angle required for side-wall implantation in semi-SJ designs introduces a charge imbalance above and below the trench midpoint [2,10]. Therefore, as illustrated in Fig. 3 (c) and (d), the n-type layer becomes charge overcompensated below the trench midpoint, shifting the maximum EF toward the trench-bottom p-type implant, with the effect becoming stronger at higher n-top doping concentrations (N_{CB}=3×10^{16} cm^{-3}).

Third-Quadrant Performance

The measured reverse conduction of the fabricated 3.3 kV planar MOSFET is shown in Fig. 4 (a) for V_{GS} values between –5 V and 0 V. As reported in [1,11], third-quadrant conduction below V_{TH} is a combination of the MOS channel, the body diode, and the parasitic BJT current components. At V_{DS} = –3 V and V_{GS} = 0 V, the lower conduction voltage drop indicates that current is primarily unipolar, enabled by the body effect and positive fixed charge (Q_F) at the SiC/SiO_2 interface. This is confirmed by the current distribution in Fig. 4 (b) and (d) simulated with the Q_F =7×10^{11} cm^{-2}, which shows high electron density conduction through the channel. At V_{DS} = –3 V and V_{GS} = –5 V, the simulated electron and hole distribution in Fig. 4 (c) and (e) shows that electron current through the parasitic npn BJT dominates, while a smaller hole component is injected at the body diode junction to provide the base drive (see Fig. 4 (c)) [11].
The simulated reverse conduction at V_{GS} = 0 V and –5 V for the semi-SJ structures, compared with the planar benchmark, are shown in Fig. 5 (a) and (b). At V_{GS} = –5 V, the semi-SJ device exhibits

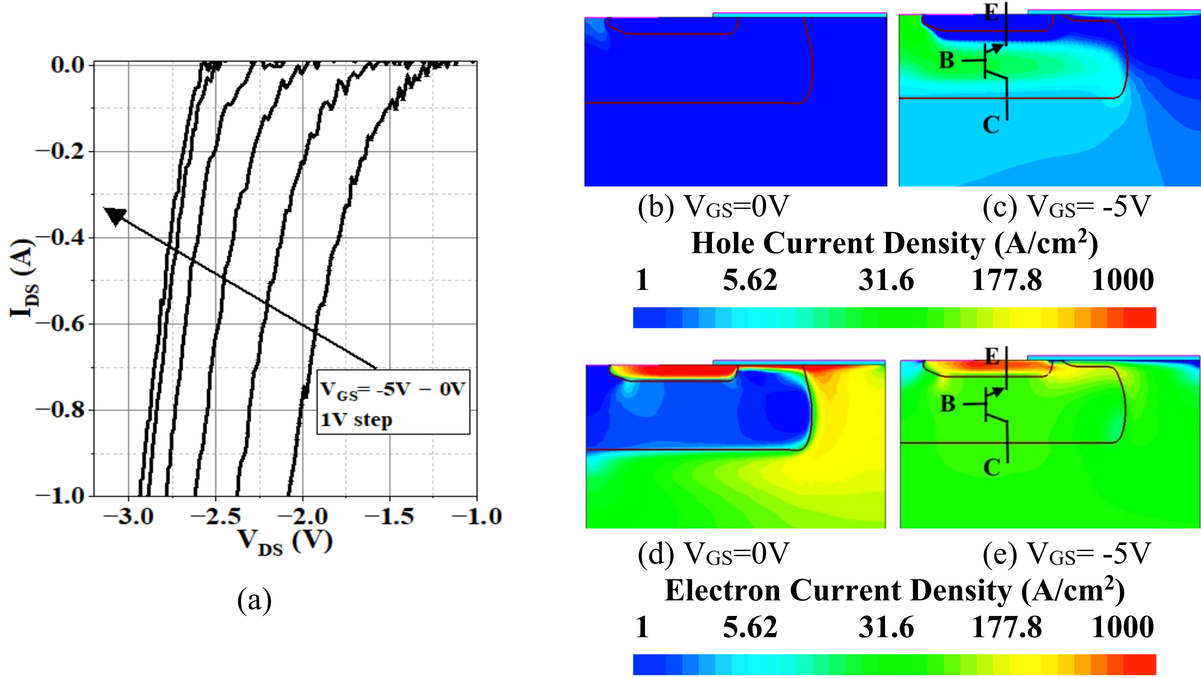

Fig. 4. (a) Measured body diode reverse conduction characteristics; hole current density (V_{DS}=-3V): (b) V_{GS}=-5V and (c) V_{GS}=0V; electron current density (V_{DS}=-3V): (d) V_{GS}=-5V and (e) V_{GS}=0V.

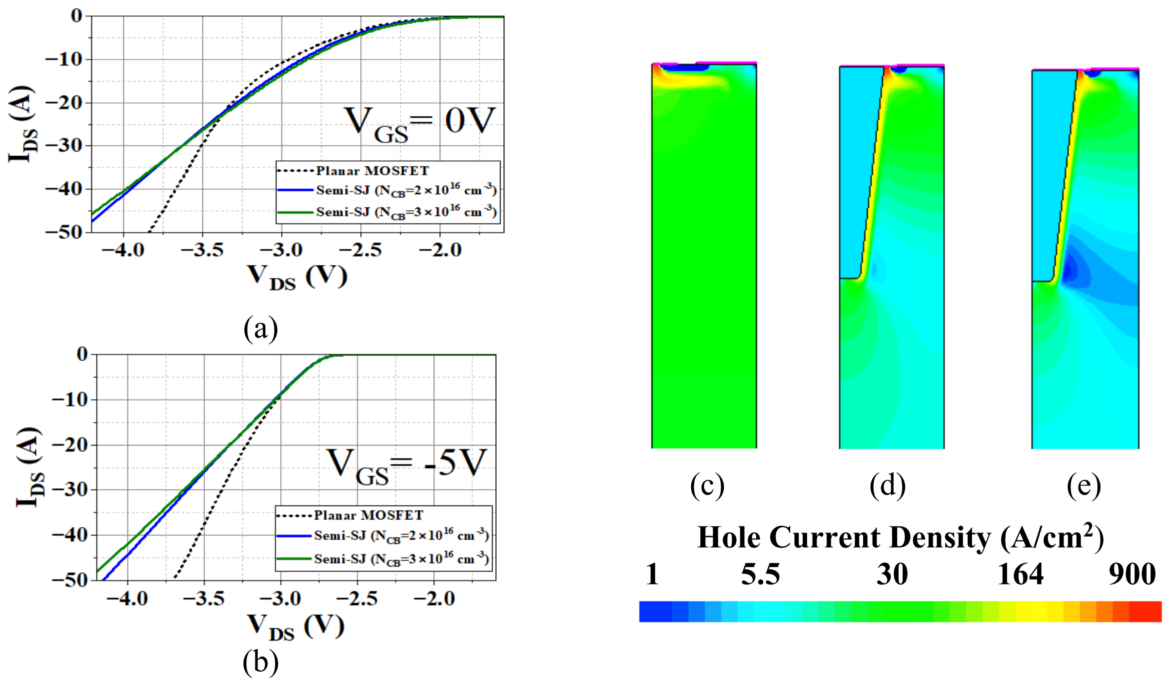

Fig. 5. Simulated third-quadrant characteristics at V_{GS}: (a) 0V, (b) -5V; Hole density distribution at V_{DS}= - 4V and V_{GS}= - 5V: (c) planar, (d) semi-SJ (N_{CB}=2×10^{16} cm^{-3}), (e) semi-SJ (N_{CB}=3×10^{16} cm^{-3}).

the highest forward voltage (V_F) drop, reaching 4.3 V at 50 A, compared with 3.7 V for the planar device. A similar trend is observed at higher current densities when V_{GS} = 0 V. The reduced conductivity modulation in the semi-SJ design is confirmed by the simulated hole current density distributions in Fig. 5 (c–e), where significantly fewer holes are injected into the drift region compared to the planar MOSFET. Reducing the N_{CB} to 2×10^{16} cm^{-3} improves reverse conduction, lowering the V_F to 4.1 V at 50 A and potentially improved reverse recovery performance.

Body Diode Reverse Recovery Performance

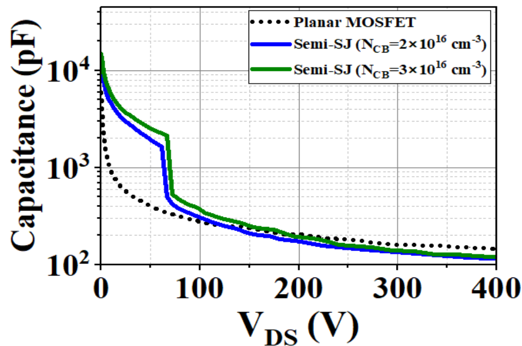

Fig. 6. Simulated output capacitance (C_{OSS}) of planar, semi-SJ and full-SJ designs.

To evaluate the dynamic performance of the investigated devices, the output capacitance (C_{OSS}) was simulated, as shown in Fig. 6. At V_{DS} = 400 V, all investigated devices exhibit a similar C_{OSS} of approximately 120 pF. At lower voltages, the semi-SJ devices exhibit higher capacitance due to the presence of a deep p–n junction formed by the side-wall p-pillars and the n-type charge-balance region. At V_{DS} = 50 V, the C_{OSS} reaches 2550 pF and 1900 pF for N_{CB} = 2×10^{16} cm^{-3} and 3×10^{16} cm^{-3}, respectively, compared with 400 pF for the planar MOSFET. As V_{DS} increases, the C_{OSS} of the semi-SJ devices start to sharply decrease at approximately 65 V as the depletion region expands, which will directly affect the switching and reverse-recovery behavior.

The body diode performance was simulated using a double-pulse test at 1.7 kV and the load inductance of 68 µH, with results shown in Fig. 7 (a) and (b). Note, that parasitic source and drain inductances were set as 5 nH and 10 nH, respectively. The high-side switch was biased at V_{GS}= –5V and the gate resistance of the low-side switch (R_G) was set to 15 Ω and 5 Ω. The simulated diode forward current (I_F) was fixed at 27 A.

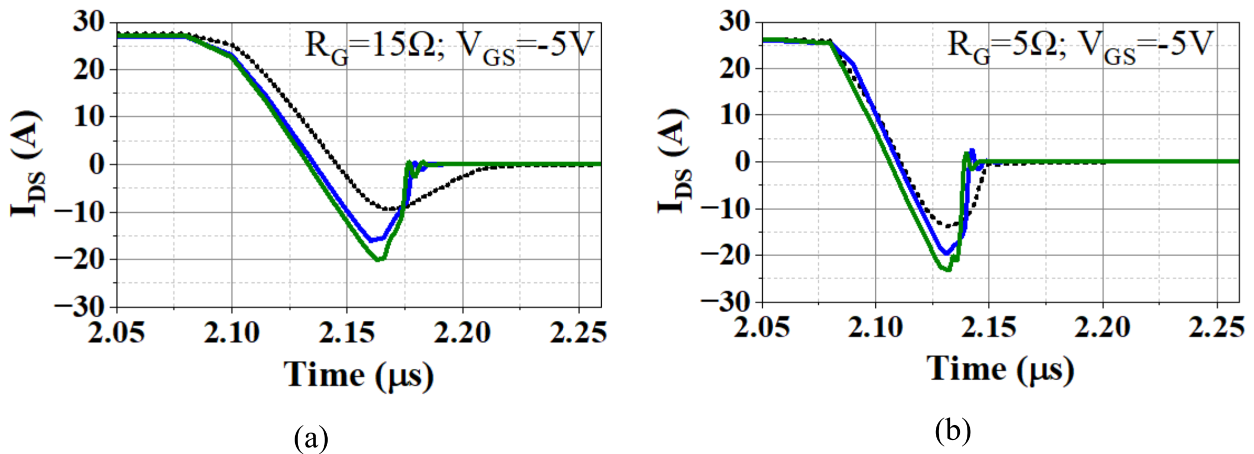

Fig. 7. Simulated planar and semi-SJ MOSFET reverse recovery current at: (a) R_G=15 Ω, V_{GS}=-5V and (b) R_G=5 Ω, V_{GS}=-5V.

Table 1. Reverse recovery characteristic of planar and semi-SJ designs.

Parameter:	Planar		Semi-SJ (N_{CB}=2×10^{16} cm^{-3})		Semi-SJ (N_{CB}=3×10^{16} cm^{-3})	
	R_G=15Ω	R_G=5Ω	R_G=15Ω	R_G=5Ω	R_G=15Ω	R_G=5Ω
t_{RR} (ns)	63	37.3	42	31.4	42	32.7
Q_{RR} (nC)	357	346	417	386	507	463
I_{RRM} (A)	9.6	13.8	16.1	19.6	20.2	23.3
dI_{RR}/dt (kA/µs)	0.25	1.1	1.1	2.6	1.8	3.5
E_{SW} (µJ)	512	437	577	523	730	648

The summary and comparison of switching characteristics can be seen in Table 1, where the Semi-SJ shows a comparable reverse recovery charge (Q_{RR}) compared to a conventional planar MOSFET. For R_G=5Ω, the planar device results in the Q_{RR} of 346 nC, while the semi-SJ with the N_{CB} = 2×10^{16} cm^{-3} shows the Q_{RR} of 386 nC, corresponding to a 10 % increase. Increasing the N_{CB} concentration to 3×10^{16} cm^{-3} in the Semi-SJ structure leads to a 30% increase in Q_{RR} (463 nC) compared to the planar device.
Additionally, the semi-SJ designs show higher peak reverse current and steeper dI_{RR}/dt during recovery, due to increased stored charge and capacitance. These results are consistent with previous reports on SiC SJ MOSFETs [4,5], where the increased pn-junction area increases C_{OSS} (see Fig. 6) and increases the reverse recovery losses.
Based on the $R_{ON}\times Q_{RR}$ figure of merit with R_G=5Ω switching results, the semi-SJ with N_{CB}=2×10^{16} cm^{-3} offers a balanced trade-off (17.8 mΩ·µC), outperforming the planar MOSFET design (19.7 mΩ·µC) and offering lower fabrication cost compared to other SJ technologies. The comparison between static and dynamic performance of all investigated devices is summarized in Table 2.

Table 2. Static and dynamic performance comparison between conventional and semi-SJ designs.

Parameter:	**Planar**	**Semi-SJ (N_{CB}=2×10^{16} cm^{-3})**	**Semi-SJ (N_{CB}=3×10^{16} cm^{-3})**
R_{ON} (mΩ)	57	46 [- 19 %]	44 [- 23 %]
BV (kV)	4	4.5 [+ 12.5 %]	4.4 [+ 10 %]
Implantation window (cm^{-3})	-	$4\text{-}7\times10^{17}$	$6\text{-}8\times10^{17}$
$R_{ON}\times Q_{RR}$ (mΩ.µC)	19.7	17.8	20.3

Conclusion

This work investigated the third-quadrant conduction and reverse recovery behavior of a 3.3 kV semi-SJ design, with static characteristics benchmarked against a fabricated planar MOSFET. The optimized semi-SJ device achieved a balanced trade-off between conduction and switching performance. With an n-top (N_{CB}) doping concentration of 2×10^{16} cm^{-3}, the optimized semi-SJ reduced R_{ON} by 19% and increased the maximum BV by 500 V compared with the planar MOSFET. This design also achieved the best $R_{ON}\times Q_{RR}$ figure of merit at 17.8 mΩ·µC, outperforming the planar device with the $R_{ON}\times Q_{RR}$ of 19.7 mΩ·µC. These results demonstrate that semi-SJ devices, designed with a cost-effective side-wall implantation fabrication method, provide a promising solution for high-voltage SiC MOSFETs with competitive static and body diode reverse recovery characteristics.

References

[1] R. Zhang *et al.*, "Third Quadrant Conduction Loss of 1.2–10 kV SiC MOSFETs: Impact of Gate Bias Control," in *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 2033-2043, Feb. 2021.

[2] M. Boccarossa *et al.*, “A 3.3 kV SiC Semi-Superjunction MOSFET with Trench Sidewall Implantations,” *Micromachines*, vol. 16, no. 2, p. 188, 2025.

[3] G. W. C. Baker *et al.*, "Optimization of 1700-V 4H-SiC Semi-Superjunction Schottky Rectifiers With Implanted P-Pillars for Practical Realization," in *IEEE Transactions on Electron Devices*, vol. 69, no. 4, pp. 1924-1930, April 2022.

[4] S. Harada *et al*., "First Demonstration of Dynamic Characteristics for SiC Superjunction MOSFET Realized using Multi-epitaxial Growth Method," *2018 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2018, pp. 8.2.1-8.2.4.

[5] M. Baba *et al*., "Ultra-Low Specific on-Resistance Achieved in 3.3 kV-Class SiC Superjunction MOSFET," *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Nagoya, Japan, 2021, pp. 83-86.

[6] J. Qian *et al*., "An investigation of body diode reliability in commercial 1.2 kV SiC power MOSFETs with planar and trench structures," *Micromachines*, vol. 15, no. 2, p. 177, 2024.

[7] M. A. Karout *et al*., "Impact of Diode Technology on the Switching Performance of 3.3 kV SiC MOSFETs," *2024 36th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Bremen, Germany, 2024, pp. 108-111.

[8] W. Cao *et al*., "SiC superjunction MOSFET with Schottky diode for improving short-circuit and reverse recovery ruggedness," *Micro and Nanostructures*, vol. 191, p. 207847, 2024.

[9] Q. Z. Cao *et al.,* "Device fabrication of SiC superjunction trench MOSFETs with Schottky diode using ICP and RIE processes," *Materials Science Forum*, vol. 1159, pp. 21–29, Sep. 2025.

[10] K. Melnyk *et al*., "3.3 kV 4H-SiC Trench Semi-Superjunction Schottky Diode With Improved ON-State Resistance," in *IEEE Transactions on Electron Devices*, vol. 71, no. 9, pp. 5573-5580, Sept. 2024.

[11] Y. Chen *et al*., "Novel Cell-Level Insights into Third Quadrant Current Paths of Power SiC MOSFET," *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, USA, 2024, pp. 6754-6758.