

## Capture/Emission Processes of Carriers in Heterointerface Traps Observed in the Transient Charge-Pumping Characteristics of SiGe/Si-Hetero-Channel pMOSFETs

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**Abstract.** Transient phenomena related to carrier capture/emission processes in interface traps were observed in the the charge pumping (CP) characteristics of SiGe/Si hetero-channel pMOSFETs, i.e., the CP characteristics were found to depend on the on/off time of the gate pulse. From these observations, time constants for the processes both in SiGe/Si heterointerface traps and in gate-oxide interface traps were derived. The time constant is considered to depend on the energy level of the interface traps that are present over a wide range within the energy gap. Therefore, these phenomena provide an interesting way of evaluating the discrete energy levels of interface traps in nanometer-scale devices containing only a few traps.

### Introduction

Strained-Si and SiGe/Si hetero-CMOS structures are highly promising materials for the construction of advanced high performance Si CMOS devices [1, 2]. To exploit the advantages of SiGe/Si heterostructure effectively and to establish adequate device reliability, an understanding of the electrical properties of the hetero-interface, i.e., heterointerface traps, is an important factor.

On the other hand, as the dimensions of MOSFETs are scaled into the nanometer regime, fluctuations in device characteristics due to variations in gate length, discrete dopant fluctuations, line-edge roughness, and so on have become serious problems [3-5]. Moreover, the presence of current noise in MOSFETs has recently become a problem even in digital circuits [6]. The 1/f noise is the dominant type of noise in silicon MOSFETs, and is considered to be determined by the electronic properties at and near the gate-oxide interface. Discrete drain current fluctuations, known as random telegraph noise (RTN), are observed in MOSFETs under constant bias conditions and are considered to be caused by charge-transport fluctuations due to the capture/emission of carriers at single traps. It has been pointed out that RTN will become one of the greatest reliability issues in

scaled-down digital devices [6-11].

Therefore, the identification of traps that exist in the vicinity of the heterointerface and the gate-oxide interface will be essential for the development of future small MOS devices.

In this paper, we describe transient phenomena that have been observed in the dependence of the charge pumping characteristics upon the on/off time of the gate pulse in SiGe/Si hetero-channel pMOSFETs. These are related to the carrier capture/emission processes in SiGe/Si heterointerface traps and/or the gate-oxide interface traps, and a time constant for the process will be derived from the transient characteristics.

## Experiments

A schematic of the cross section of the SiGe/Si hetero-p-channel MOSFETs (pMOSFETs) used in this study is shown in Fig. 1. These devices were fabricated using a high-quality low-temperature epitaxially grown heterostructure incorporating a Si buffer layer, a strained SiGe layer and a Si capping layer. The heterostructure was grown in an ultraclean low-pressure chemical vapour deposition (CVD) system [12]. The deposition temperature was 750 °C for the Si buffer layer (100 nm thick), 500 °C for the strained SiGe layer (7 nm thick), and 500 °C for the Si capping layer (10 nm thick). The Ge fraction in the SiGe layer was 0.4. This was estimated using X-ray diffractometry by determining the lattice constant of a thicker relaxed SiGe layer deposited under the same deposition conditions. After forming a 700-nm-thick field oxide layer at 400 °C by CVD, a 10 nm gate oxide layer was thermally grown by wet oxidation at 700 °C. Thus, the final thickness of the Si capping layer was 6 nm. An in-situ phosphorous-doped  $n^+$  polysilicon layer was deposited and patterned to form the gate, and the source and drain were formed by  $B^+$  ion implantation ( $1.2 \times 10^{15} \text{ cm}^{-2}$  at 25 keV). The gate length and width of the MOSFETs were 1.5 and 4  $\mu\text{m}$ , respectively. After the interconnection processes, a final forming gas annealing was performed at 400 °C. All of the annealing processes were performed at temperatures below 700 °C to prevent degradation of both the flatness of the heterostructure surface and the Ge profile in the channel region.

Typical electrical characteristics of the SiGe/Si hetero-pMOSFET used in this study are shown in Fig. 2.

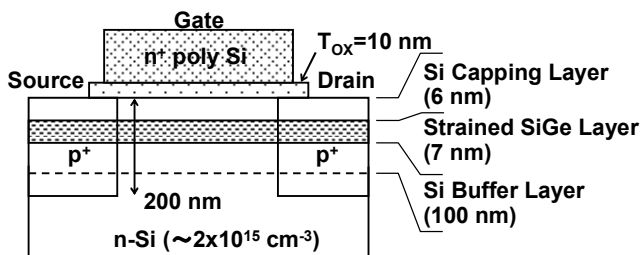


Fig. 1 SiGe/Si-hetero-channel pMOSFET used in this study.

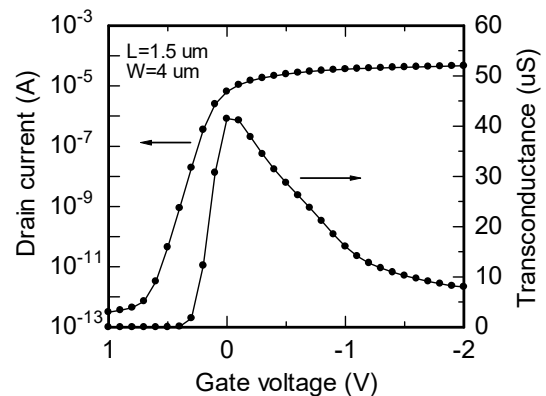


Fig. 2 Typical drain current and transconductance as a function of gate voltage in the SiGe/Si-hetero-channel pMOSFETs.

Charge pumping (CP) measurements [13] were performed using a gate pulse of fixed amplitude ( $-3$  V) and a variable base level,  $V_{\text{BASE}}$ , with a pulse frequency of 66~250 kHz, in the temperature range from RT to 91 K. The gate pulse configuration during the CP measurements is shown in Fig. 3.

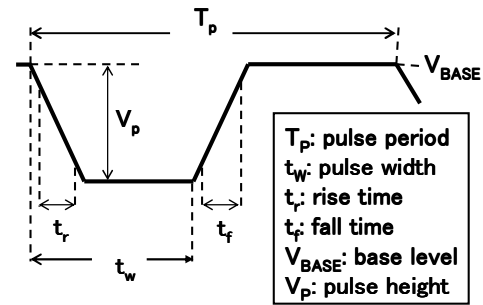


Fig. 3 Gate pulse configuration during charge pumping measurements.

## Results and Discussions

It is well known that the maximum CP current depends upon the rise time ( $t_r$ ) of the gate pulse, even when adequate inversion and accumulation conditions are attained during the measurement, as shown in Fig. 4. This is due to decrease in the emission current from electrons in non-steady-state interface traps in the upper part of the energy band gap moving to the conduction band under the influence of the rapidly rising gate voltage [13].

We observed another transient phenomenon in the rising portion (but not at maximum current) of the CP characteristics at room temperature (RT) [14]. The dependence of the pulse-width ( $t_w$ ), i.e., the on-time of the gate pulse, upon the CP characteristics is shown in Fig. 5. The CP currents ( $I_{\text{CP}}$ ) at a given  $V_{\text{BASE}}$  in the rising portion as a function of on-time are shown in Fig. 6. The current increases with increasing on-time, and shows a saturation behavior that can be described by  $I_{\text{CP}} = I_{\text{CP0}}[1 - \exp(-t/\tau_T)]$  using a time constant  $\tau_T$ , where  $I_{\text{CP0}}$  is a saturated CP current.  $1 - I_{\text{CP}}/I_{\text{CP0}}$  for each value of  $V_{\text{BASE}}$  as a function of on-time is shown in Fig. 7. The time constant ( $\tau_T$ ) for each  $V_{\text{BASE}}$  can be derived from Fig. 7, as indicated in the figure.

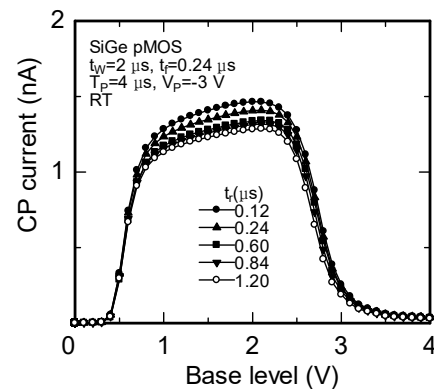


Fig. 4 Dependence of CP characteristics on the rise time of the gate pulse.

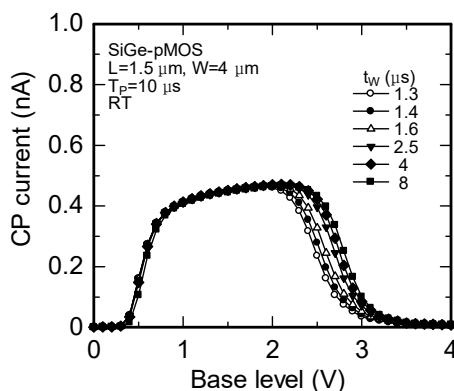


Fig. 5 Dependence of the CP characteristics in the rising portion on the pulse width, i.e., on-time of the gate pulse.

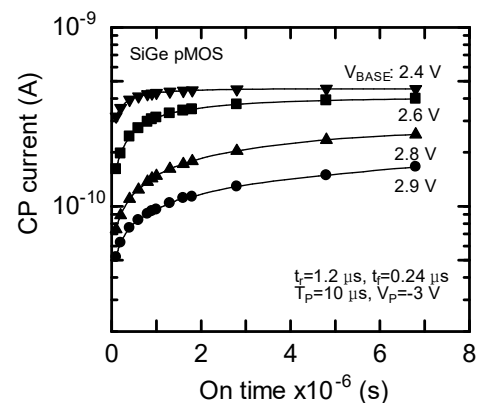


Fig. 6 CP current as a function of on-time for different base levels in the rising portion.

The value of  $\tau_T$  is considered to be related to the capture process of holes from the less strong inversion layer to both the gate-oxide interface traps and the heterointerface traps, as follows: Changes in the energy band diagram during this process are shown in Fig. 8. Holes trapped in the interface traps recombine with electrons coming from the accumulation layer formed while at the base level (i.e., during accumulation) as shown in Fig. 8(a), and some of the holes in the inversion layer are captured by interface traps during the on-time (i.e., during inversion) as shown in Figs. 8(b) and 8(c). However, in this case, inversion is less strong because of the rising portion in the CP characteristics, and only a small fraction of the interface traps can capture holes if the on-time is insufficient, as shown in Fig. 8(b).

We also observed similar transient behavior in the opposite rising portion of the CP characteristics, which depends upon the off-time of the gate pulse. This is considered to be related to the emission of holes from interface traps to the less strong accumulation layer. The time constants related to the emission process ( $\tau_T \sim 1.5\text{--}2\ \mu\text{s}$ ) were derived from the dependences.

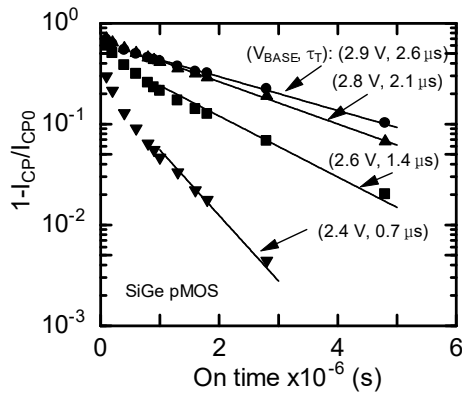


Fig. 7 Time constant of the on-time dependent CP current with base level as a parameter.

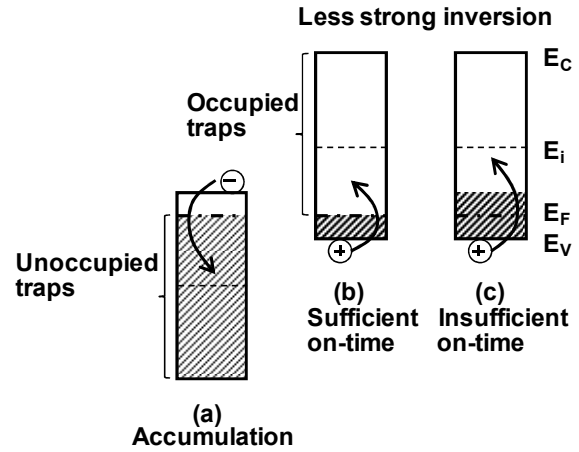


Fig. 8 Energy band diagrams explaining the on-time dependent CP characteristics, indicating capture process of holes from the less strong inversion layer to the heterointerface traps.

Moreover, if we perform low temperature CP measurements [15], the value of  $\tau_T$  for heterointerface traps only should be obtained. The dependence of the pulse-width ( $t_w$ ) upon the CP characteristics at 90 K is shown in Fig. 9. The plateau region seen at around  $V_{\text{BASE}} = 2.5\text{--}3\text{ V}$  in Fig. 9 is the CP current due to the heterointerface traps [15]. Therefore, we can derive the time constant ( $\tau_T$ ) from the change in the CP current in the rising portion of the plateau region. The CP currents at a base level of 3.2 V in the rising portion as a function of on-time at 90 K are shown in Fig. 10. From this figure, we obtained  $\tau_T \sim 1\ \mu\text{s}$ . However, since the number of heterointerface traps is small, the CP current in the rising portion at a base level of around 3.2 V in Fig. 9 is very low. Therefore, the accuracy of the obtained value of  $\tau_T$  may not be very high.

Then, we used hot carriers to generate heterointerface traps [16, 17] and tried to improve the accuracy. The CP characteristics at RT before and after hot carrier stress are shown in Fig. 11. Stress drain and gate voltages were -8 V and -1 V, respectively, and stress time was 20 min. It can be seen

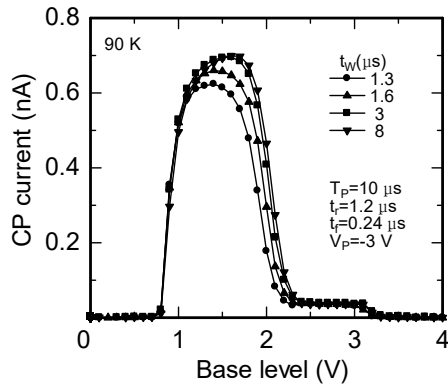


Fig. 9 Dependence of the CP characteristics on the pulse width at 90 K.

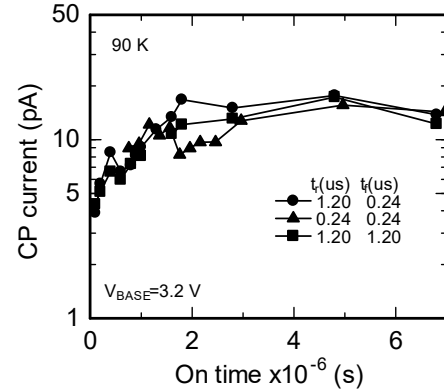


Fig. 10 On-time dependent CP current related to heterointerface traps at 90 K.

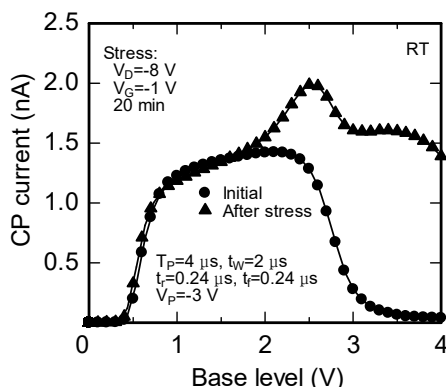


Fig. 11 CP characteristics at RT before and after hot carrier stress.

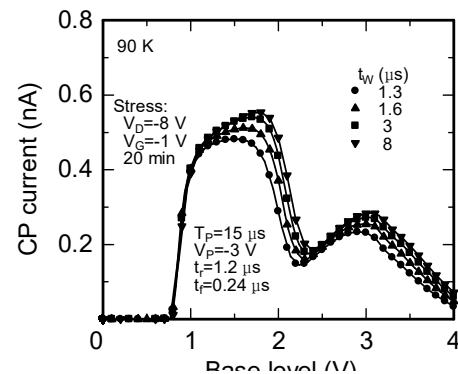


Fig. 12 On-time dependent CP characteristics at 90 K after hot carrier stress.

from the figure that significant numbers of interface traps were generated. The dependence of the pulse-width upon the CP characteristics at 90 K after stress is illustrated in Fig. 12, which shows a marked increase in heterointerface traps.  $1 - I_{CP}/I_{CP0}$  at some values of  $V_{BASE}$  in the rising portion are shown as a function of on-time at 90 K in Fig. 13. The values of  $\tau_T \sim 1.7$ - $2.0$   $\mu s$  are derived from the figure, which is related to the capture process of holes in the heterointerface traps.

## Summary

Transient phenomena related to the carrier capture/emission processes in interface traps were observed in the charge pumping characteristics of SiGe/Si hetero-channel pMOSFETs, i.e., the charge pumping characteristics were found to depend on the on/off time of the gate pulse. From these observations, time constants for the processes both in the SiGe/Si hetero-interface traps and in the gate-oxide interface traps were derived. The time constant is considered to depend on the energy level of the interface traps that are present over a wide range within the energy band gap. Therefore, this method provides an interesting way by which to evaluate the discrete energy levels of interface

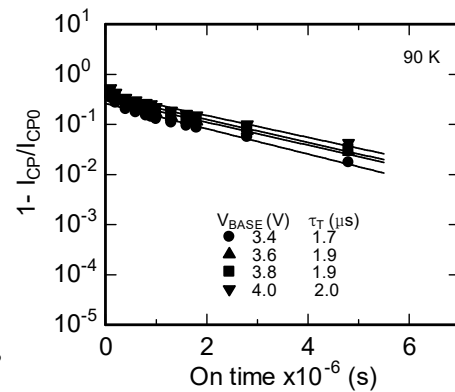


Fig. 13 Time constant of the on-time dependent CP current derived from heterointerface traps generated by hot carriers.

traps in future small devices containing only a few traps.

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