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Fabrication of Quasi-Vertical GaN-on-SiC Trench MOSFETs

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Abstract. We demonstrate quasi-vertical GaN MOSFETs fabricated on SiC substrates. The GaN epitaxial layers were grown via MOCVD on 100 mm 4H-SiC wafers, with the device structure consisting of a 2.5 μm drift layer and a Mg doped p-GaN body. The fabricated transistors exhibit normally-off characteristics, with low off-state leakage behavior and an on/off ratio of over 10^8. The specific on-resistance was measured to be $8.5\ \mathrm{m\Omega cm^2}$, which compares favorably to devices fabricated on other foreign substrates. Our results demonstrate an alternative substrate for realizing vertical GaN devices, which potentially offers better material quality and thermal properties compared with other foreign substrate choices.

Introduction

Gallium nitride (GaN) is currently a popular candidate for next generation power systems. Lateral GaN transistors based on AlGaN/GaN heterostructures have been widely adopted as efficient and compact replacements for silicon power devices in specific low voltage (<650 V) applications. For medium voltage applications over 1.2 kV, these high electron mobility transistors (HEMTs) are inherently difficult to scale due to the lateral device architecture – reaching higher breakdown voltages requires a proportionally larger chip area and creates technical challenges related to passivation, high surface electric fields and device reliability [1].

Silicon carbide (SiC) has been the next generation wide-bandgap material of choice for medium voltage applications to surpass silicon in terms of efficiency, size and weight. In contrast to GaN, SiC devices can be based on tradition silicon architecture such as vertical trench MOSFETs, which offer a beneficial trade-off between on-resistance and breakdown voltage and where breakdown voltage can be scaled independently of chip area by increasing the thickness of the drift layer.

Vertical GaN MOSFETs offer a possible route for bringing GaN into the medium voltage application space. In addition to voltage scaling, vertical devices offer easier thermal management compared with lateral HEMT devices, due to thermal losses being created in the bulk and removed from both sides of the die [2]. Developing high quality GaN epitaxy to allow the growth of thick drift layers with low defectivity, controllable doping and high mobility remains a key challenge for vertical devices [3]. While GaN grown on GaN substrates offers superior material quality due to lattice and CTE match, the high cost of GaN substates has spurred on the development of epitaxy technology to allow the growth of thick drift layers on foreign substrates. Vertical GaN transistors have previously been demonstrated, with buffered epitaxy used to accommodate GaN on non-lattice matched silicon [4, 5]. Vertical GaN has also been reported on specialist engineered CTE matched substrates [6].

An alternative approach is the growth of GaN on SiC – SiC has a closely matched lattice parameter, allowing growth of GaN with lower dislocation densities compared with other semiconductor substrate materials, along with offering superior thermal properties to both Si and bulk GaN [7].

Here we report on the realization of quasi-vertical GaN-on-SiC trench MOSFETs using 100mm semi-insulating 4H-SiC substrates, fabricated without the need for epitaxial regrowth. A fabrication process was developed to mitigate damage to the n-p-n sidewalls that form the gate and drain contact trenches. A low specific on-resistance (Ron, sp) of 8.5 $m\Omega cm^2$ is reported at a drift thickness of 2.5 µm, which supported an off-state breakdown voltage of 218 V. Low subthreshold and gate oxide leakage currents were observed, with off-state leakage staying below 10^{-2} A/cm^2 until breakdown.

Device Fabrication

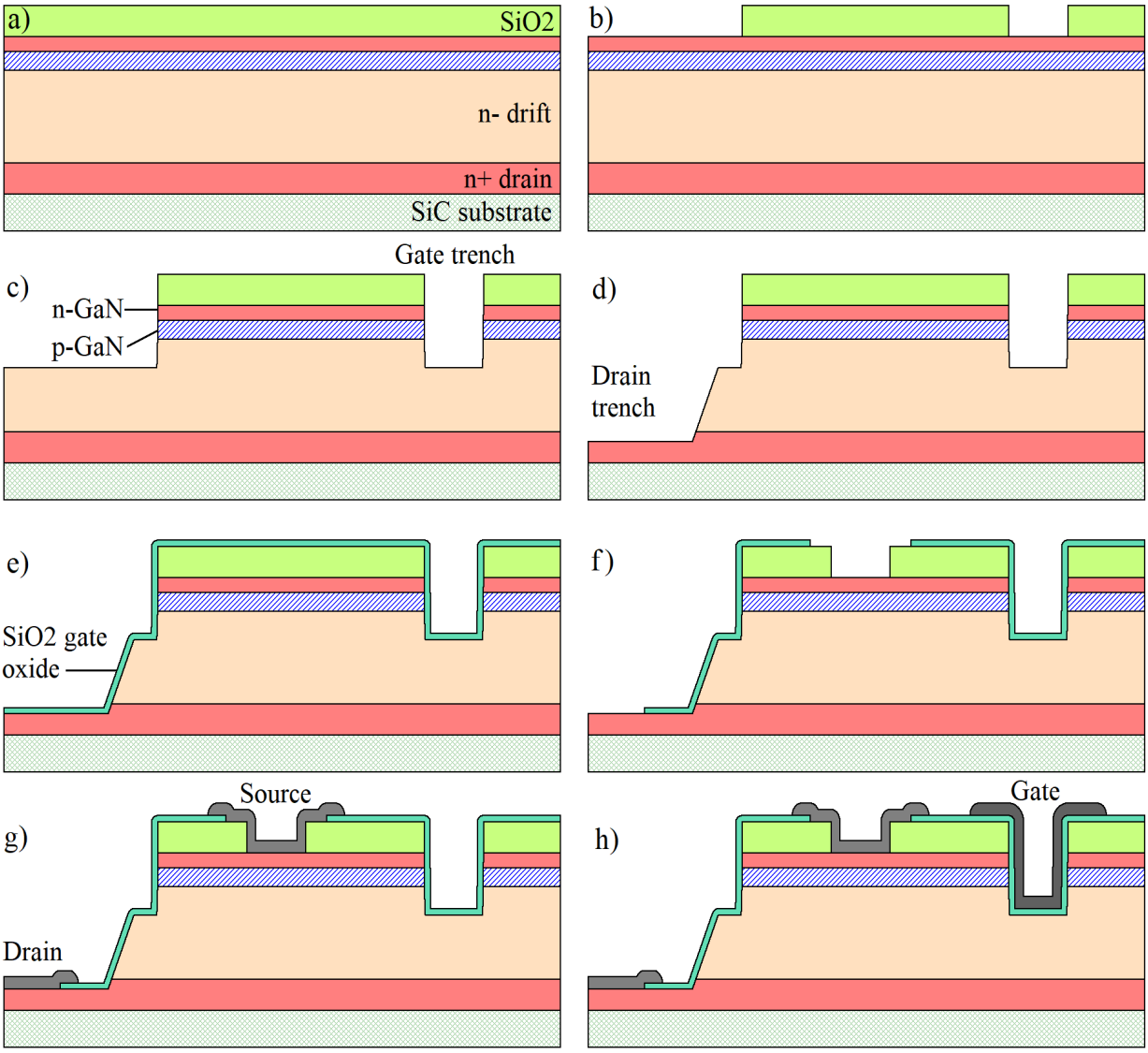

Fig. 1. Schematic showing simplified fabrication process for the quasi-vertical GaN-on-SiC trench MOSFET. (a) Deposition of the SiO_2 hardmask via PECVD. (b) Opening the hardmask to define the gate and drain trench areas. (c) Cl_2/Ar based dry etch process to etch the gate trench. (d) Additional dry etch process to extend the drain trench down to n+ drain epi-layer using a photoresist mask. (e) Deposition of SiO_2 gate dielectric. (f) Selective removal of gate dielectric and opening of oxide hardmask using a CF_4 based dry etch, to allow contacting of underlying GaN. (g) Lift-off of ohmic contact metallisation in source and drain regions (Ti/Al 20/200 nm). (h) Lift-off of gate metal (Ti/Al 20/200 nm).

The epitaxial layers were grown on 100 mm semi-insulating 4H-SiC substrates using metal organic chemical vapor deposition (MOCVD). A 60 nm AlN nucleation layer was first grown on the substrate, followed by the device layers: 500 nm n+-GaN drain layer (Si, $1 \times 10^{19}\mathrm{cm}^{-3}$), 2500 nm n-GaN drift layer (Si, $1 \times 10^{17}\mathrm{cm}^{-3}$), 400 nm p-GaN (Mg, $3 \times 10^{19}\mathrm{cm}^{-3}$), 220 nm n-GaN (Si, $5 \times 10^{18}\mathrm{cm}^{-3}$) and 20 nm n+-GaN contact layer (Si, $1 \times 10^{19}\mathrm{cm}^{-3}$).

A schematic of the device fabrication process flow is shown in Fig. 1. The initial step was deposition of a 500nm SiO_2 hardmask via PECVD (Fig. 1a), followed by photolithographic patterning to define the trenches. Trench sidewalls were aligned parallel to the GaN *m*-plane, which has been shown to increase channel mobility compared with the *a*-plane sidewalls [4, 8]. The oxide hardmask was opened using a CF_4 based dry etch and the photoresist was then stripped to prevent sputtering/re-deposition during the GaN trench etch (Fig. 1b). Trench etching is a key part of the vertical GaN fabrication process, with smooth vertical sidewalls being an essential requirement for optimizing channel mobility [4, 9, 10]. An SPTS Synapse etch tool was used to develop a Cl_2/Ar based dry etch process, with the gate trench etched to a depth of 1 µm into the epi-layers (Fig. 1c). In addition to etching the gate trench, this process simultaneously etched the first stage of the drain trench, which was subsequently extended down to the drain layer using a similar Cl_2/Ar plasma and a photoresist mask (Fig. 1d). This two-stage approach enabled the oxide hardmask and high-quality gate trench etch to also terminate the device by etching through the n-p-n epi-layers. For the additional drain trench etch process using a photoresist mask, lower etch quality resulting from mask-induced sidewall roughness is less critical, as surface conduction paths would not contribute to off-state leakage across the n-p-n junctions.

To remove etch residues, reduce sputter related defects and improve the smoothness of the sidewalls, a 25% tetramethylammonium hydroxide (TMAH) wet etched was performed for 1hr at 80°C [4, 5]. Immediately following this surface treatment, the 100nm SiO_2 gate oxide was deposited using PECVD (Fig. 1e). This gate oxide is also deposited on the drain trench sidewall, which serves to passivate leakage paths across the exposed n-p-n junctions. A dry etch process was then used to open the oxide hardmask in the source contact region and to remove the gate dielectric from both the source and drain contact regions (Fig. 1f). For the Ohmics, a lift-off process was used to define the source and drain contacts (Ti/Al 20/200 nm, Fig. 1g), which were subsequently annealed at 400°C for 30s in N2 ambient to give a low specific contact resistance ρ_c of $2 \times 10^{-6}\ \Omega\mathrm{cm}^{-2}$, which compares favorably with a survey of the literature data on GaN n-type Ohmic contacts [11]. Finally, the gate metallization (Ti/Al 20/200 nm) was deposited using a similar lift-off process (Fig. 1h).

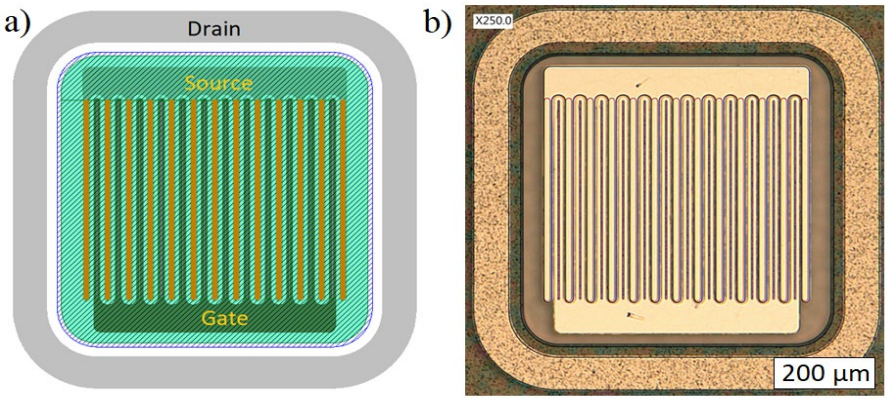

Fig. 2. (a) Top-down mask layout schematic of quasi-vertical GaN-on-SiC trench MOSFET showing layout of source and gate fingers and source, gate and drain pads. (b) Microscope image of fabricated device with gate trenches visible under gate metallisation.

Devices measured approximately 1x1 mm including the pads and ring drain contact and the designed gate trench width was 2 µm. The mask layout and a microscope image of the fabricated device is shown in Fig 2.

Results and Discussion

The transfer and output characteristics of the quasi-vertical MOSFET are shown in Fig. 3a and Fig. 3b, respectively, with the current values normalized to the gate trench area [4, 5, 12]. The transfer characteristics confirmed the normally-off switching operation of the device, with a relatively high on-state current density of 0.8 kA/cm^2 and a low off-state leakage current density of 4×10^{-9} kA/cm^2, leading to an on/off ratio of over 10^8 (inset Fig. 3a), which demonstrates the effective current blocking of the p-n junction in the off-state and compares favorably with GaN MOSFETs fabricated on other foreign substrates [4, 5, 13]. The threshold voltage, V_{th}, extracted from extrapolating the linear part of the curve, is approximately 10 V, which is higher that has been previously reported on vertical GaN devices fabricated on silicon substrates [4, 5, 14], suggesting fixed oxide charges and/or traps in the oxide bulk and near interface [15]. This could be improved by further development of the gate trench interface and dielectric deposition process, with Al_2O_3 generally being the preferred dielectric material for vertical MOS devices to mitigate these issues [14]. Despite this, V_{th} was found to be stable under several repeats of the transfer characteristics, with no substantial change in V_{th} observed due to e.g. initial filling of charge traps at higher V_{GS}. The gate oxide leakage current is shown inset in Fig. 3a and remained low even under strong inversion (2×10^{-7} kA/cm^2 at $V_{GS} = 20$ V).

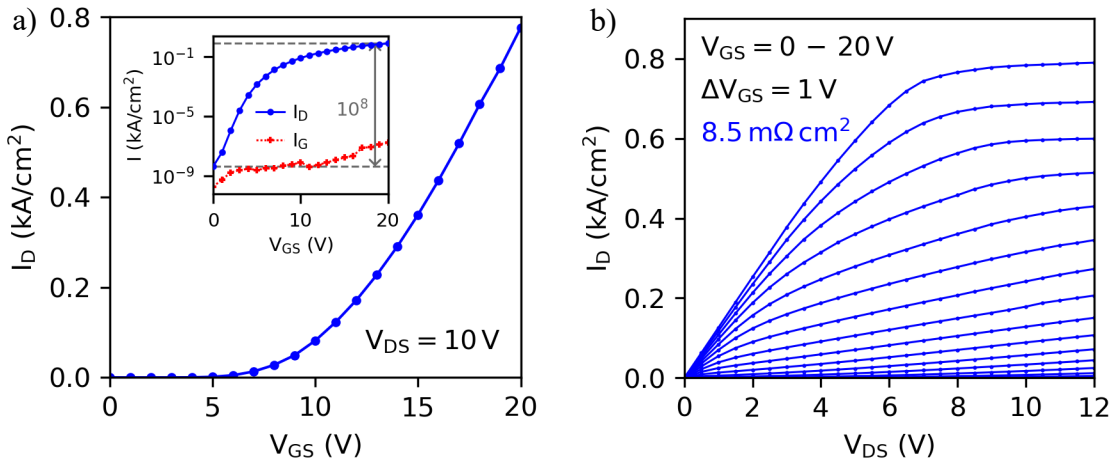

Fig. 3. (a) Transfer characteristics of quasi-vertical GaN-on-SiC MOSFET with inset semi-log plot showing low gate oxide (I_G) and off-state leakage current (I_D). (b) Output characteristics with specific on-resistance extracted from linear portion of curve at $V_{GS} = 20$ V.

A specific on-resistance ($R_{on,sp}$) of 8.5 $m\Omega cm^2$ was extracted from the output characteristics, which is comparable to, but slightly higher than, the on-state resistance measured for GaN MOSFETs fabricated on foreign substrates with thicker drift layers [4, 13, 16]. This indicates high resistance contribution due to lower channel mobility, which can be attributed to non-idealities at the interface such as oxide interface traps and surface roughness induced scattering [15]. A lower estimate of the channel mobility can be extracted from the transfer characteristics using the equation [17]:

$$\frac{dI_D}{dV_{GS}}\bigg|_{V_{DS}=const} = \frac{Z}{L}\mu_{ch}C_{ox}V_{DS}$$

where Z is the channel width, L is the channel length, μ_{ch} is the channel mobility and C_{ox} is the specific capacitance of the gate oxide. Using the device dimensions and assuming a dielectric constant of 3.9 for SiO_2, a maximum channel mobility of 6 $cm^2/(V\,s)$ was obtained, as show in Fig. 4a. This assumes a dominant contribution to the total on-resistance from the channel, with other contributions becoming negligible at high p-GaN doping concentrations and low channel mobilities [18]. These characteristics were achieved without any post-etch activation anneal to activate the Mg atoms in the p-body close to the trench sidewall [4, 5, 12]. The Mg activation rate of p-GaN is typically only 1-

3% [19], a higher activation of the Mg than anticipated could also have contributed to the high threshold voltage and relatively low channel mobility observed here [18]. It should be noted that no current collapse or dynamic on-state behavior is observed in the characteristics of the GaN transistor, due to the nature of the device structure, offering advantages over lateral GaN HEMTs.

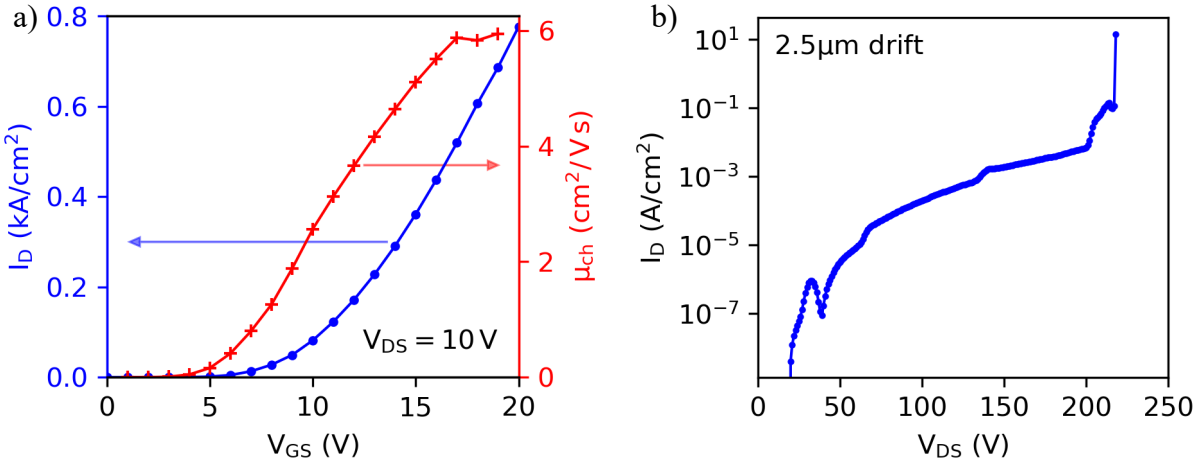

Fig. 4. (a) Transfer characteristics and estimated field-effect mobility extracted from the gradient of the transfer characteristics. (b) Semi-log plot of off-state leakage and breakdown characteristics of the 2.5 µm drift layer.

The off-state characteristics of the drift layer were also investigated. Fig. 4b shows the leakage and breakdown characteristics, with drain-to-source leakage current staying below 10^{-2} A/cm^2 until breakdown at 218 V. This translates to a blocking voltage of 87 V/µm of drift layer, which could be improved by optimizing the particular layout and process details to mitigate high field points in the device structure.

Conclusion

Quasi-vertical GaN-on-SiC trench MOSFETs were realized on 100mm 4H-SiC substates using a specially developed fabrication process to avoid leakage paths on the drain trench (termination) sidewalls. The devices exhibited normally-off behavior with a subthreshold leakage current density as low as 4×10^{-9} kA/cm^2 and a on/off ratio of over 10^8. A specific on-resistance of 8.5 mΩcm^2 was achieved, which along with the threshold voltage, is expected to improve with optimization of the gate trench process, GaN-dielectric interface and p-body doping concentration. The breakdown voltage of the 2.5 µm drift layer was measured to be 218 V. With SiC power devices reaching maturity, the decrease in the cost of SiC wafers due to increased production may lead to renewed interest in SiC as a substrate for low dislocation GaN epitaxy for vertical devices.

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