Optimized 750V SiC MOSFETs for Electric Vehicle Inverter Operation

Submitted: 2022-09-09

Accepted: 2022-11-11

Online: 2023-05-19

Arash Salemi^{1,a*}, Bob Zhu^{2,b}, Phong Bui-Quang^{1,c}, Yu Ding^{2,d}, Kiran Chatty^{1,e}, Alvin Liu^{2,f}, and David Sheridan^{1,g}

¹Alpha and Omega Semiconductor, Inc., Sunnyvale, CA, USA

²Alpha & Omega Semiconductor (Shenzhen) Ltd., Shanghai, China

^aarash.salemi@us.aosmd.com, ^blisi.zhu@sh.aosmd.com, ^cpbquang@us.aosmd.com, ^dyuding@sh.aosmd.com, ^ekiran.chatty@us.aosmd.com, ^fzhan.liu@sh.aosmd.com ^gdavid.sheridan@us.aosmd.com

Keywords: SiC MOSFET, AECQ-101, $R_{DS(on)}$, $R_{ON,SP}$, V_{th} , short circuit withstand time (SCWT), E_{ON} , E_{OFF} , TDDB

Abstract. We report an AEC-Q101-qualified 750V, 15 m Ω planar SiC MOSFETs with a long short circuit withstand time (SCWT) of > 9 μ s at V_{DS}=400V and V_{GS}=15V and a low specific on-resistance (RoN,SP) of 2.1 m Ω .cm² at V_{GS}=15V designed for xEV traction inverter applications. The R_{DS(on)} at V_{GS}=15V increases from 15m Ω at 25 °C to 21 m Ω at 175 °C. A low turn-on (E_{ON}) and turn-off (E_{OFF}) switching energy loss of 95.5 μ J and 67 μ J at I_{DS}=75A, V_{DS}=400V was measured at 25 °C. The gate oxide lifetime at worst case operating fields of 5MV/cm is >> 20 years.

Introduction

SiC MOSFETs are now the ideal semiconductor choice for high-efficiency xEV traction inverters. These applications demand SiC MOSFETs with low R_{DS(on)} which in turn requires low R_{ON,SP} to drive down the die size, improve yields and reduce cost. The design for low R_{ON,SP} in planar MOSFETs generally requires a thinner gate oxide (t_{ox}) and/or shorter channel length – both of which result in reduced short-circuit withstand times (SCWT). However, in automotive inverter applications, long SCWT is favored due to possible locked rotor and climb events in a normal drive cycle [1]. The significantly shorter SCWT of SiC MOSFETs compared to traditional IGBTs has been one of the major concerns for market acceptance in motor drive applications[2]. Although some circuit design methods to improve SCWT capability have been recently reported [2], these advanced circuit methods required for dealing with SiC planar devices might not be needed if such devices were available with long SCWT.

In this work, we report on an AEC Q101-qualified 750V SiC MOSFET platform that breaks the traditional low $R_{ON,SP}$ vs SCWT trade-off by showing a highly-reliable large area planar SiC MOSFET with a long SCWT of >9 μ s combined with a very low $R_{ON,SP}$ of 2.1m Ω .cm² at V_{GS} =15V. These devices a have measured stable V_{th} , robust UIS capability, and ultra-low switching energies thus making this device attractive for high-efficiency traction inverter applications.

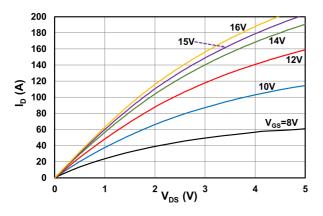
Experimental Results

Fig. 1 and Fig. 2 show the drain characteristics of the 750V, $15m\Omega$ SiC MOSFETs acquired at V_{GS} values ranging from 8V to 16V at at 25 °C and 175 °C, respectively. The nominal R_{DS(on)} of the MOSFET extracted at V_{GS}=15V, I_{DS}=24A is 15 m Ω which results in a low specific on-resistance (Ro_{N,SP}) of 2.1 m Ω .cm². The device is normally-off at V_{GS}=0V with a typical drain to source leakage current <100nA at V_{DS}=750V at 25 °C. The R_{DS(on)} at V_{GS}=15V increases <1.4X from 25 °C to 150 °C lower than many trench devices. Fig. 3 shows the normalized R_{DS(on)} vs. Junction temperature at V_{DS}=15V, I_D=24A of this device along with two acquired commercially available MOSFETs (suppliers C and D) using the same setup. Fig. 4 shows the normalized V_{th} vs. Junction temperature for these 3 devices acquired at V_{GS}=15V, I_D=24A using the same test setup. The V_{th} of the 750V, 15m Ω MOSFETs at V_{GS}=15V and I_D=24mA decreases from 2.5V at 25 °C to 1.9V at 175 °C.

Fig. 5 shows the short circuit test waveform measured on the 750V, $15m\Omega$ MOSFET in a 4L TO-247 package at V_{GS}=15V, V_{DS}=400V with an SCWT of 9.6µs recorded. Table I presents a comparison of the short circuit times measured in this work with prior works. The data corresponding to the commercially available MOSFETs (suppliers A, B, C, D, E) was acquired using the same test setup as this work, and the results for devices F and G are from published reports. The short circuit time of >9 µs represents a significant improvement compared to the published reports.

Fig. 6 compares the body diode reverse recovery charge (Q_{rr}) of 750V, 15m Ω MOSFET with suppliers C and D at V_{DC}=400V, I_F=50 A, 25 °C, di/dt=2500 A/us, L=30 μ H, and V_{GS}=-5V utilizing the same setup. The 750V, 15m Ω SiC MOSFET shows 1.1X and 1.4X lower Q_{rr} than suppliers C and D.

Fig. 7 shows the turn-on (E_{ON}) and turn-off (E_{OFF}) switching energy loss values measured as a function of I_{DS} for the 750V, $15m\Omega$ SiC MOSFET. It also shows the switching measurements acquired commercially available suppliers C (650V, $15m\Omega$) and D (750V, $18m\Omega$) using the same test setup. The data was acquired at V_{DS} =400V, R_{Goff} =0 Ω , R_{Gon} =2 Ω , V_{GS} =-5V to +15V. Also shown in this figure are measurements acquired from commercially available suppliers C (650V, $15m\Omega$) and D (750V, $18m\Omega$) using the same test setup. The E_{ON} of this work is 48% and 30% lower than suppliers C and D in I_{D} =100A. Likewise, The E_{OFF} of this work is 68% and 57% lower than suppliers C and D in I_{D} =100A.



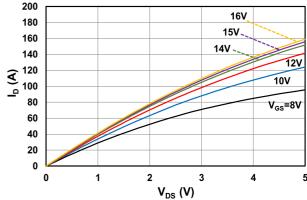


Fig. 1. Drain characteristics of 750V, $15m\Omega$ SiC MOSFET assembled in 4L TO-247 package at 25 °C.

Fig. 2. Drain characteristics of 750V, $15m\Omega$ SiC MOSFET assembled in 4L TO-247 package at 175 °C.

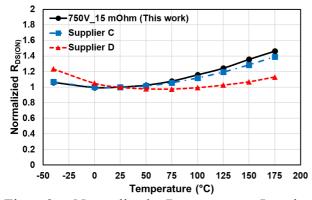


Fig. 3. Normalized $R_{DS(on)}$ vs. Junction temperature for 750V, $15m\Omega$ MOSFET (this work), supplier C (650V, $15m\Omega$), and D (750V, $18m\Omega$) acquired at $V_{GS}=15V$, $I_D=24A$ using the same test setup.

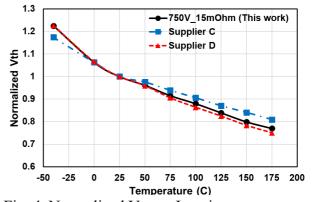


Fig. 4. Normalized V_{th} vs. Junction temperature for 750V, $15m\Omega$ MOSFET (this work), supplier C (650V, $15m\Omega$), and D (750V, $18m\Omega$) acquired at V_{GS} =15V, I_{D} =24A using the same test setup.

The long-term integrity of the gate oxides of SiC power MOSFETs is a primary concern for automotive applications. Fig. 8 shows the t63% lifetimes, extracted from time-dependent dielectric breakdown (TDDB) measurements on this work at 150 °C, plotted as a function of V_{GS}. The gate oxide lifetime at its nominal V_{GS}=15V is >> 20 years. Fig. 9 shows the V_{th} of the 750V, 15 m Ω MOSFET as a function of stress time during HTGB stress performed at V_{GS}=+18V, 175 °C for 1000 hours. An increase in V_{th} of <4% was observed after 1000hrs. These results demonstrate a manufacturable, rugged, and reliable 750V SiC MOSFET platform that has been developed for automotive applications.

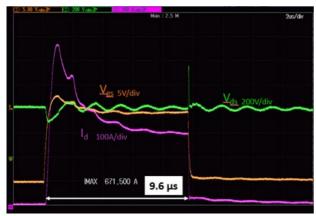


Fig. 5. Short circuit measurement of 750V, $15\text{m}\Omega$ at V_{GS}=15V and V_{DS}=400V. A Short Circuit time of 9.6 μ s was extracted.

Table I. Comparison of Short Circuit times for 750V, 15m m Ω SiC MOSFET (this work) with commercial and published reports for 650V/750V MOSFETs.

Device	Type	V _{DS}	R _{DS(on)}	SCWT
		(V)	$(m\Omega)$	(µs)
Supplier A	Trench	650	60	8
Supplier B	Planar	650	45	5
Supplier C	Planar	650	15	4.3
Supplier D	Planar	750	18	2.1
Supplier E	Planar	750	23	3.4
F [3]	Planar	650	85	4.4
G [4]	Planar	650	7	8
This work	Planar	750	15	9.6

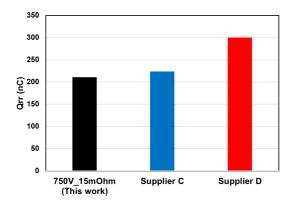


Fig. 6. Body diode reverse recovery charge (Q_{rr}) of 750V, 15m Ω MOSFET with supplier C (650V, 15m Ω) and D (750V, 18m Ω) at V_{DC}=400V, I_F=50A, 25 °C, di/dt=2500A/us. L=30 μ H, V_{GS}=-5V using the same setup.

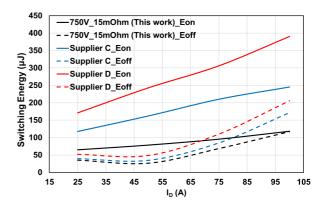
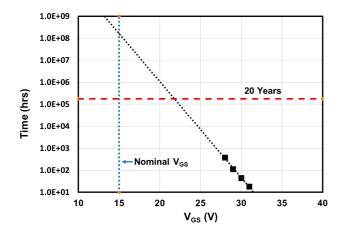


Fig. 7. E_{ON} and E_{OFF} vs. I_{DS} for 750V, 15 m Ω MOSFET (this work), supplier C (650V, 15m Ω) and D (750V, 18m Ω) acquired at V_{DS}=400V, R_{Goff} =0 Ω , R_{Gon}= 2 Ω , V_{GS}= -5V/+15V using the same test setup.



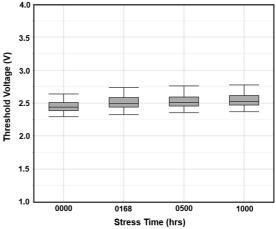


Fig. 8. Lifetimes extracted from TDDB measurements on 750V process technology vs. Electric field in the gate oxide.

Fig. 9. Shift in V_{th} vs. time for 750V SiC MOSFET during high-temperature Gate Bias stress test at V_{GS}=18V at 175 °C.

Summary

An AEC Q101-qualified 750V planar SiC MOSFET platform that breaks the traditional low $R_{ON,SP}$ vs SCWT trade-off by showing a highly-reliable large area planar SiC MOSFET with a long SCWT of >9 μ s at V_{DS} =400V, low $R_{ON,SP}$ of 2.1 μ 0.cm² at V_{GS} =15V. These rugged and highly reliable planar SiC MOSFETs with stable V_{th} , robust UIS capability, ultra-low switching energies, low $R_{ON,SP}$ and high SCWT are attractive devices for high-efficiency traction inverter applications.

References

- [1] D. Xing et al., "Design Strategies for Rugged SiC Power Devices," Proceedings of the 2019 *IEEE International Reliability Physics Symposium (IRPS)*, pp. 1-5, DOI: 10.1109/IRPS.2019.8720557
- [2] D. Xing et al., "1200-V SiC MOSFET Short-Circuit Ruggedness Evaluation and Method to Improve Withstand Time," Proceedings of the 2022 *IEEE Journal of Emerging and Selected Topics in Power Electronics (JESTPE)*, DOI: 10.1109/JESTPE.2022.3144995
- [3] A. Agarwal et al, "Switching and Short-Circuit Performance of 27 nm Gate Oxide, 650 V SiC Planar-Gate MOSFETs with 10 to 15 V Gate Drive Voltage," Proceedings of the 2020 *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 250-253, DOI: 10.1109/ISPSD46842.2020.9170151
- [4] A. Bhalla et al, "Ultra-high speed 7mohm, 650V SiC half-bridge module with robust short circuit capability for EV inverters," Proceedings of the 2019 *IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pp. 191-194, DOI: 10.1109/ISPSD.2019.8757666