

## Influence of Cell Design and Gate-to-Source Voltage on Avalanche Robustness of SiC MOSFET Integrated JBS Diode

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**Keywords:** SiC MOSFET integrated JBS Diode, avalanche robustness(UIS capability), failure mechanism.

**Abstract.** In this work, 1200 V SiC JMOS devices with different  $W_{sch}$  (2  $\mu\text{m}$ , 2.5  $\mu\text{m}$  and 3  $\mu\text{m}$ ) are fabricated. The single UIS tests under different  $V_{gs\_off}$  (-5 V and 0 V) are carried out to investigate the avalanche capability. The avalanche robustness among various  $W_{sch}$  under same  $V_{gs\_off}$  is also compared and analyzed by simulation. The different failure mechanisms between different  $V_{gs\_off}$  are studied by observation of de-cap result and analysis through simulation. The method of improving avalanche ruggedness of JMOS is proposed.

### Introduction

The SiC MOSFET, operating at high-temperature and high-speed condition, has been proved to enhance power density significantly [1]. The performance in the third quadrant receives much attention for the body diode of SiC MOSFET can be used as a freewheeling diode in the forward circuit, bridge rectifier and PFC [2]. However, the body diode of SiC MOSFET, PN diode, will increase switching loss for its high turn-on voltage and long reverse time [3]. Besides, large stacking faults induced by basal plane dislocations will occur when PN diode conducts, which will increase on-resistance and diode voltage drop[4]. To eliminate this effect caused by the PN body diode, the SiC MOSFET embedded a low turn-on voltage Junction-Barrier-Schottky diode (JMOS) has been proposed [5-7]. The Junction-Barrier-Schottky diode can work during the operation in place of PN diode for its lower built-in potential and reduce the risk of potential failures caused by electrons and holes recombination.

The ruggedness of body diode remains a concern for JMOS in applications. Some works have been proposed to examine the reliability of JMOS, including short-circuit reliability, UIS reliability and surge current capability [8,9]. However, the mechanism study on avalanche robustness of JMOS is not enough and specific especially for different  $V_{gs\_off}$ .

In this work, 1200 V SiC JMOS devices with different  $W_{sch}$  (2  $\mu\text{m}$ , 2.5  $\mu\text{m}$  and 3  $\mu\text{m}$ ) are fabricated. The single UIS tests under different  $V_{gs\_off}$  (-5 V and 0 V) are carried out to investigate the avalanche capability. The avalanche robustness among various  $W_{sch}$  under same  $V_{gs\_off}$  is also compared and analyzed by simulation. The different failure mechanisms between different  $V_{gs\_off}$  are studied by observation of de-cap result and analysis through simulation. The method of improving avalanche ruggedness of JMOS is proposed.

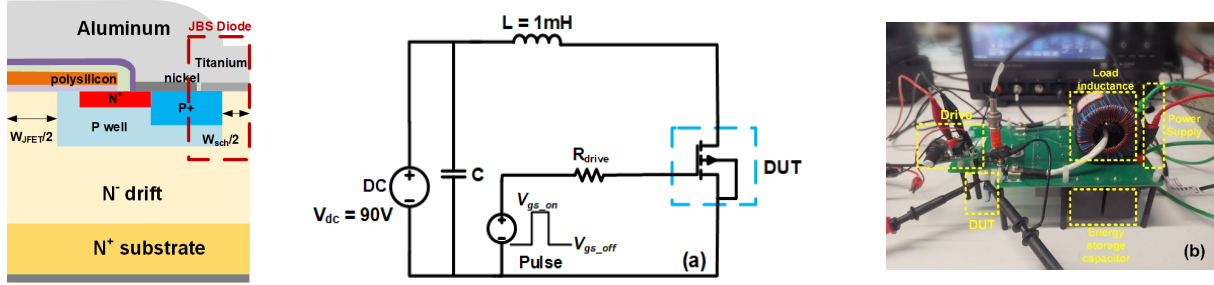
### Single Unclamped Inductive Switching Test Result

In this study, the Schottky barrier is integrated into the source region, which is referred as JMOS. The half-cell structure of 1.2kV JMOS in this work is shown in Fig. 1.

The UIS test bench and circuit schematic are shown in Fig. 2(a) and (b). The load inductance is 1mH. Power charges the inductor to a peak current when the device under test (DUT) turns on. The drain to source voltage climbs up to avalanche voltage and the current goes down until the stored energy is dissipated by the device when DUT turns off. Avalanche energy can be calculated by Eq. (1):

$$E_{ava} = \int_0^{t_{ava}} V_{ds} \cdot I_{ds} dt \quad (1)$$

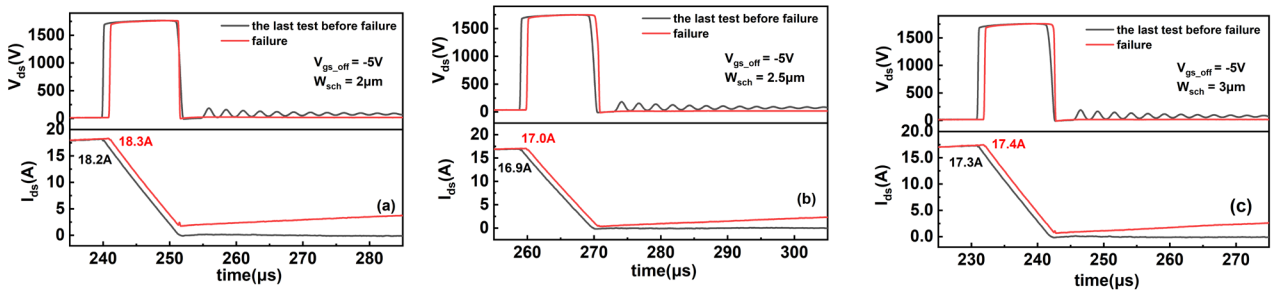
where  $t_{ava}$  is the avalanche time,  $V_{ds}$  and  $I_{ds}$  are the drain to source voltage and drain current of the DUT.



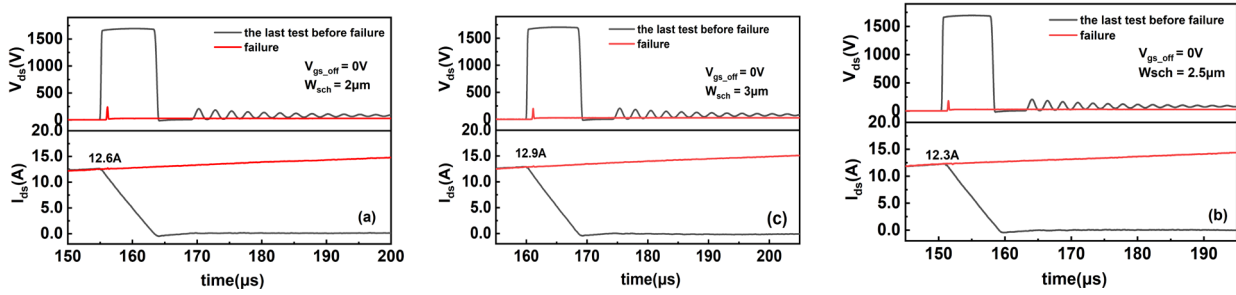
**Fig. 1:** Schematic of SiC MOSFET integrated Junction-Barrier-Schottky diode (JMOS) with  $W_{JFET} = 3 \mu\text{m}$ .

**Fig. 2:** (a) Schematic of Single Pulse Unclamped Inductive Switching test circuit. (b) UIS test bench. Test conditions:  $V_{dc} = 90\text{V}$ ,  $L = 1\text{mH}$ ,  $V_{gs\_on} = 15\text{V}$ ,  $V_{gs\_off} = -5\text{V}/0\text{V}$ , room temperature ( $T_0$ ) = 300K.

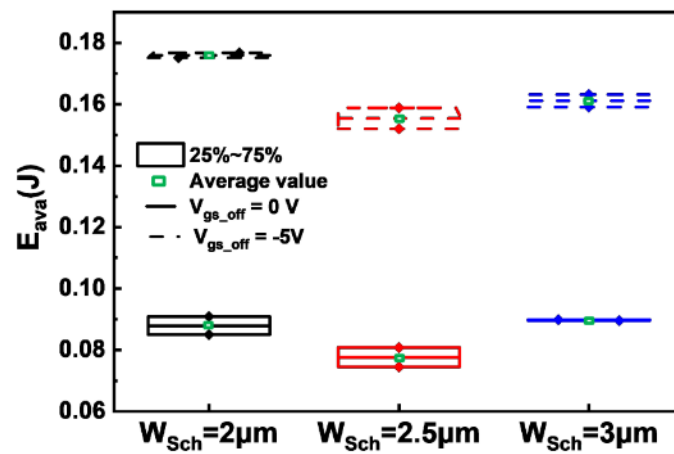
The single UIS test waveforms for JMOS with different  $W_{sch}$  ( $2\mu\text{m}$ ,  $2.5\mu\text{m}$  and  $3\mu\text{m}$ ) under  $V_{gs\_off} = -5\text{V}$  and  $V_{gs\_off} = 0\text{V}$  are shown in Fig. 3(a), (b), (c) and Fig. 4(a), (b), (c). The last non-destructive waveform and failure waveforms for three types of devices are shown. Two devices are evaluated for each test condition. The maximum avalanche energy ( $E_{ava\_max}$ ) is summarized in Fig. 5. It is found that JMOS with  $2.5\mu\text{m}$  Schottky width has the lowest avalanche robustness under  $V_{gs\_off} = 0\text{V}$  and  $-5\text{V}$ . For JMOS with fixed  $W_{sch}$ ,  $E_{ava\_max}$  under  $V_{gs\_off} = -5\text{V}$  is nearly twice of that under  $V_{gs\_off} = 0\text{V}$ .



**Fig. 3:** The last UIS test before failure and failure test waveform ( $V_{ds}$ ,  $I_{ds}$ ) under  $V_{gs\_off} = -5\text{V}$  of JMOS with (a)  $W_{sch} = 2 \mu\text{m}$  (b)  $W_{sch} = 2.5 \mu\text{m}$  or (c)  $W_{sch} = 3 \mu\text{m}$ . The maximum avalanche currents for JMOS with  $2 \mu\text{m}$ ,  $2.5 \mu\text{m}$  and  $3 \mu\text{m}$  Schottky diode width are 18.2 A, 16.9 A and 17.3 A. The avalanche voltage is around 1700V.



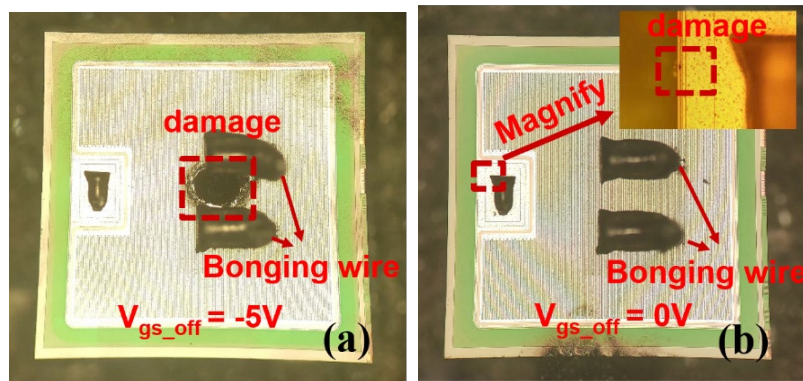
**Fig. 4:** The last UIS test before failure and failure test waveform ( $V_{ds}$ ,  $I_{ds}$ ) under  $V_{gs\_off} = 0V$  of JMOS with (a)  $W_{sch} = 2\mu m$  (b)  $W_{sch} = 2.5\mu m$  (c)  $W_{sch} = 3\mu m$ . The maximum avalanche currents for JMOS with  $2\mu m$ ,  $2.5\mu m$  and  $3\mu m$  Schottky diode width are 12.6A, 16.9A and 17.3A. The device fails immediately under  $V_{gs\_off} = 0V$  after the onset of avalanche and dissipates no energy during avalanche when the current is large enough, which is different from  $V_{gs\_off} = -5V$ .



**Fig. 5:** The maximum avalanche energy for JMOS with various Schottky diode width under different  $V_{gs\_off}$ . It is found that JMOS with  $2.5\mu m$  Schottky diode width has the lowest avalanche robustness under  $V_{gs\_off} = -5V$  and  $V_{gs\_off} = 0V$ . For JMOS with fixed  $W_{sch}$ , the maximum avalanche energy under  $V_{gs\_off} = -5V$  is nearly twice of that under  $V_{gs\_off} = 0V$ .

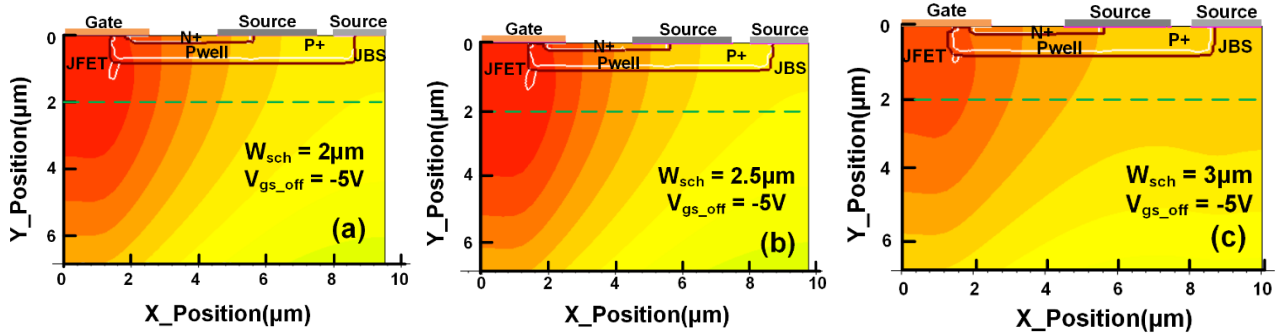
### Failure Mechanism Analysis

**De-caped results** To figure out the failure mechanism, the destructive devices are de-caped and the failure spot are displayed in Fig. 6. The large burn mark located in the active region under  $V_{gs\_off} = -5V$  test due to huge energy dissipation and junction temperature rise. On the other hand, the leakage current point is found near gate-finger under  $V_{gs\_off} = 0V$  test.

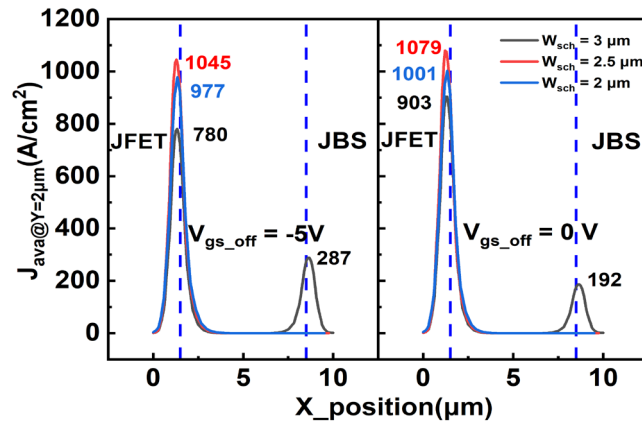


**Fig. 6:** Vertical view of failed JMOS ( $W_{sch} = 3\mu m$ ). The large burn damage between Bonding wire occurs under  $V_{gs\_off} = -5V$  test. The failure spot can be found near gate-finger under  $V_{gs\_off} = 0V$  test.

**UIS capability analysis under the same  $V_{gs\_off}$**  The UIS simulations are conducted for JMOS with different  $W_{sch}$ . For  $V_{gs\_off} = -5V$ , the lattice temperature distributions at the same time during avalanche for JMOS with different  $W_{sch}$  are shown in Fig. 7 and avalanche current density distribution at  $Y=2\mu m$  shown in Fig. 8. The JMOS with  $W_{sch} = 2.5\mu m$  has lowest avalanche robustness. Narrow  $W_{sch}$  leads to lower cell avalanche current density ( $J_{ava}$ ) under same chip area and wider  $W_{sch}$  means Schottky junction undertakes more avalanche current. The JMOS with  $W_{sch} = 2.5\mu m$  under  $V_{gs\_off} = 0V$  has the lowest UIS capability which has similar mechanism under  $V_{gs\_off} = -5V$ .

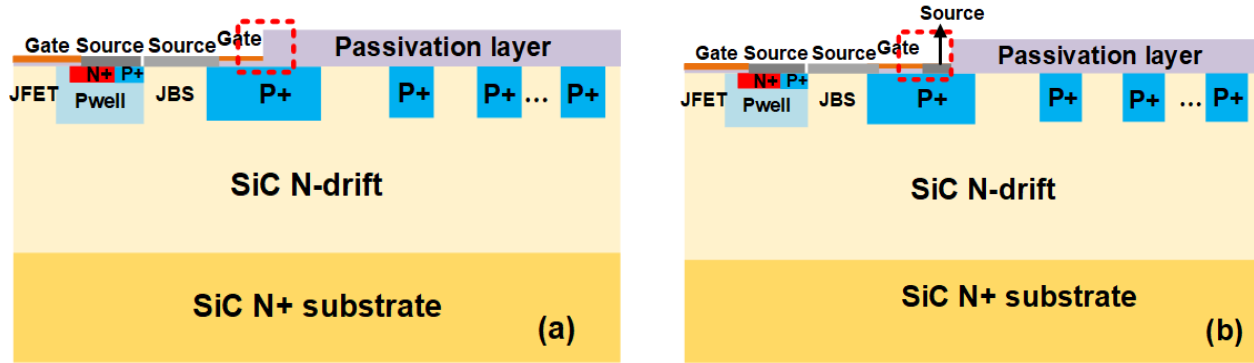


**Fig. 7:** UIS simulation results: the lattice temperature distributions at maximum average temperature during avalanche for JMOS with (a)  $W_{sch} = 2\mu m$  (b)  $W_{sch} = 2.5\mu m$  or (c)  $W_{sch} = 3\mu m$ . The temperature of hot point in JFET area is highest for  $W_{sch} = 2.5\mu m$ , which means its lowest avalanche robustness.

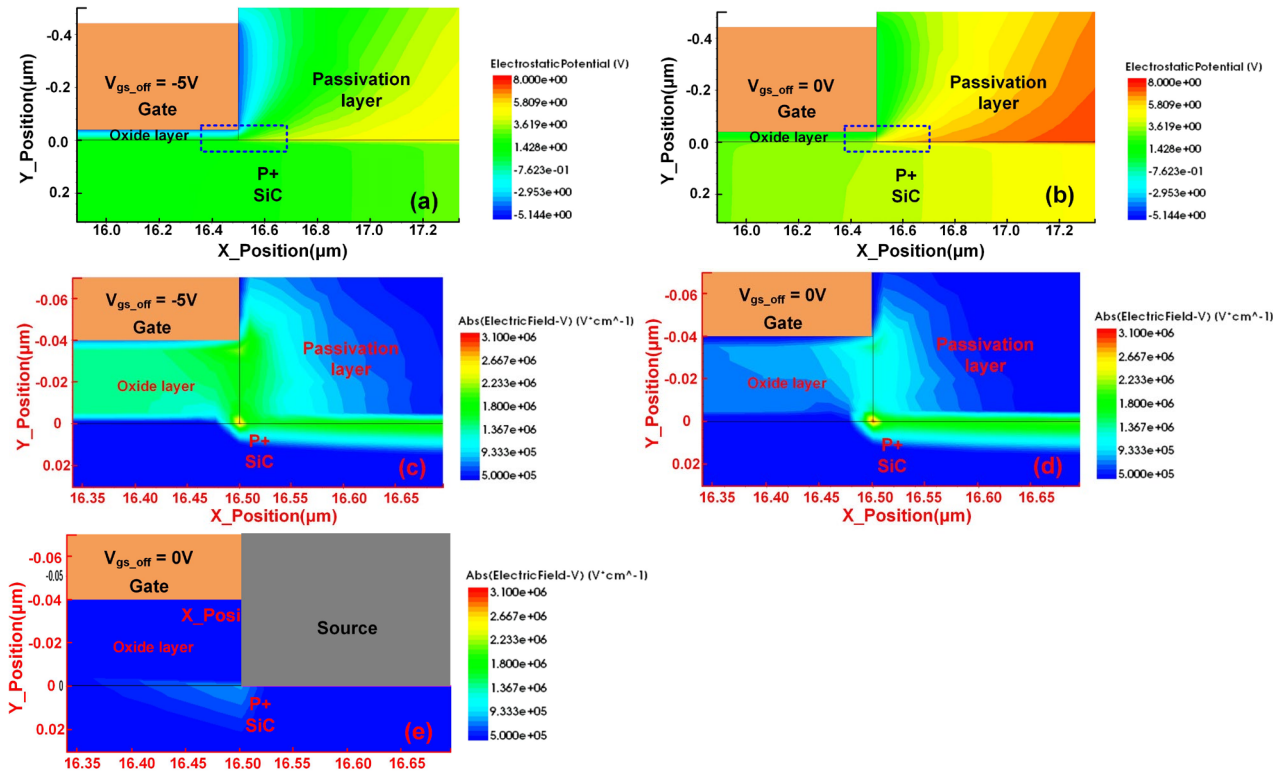


**Fig. 8:** Avalanche current density at  $Y=2\mu m$  (green dotted line in Fig. 7) at the same time during avalanche. The highest  $J_{ava}$  leads to the highest temperature in JFET area for  $W_{sch} = 2.5\mu m$ . When  $W_{sch}$  decreases, cell pitch decreases and cell number increases under same chip area. Therefore, the  $J_{ava}$  is lower for one cell and avalanche robustness is better. When  $W_{sch}$  increases, the  $J_{ava}$  is highest for one cell. However, JBS diode will undertake a portion of  $J_{ava}$  and thus, the current accumulation at Pwell corner near JFET area will be alleviated. Local heating power in JFET area is reduced and the avalanche robustness is enhanced.

**Failure mechanism analysis under different  $V_{gs\_off}$**  To find out the difference between  $V_{gs\_off} = -5V$  and  $0V$ , UIS simulations of transition region shown in Fig. 9(a) are carried out. The interaction of oxide, passivation layer near gate-finger is in red dotted line circle in Fig. 9. Take  $W_{sch} = 3\mu m$  for example, electrostatic potential distributions at the same  $J_{ava}$  for interaction area under  $V_{gs\_off} = -5V$  and  $0V$  are shown in Fig. 10(a) and (b). The electrostatic potential under  $V_{gs\_off} = 0V$  is denser. Electric field in blue dotted line area under  $V_{gs\_off} = -5V$  and  $0V$  shown in Fig. 10(c) and (d). Higher electric field occurs at tri-corner under  $V_{gs\_off} = 0V$ . The new transition region (shown in Fig. 9(b)) with source between oxide and passivation layer is proposed. The simulation result (Fig. 10(e)) shows the electric field at tri-corner decreases to safe level. Thus, the influence of cell design and  $V_{gs\_off}$  on avalanche robustness of SiC JMOS are investigated and new device design with source finger added in transition region is proposed in this work to enhance the avalanche robustness.



**Fig. 9:** (a) The existing transition region in JMOS. (b) The proposed transition region in JMOS. The interaction area of oxide, passivation layer near gate-finger and SiC area is in red dotted line circle. Source electrode is added between gate oxide and passivation layer in proposed region to decrease electric field in interaction area (red dotted line area).



**Fig. 10:** Electrostatic Potential distribution in existing interaction area at the same avalanche current under (a)  $V_{gs\_off} = -5V$  and (b)  $V_{gs\_off} = 0V$ . A surface depletion area is formed on the surface between SiC and SiO<sub>2</sub> due to interface charge. Electrostatic potential lines are denser under  $V_{gs\_off} = 0V$  in blue dotted line area compared with  $V_{gs\_off} = -5V$ , which means higher Electric field in this area. Electric field in blue dotted line area in (a) and (b) are shown in (c)  $V_{gs\_off} = -5V$  and (d)  $V_{gs\_off} = 0V$ . Higher electric field occurs at tri-corner of oxide, passivation layer and SiC area under  $V_{gs\_off} = 0V$ , which causes oxide premature breakdown at gate finger (as observed in Fig. 6(b)) during avalanche test. (e) Electric field in proposed interaction area under  $V_{gs\_off} = 0V$ . The electric field in tri-corner area is improved below 1MV/cm.

## Summary

1200 V SiC JMOS devices with different  $W_{sch}$  (2  $\mu m$ , 2.5  $\mu m$  and 3  $\mu m$ ) are fabricated. The single UIS tests under different  $V_{gs\_off}$  (-5 V and 0 V) are carried out to investigate the avalanche capability. It is found that JMOS with 2.5 $\mu m$  Schottky width has the lowest avalanche robustness under  $V_{gs\_off} = 0V$  and -5V. For JMOS with fixed  $W_{sch}$ ,  $E_{ava\_max}$  under  $V_{gs\_off} = -5V$  is nearly twice of that under  $V_{gs\_off} = 0V$ .

The avalanche robustness among various  $W_{sch}$  under same  $V_{gs\_off}$  is also compared and analyzed by simulation. Narrow  $W_{sch}$  leads to lower cell avalanche current density ( $J_{ava}$ ) under same chip area and wider  $W_{sch}$  means Schottky junction undertakes more avalanche current.

The different failure mechanisms between different  $V_{gs\_off}$  are studied by observation of de-cap result and analysis through simulation. Higher electric field occurs at tri-corner in the transition region under  $V_{gs\_off} = 0V$ . A new device design with source finger added in transition region is proposed in this work to enhance the avalanche robustness.

### Acknowledgments

This research was funded by grants from the key area research and development program of Guangdong Province (Grant No.2021B0101300005) and Key Technologies R&D Program of Guangdong Province (2019B010143001).

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