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Enhanced Device Performance with Vertical SiC Gate-All-Around Nanowire Power MOSFETs

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Abstract. SiC gate-all-around (GAA) nanowire (NW) MOSFET is one of the most promising device architecture for the next generation of SiC power MOSFETs. This work reveals the great application potential of vertical SiC GAA NW power MOSFETs via TCAD simulation. The investigated devices show higher channel electron mobility (μ_{ch}) and larger channel carrier density (n_{ch}) compared to the conventional SiC power MOSFET. Scaling down of NW diameter (D_{NW}) is beneficial in terms of both, lowering channel resistance (R_{ch}) via improving n_{ch} and, increasing breakdown voltage (V_b) by modifying electric field distribution. Low specific-on resistance ($R_{on,sp}$) of about 0.68 mΩ·cm^2 for 1 kV SiC MOSFET is shown possible. However, scaling down the D_{NW} below 100 nm causes undesirable increase in $R_{on,sp}$ due to the unscalable device area which is limited by the vertical gate wrapping stacks. The study on device scaling where the NW diameter (D_{NW}) varies from 500 nm to 25 nm provides valuable design considerations for the device performance. Finally, a top-down process has been developed for the device fabrication. Vertical SiC NWs with aspect ratio of 10 are formed by an optimized micro-trench free dry etching process.

Introduction

SiC power electronics entered the market as the most promising candidate for high power and high voltage applications due to its superior intrinsic properties over Si devices regarding larger breakdown field, higher electron saturation velocity and higher thermal conductance [1]. However, SiC metal-oxide-semiconductor field-effect transistors (MOSFETs) suffer from high channel resistance due to low channel free electron density (n_{ch}) and low channel electron mobility (μ_{ch}) as a result of high interface trap density (D_{it}) [2-4]. A lot of research efforts have been put into the improvement of μ_{ch}[5-7] by optimization of the dielectrics, including post-oxidation annealing at high temperature in nitric oxide (NO), nitrous oxide (N_2O), boron nitride (BN) and phosphoryl chloride ($POCl_3$) ambient. Still μ_{ch} is far beyond SiC bulk electron mobility (μ_b).

Gate-all-around (GAA) nanowire (NW) [8, 9] is one of the most promising device architectures for the next generation of MOSFETs. Recently, multi-gate SiC FinFETs have been published [10-12], showing advantages of scaled device architecture. A 3D and cross-sectional schematics of a vertical SiC GAA NW MOSFET design used in the present TCAD simulations is illustrated in Fig. 1 (a) and (b), respectively. Fig. 1 (c) is the 3D schematic of a conventional SiC MOSFET. The GAA NW devices exhibit higher μ_{ch} and higher inversion channel electron density compared to that of the conventional devices. The higher mobility is due to the lower electric field in SiC NWs. Thus, a lower channel resistance (R_{ch}) is obtained for vertical SiC GAA NW MOSFETs.

The study on device scaling where the NW diameter (D_{NW}) varies from 300 nm to 25 nm provides few design considerations for performance improvement. By scaling of D_{NW}, both gate oxide and gate electrode thicknesses remain constant, here both are 50 nm. The cell pitch and the devices area are thus described as (D_{NW} + 200) nm and (D_{NW} + 200)^2 nm^2, respectively. For the simulation a maximum D_{it} of 9.5×10^{13} cm^{-2}eV^{-1} is considered to match the real situation at the SiC/SiO_2 interface. Schockley-Read-Hall (SRH) recombination with doping and temperature dependency, anisotropic

mobility model, anisotropic avalanche model, Auger recombination model and bandgap narrowing model (Slotboom) are taken into account for electrical simulations of the devices.

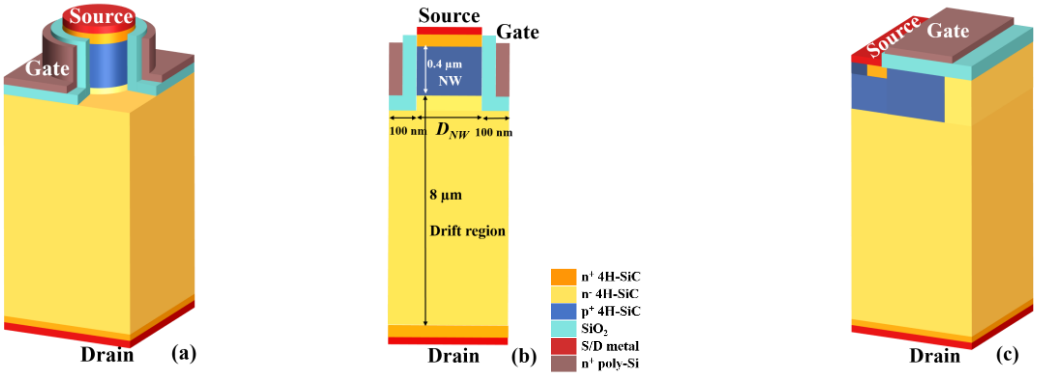

Fig. 1. (a) Three-dimensional and (b) cross-sectional schematics of a vertical SiC GAA NW MOSFET. The NW channel and the drift region are p-type (1×10^{17} cm^{-3}) and n-type (1×10^{16} cm^{-3}) doped, respectively. (c) A conventional SiC MOSFET is also shown as a reference. All the structural parameters are set as the same as in (b) for the two devices during the simulation.

Results and Discussion

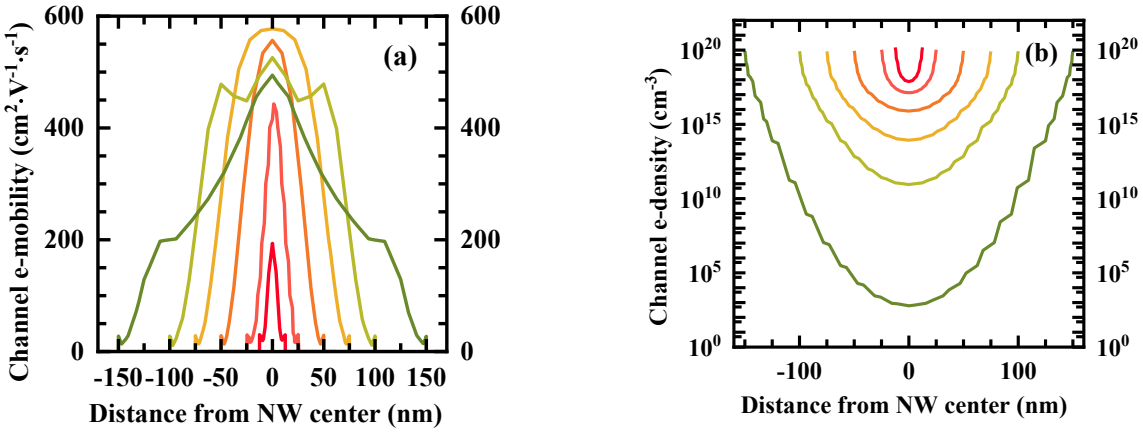

Fig. 2. (a) Channel electron mobility and (b) electron density distributions in NWs as function of D_{NW} from 300 nm to 25 nm. A gate bias of (V_{th} + 10) V is applied to turn on the devices.

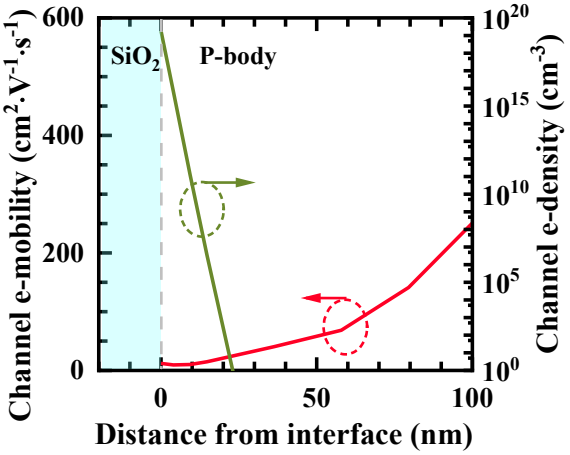

Fig. 3. Channel electron mobility and electron density of a conventional SiC MOSFET.

The simulated channel electron mobility and electron density as a function of NW dimeter, D_{NW} are shown in Fig. 2 (a) and (b). As D_{NW} reduces to 150 nm, μ_{ch} reaches a maximum value of 570 $cm^2V^{-1}s^{-1}$ at the NW center. The corresponding n_{ch} in the NW center is 1×10^{14} cm^{-3}. Both values are much higher than that of the conventional device in the same distance from SiC/SiO_2 interface, 100 $cm^2V^{-1}s^{-1}$ and 7.7×10^{-31} cm^{-3}, respectively, as shown in Fig. 3. A volume inversion is observed for a D_{NW}<100nm. However, the scaling down of D_{NW} to <100nm leads to a decrease of electron mobility in NW center, associated with electric field increase.

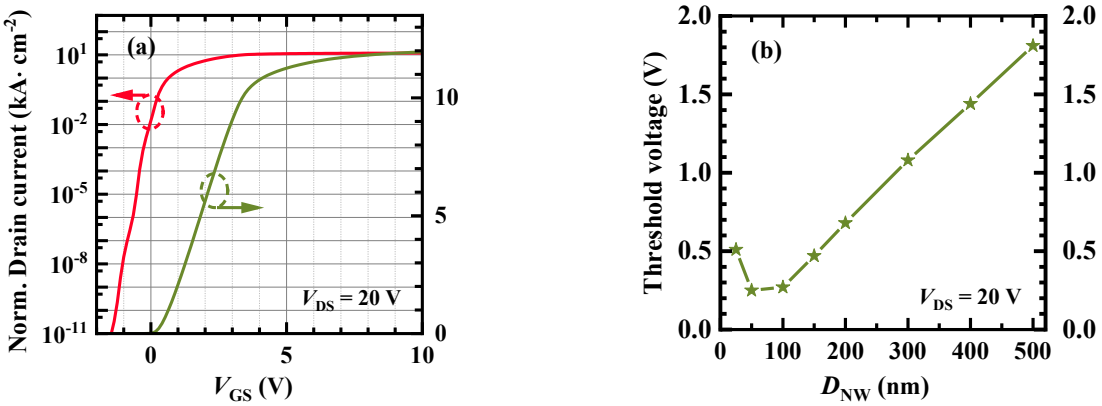

Fig. 4. (a) Transfer characteristics for a vertical SiC GAA MOSFET with D_{NW} of 150 nm in both linear and logarithmic scale. (b) The extracted V_{th} versus D_{NW} of the devices.

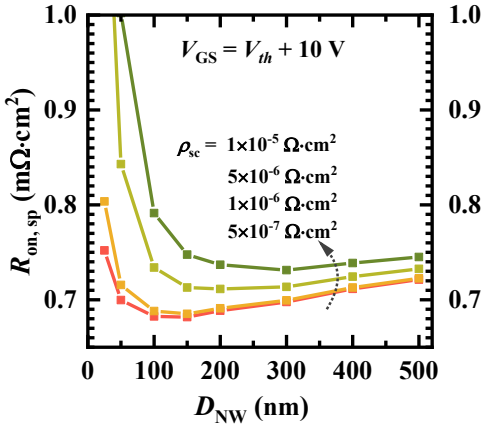

Fig. 5. $R_{on,sp}$ versus D_{NW} of the devices with ρ_{sc} from 5×10^{-7} Ω·cm^2 to 1×10^{-5} Ω·cm^2.

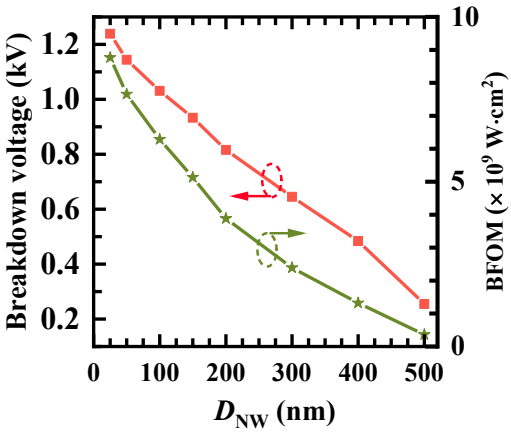

Fig. 6. Dependences of breakdown voltage and BFOM on D_{NW} at gate voltage V_{GS} = 0 V.

The transfer characteristics of a vertical SiC GAA NW MOSFET with a D_{NW} of 150 nm are shown in Fig. 4 (a) in both linear and logarithmic scale. The current is normalized to the device area using $(200 + D_{NW})^2$ nm^2 and considering a constant pitch size of 200 nm between NWs. The pitch size scalability is limited by the gate oxide thickness (here 50 nm SiO_2) and the metal gate thickness. The improved electrostatics of GAA NW device are evidenced by the very low off-current and a subthreshold swing (SS) of 160 mV/decade. The threshold voltage (V_{th}), shown in Fig. 4 (b), decreases from 1.8 V to 0.25 V when the D_{NW} scales from 500 nm to 50 nm. Further scaling down to 25 nm causes a slight V_{th} increase to 0.51 V. The dependence of specific on-resistance ($R_{on,sp}$) on D_{NW} is presented in Fig. 5 after considering of source contact resistivity (ρ_{sc}) from 5×10^{-7} Ω·cm^2 to 1×10^{-5} Ω·cm^2. We have to point out that the scaling of NW cause a high contact resistance at the source. This can be solved by enlarging the diameter of the top NW to increase the contact area while keep the channel with a smaller diameter. The minimum $R_{on,sp}$ of approximate 0.68 mΩ·cm^2 is obtained in the D_{NW} range between 100 nm and 300nm, depending on the value of ρ_{sc}. The higher ρ_{sc}, the larger minimum $R_{on,sp}$ and the corresponding optimal D_{NW}. Scaling D_{NW} below 100 nm results in dramatic

increase in $R_{on,sp}$ due to both extremely small source contact area and effective channel area compared to the pitch size. Indubitably, $R_{on,sp}$ for very small NWs can be further reduced by shrinking the peripheral area of SiC NWs, e.g. thinning gate oxide or gate electrode, but with the cost of higher gate leakage current.

Furthermore, scaling down the D_{NW} improves the off-state performance of the device. The breakdown voltage (V_b) and Baliga's figure-of merits (BFOM) [13] are increased by downscaling of D_{NW} (Fig. 6). A D_{NW} of 25 nm improves the V_b above 1.2 kV. For devices with larger D_{NW}, V_b can be improved by extending drift region or decreasing drift region doping concentration at the expense of increasing $R_{on,sp}$. Considering all the performance parameters, the device achieves optimum performance for NW diameter ranging from 100 to 200 nm which has advantage in processing feasibility. Based on the simulation data, vertical SiC GAA NW MOSFETs are presently under fabrication using a top-down process as shown in Fig. 7. Specific technology steps like SiC NWs patterning and micro-trench free etching processes have been successfully developed and tested. Fig. 8 shows, as an example, a SiC NW with a diameter of 35 nm and a height to width aspect ratio of ~10.

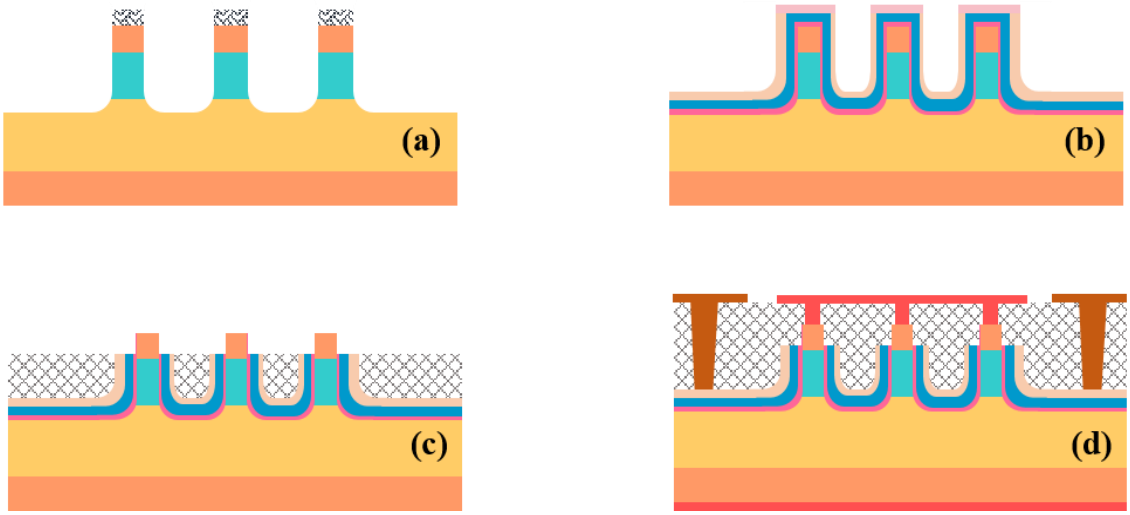

Fig. 7. A top-down process for fabrication of vertical SiC GAA NW MOSFETs. (a) NW etching by dry etching, (b) gate dielectrics and gate metal deposition, (c) planarization and top gate stacks removal, and (d) source, drain and gate contact formations.

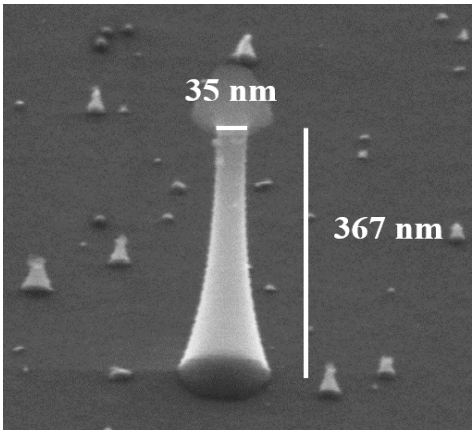

Fig. 8. SEM image of a vertical SiC NW formed by an optimized dry etching process.

Summary

The high inversion channel electron mobility and channel electron density indicate that GAA NW is a superior device architecture for SiC power MOSFET. A D_{NW} designing window of 100 nm to 200 nm is suggested to achieve high μ_{ch} and low $R_{on,sp}$. The maximum μ_{ch} in NW center, 570 $cm^2V^{-1}s^{-1}$, is obtained for D_{NW} =150 nm. Further down scale of D_{NW} results in undesired μ_{ch} decrease. In addition, when the D_{NW} is below 100 nm, the source contact resistance becomes the most significant factor in increasing $R_{on,sp}$ due to the extremely small contact area and the small effective channel area. For device with a D_{NW} of 100 nm, V_b, $R_{on,sp}$ and BFOM are 1 kV, 0.68 $m\Omega \cdot cm^2$ and 7.65 × 10^{19} $W \cdot cm^2$, respectively. Finally, a top-down process with an optimized micro-trench free dry etching process has been developed for the device fabrication. A high conduct can be achieved by fabricating NW array. As an illustration, 1 A current can be conducted by an array of 47600 100nm NWs.

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