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Suppression of Short Channel Effects for a SiC MOSFET Based on the S-MOS Cell Concept

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Abstract. This paper investigates the short channel effects (SCE) of the recently proposed Singular Point Source MOS (S-MOS) SiC MOSFET. The study was carried out using 2D and 3D TCAD simulations for a planar, trench and S-MOS 1200V SiC MOSFETs for the IV output characteristics up to 1200V and under short circuit transient conditions. The S-MOS device shows no SCE up to the rated voltage when compared to reference planar and trench devices which exhibit strong SCE. This is due to the appropriate P++ protection of the N++ source and the electric field shielding due to the narrow mesa dimensions between orthogonal trenches where the channel is located.

Introduction

State-of-the-art planar and trench gate SiC MOSFETs provide near ideal device performance with low losses and high temperature capability [1]. However, both planar and trench SiC MOSFETs are still prone to suffer from short channel effects (SCE) [2][3], which lead to performance drawbacks such as lowering the short circuit capability and restricting further design improvements for reducing the device losses. A new "Singular Point Source" MOS cell concept (S-MOS) was proposed for a 1200V SiC MOSFET by means of 3D-TCAD simulations [4] using Silvaco. In this paper, we provide more insight into the S-MOS design impact on the SCE and the potential performance improvements the S-MOS concept can provide for next generation devices.

S-MOS Device Concept

The S-MOS combines design and process features from Planar, Trench and FINFET MOS cell concepts while at the same time providing a unique way to achieve very high cell densities for MOS based power devices. The MOS structures for planar, trench and S-MOS are shown in Fig. 1 below.

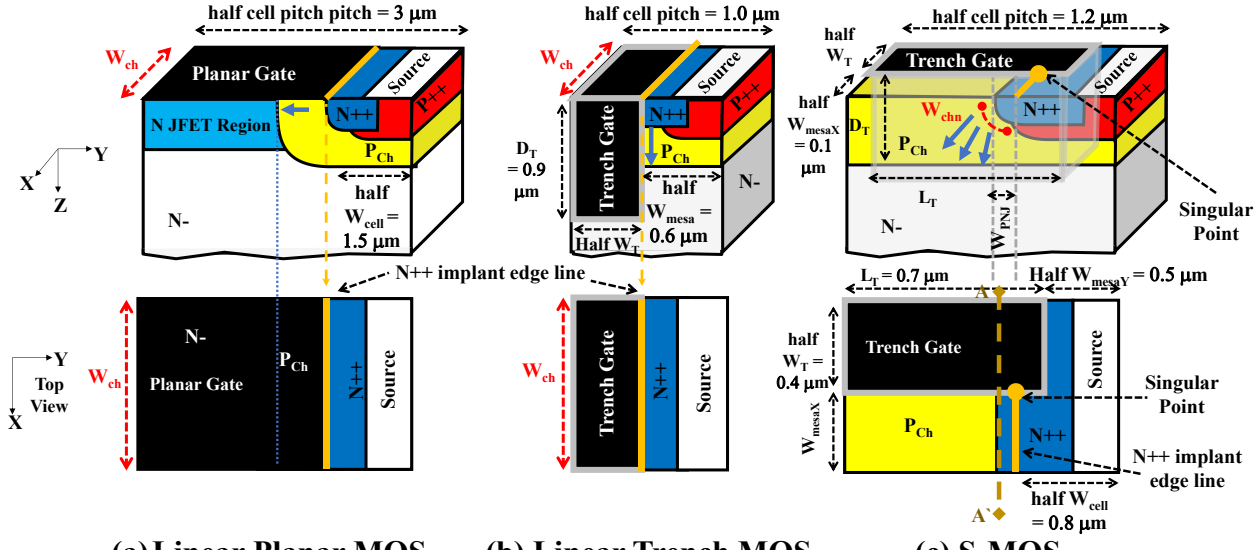


Fig. 1 MOS cell concepts including dimensions for planar MOS (a), Trench MOS (b) and S-MOS (c).

While the established design platforms rely on photolithography mask dimensions to define the channel area / cell density, the S-MOS 3D architecture relies on a singular point source implant position on a trench side-wall for defining and adjusting the channel density. Other key S-MOS structural features are the absence of a vertical channel and a fully shielded N++ source positioned between adjacent trench gate regions. Previous results show that the S-MOS can provide low R_{dson} along with low switching losses. In addition, improved IV output curves were observed where the S-MOS show a flat saturation current compared to a continuously rising drain current for both the reference planar and trench SiC MOSFETs. It is well known that such behaviour is directly related to the SCE in MOSFETs. These characteristics were not investigated further in the previous work.

1200V SiC MOSFET Simulation Models and Electrical Results

1200 V SiC MOSFETs were modelled based on the structures shown in Fig. 1. All devices had a total thickness = 10 µm, N-drift doping = $8x10^{15}$ /cm^3, N++ drain depth =1 µm and doping =$1x10^{20}$ /cm^3. The trench gate oxide thickness = 50 nm while for the planar = 100 nm to reduce the saturation current. The $P_{Channel}$ doping profile was adjusted to obtain the required saturation current and blocking capability above 1400 V. The doping concentration for the N++ source and P++ base = $1x10^{20}$ /cm^3 and $1x10^{19}$ /cm^3 respectively. All dimensions are shown on the different structures. The output IV curves (scaled to 1 cm^2) up to 1200 V at 150 °C and V_{gs} = 15 V are shown in Fig. 2. A zoom-in is provided up to 3.0 V for assessing the conduction losses while also providing the total switching losses under nominal conditions at 600 V, 100 A/cm^2 and 150°C. Fig. 3 shows the short circuit waveforms for both the S-MOS and Trench devices at 600 V, 150 °C and V_{gs} = 15 V.

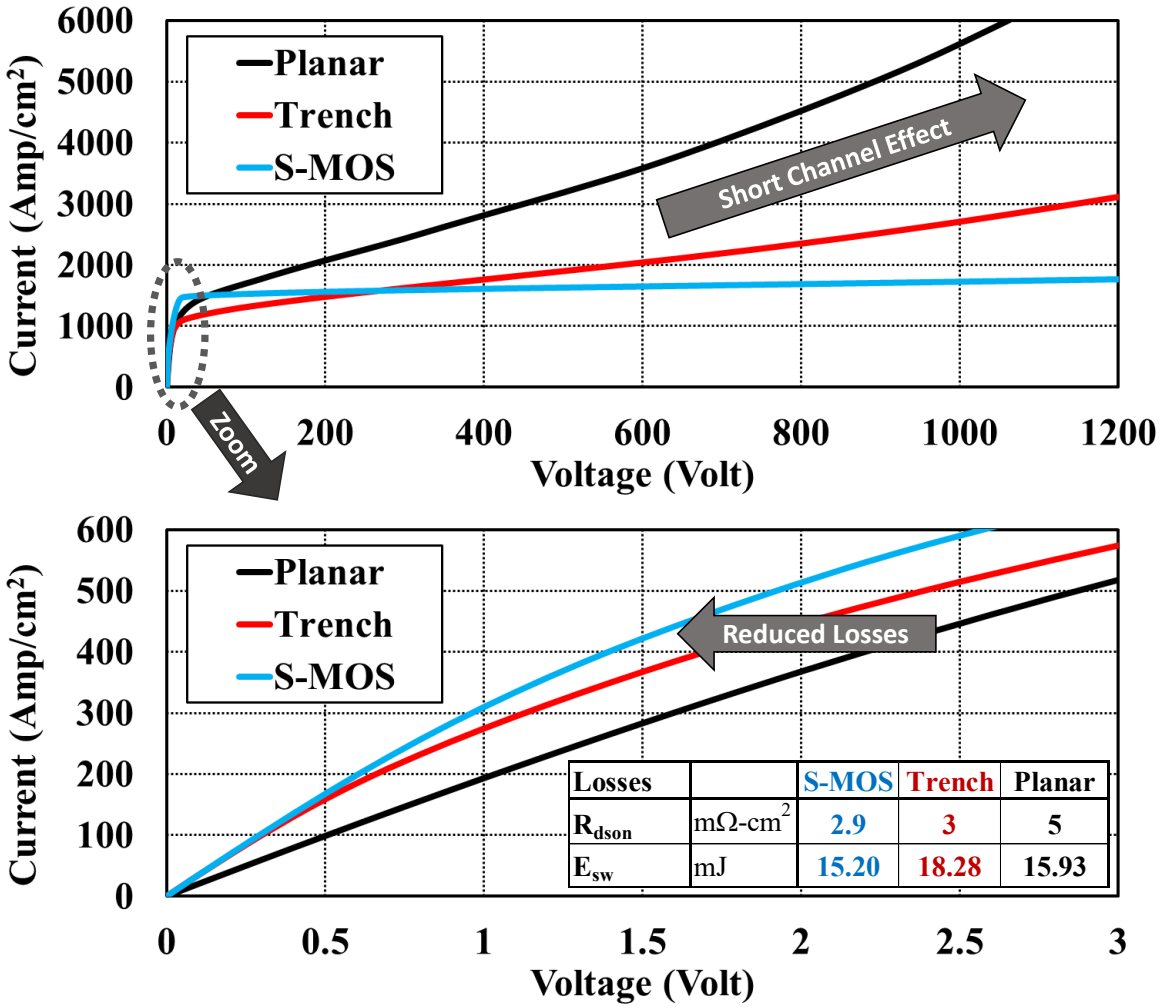


Fig. 2 1200V SiC MOSFET IV output curves at V_{gs} = 15 V at 150 °C (losses are shown in table).

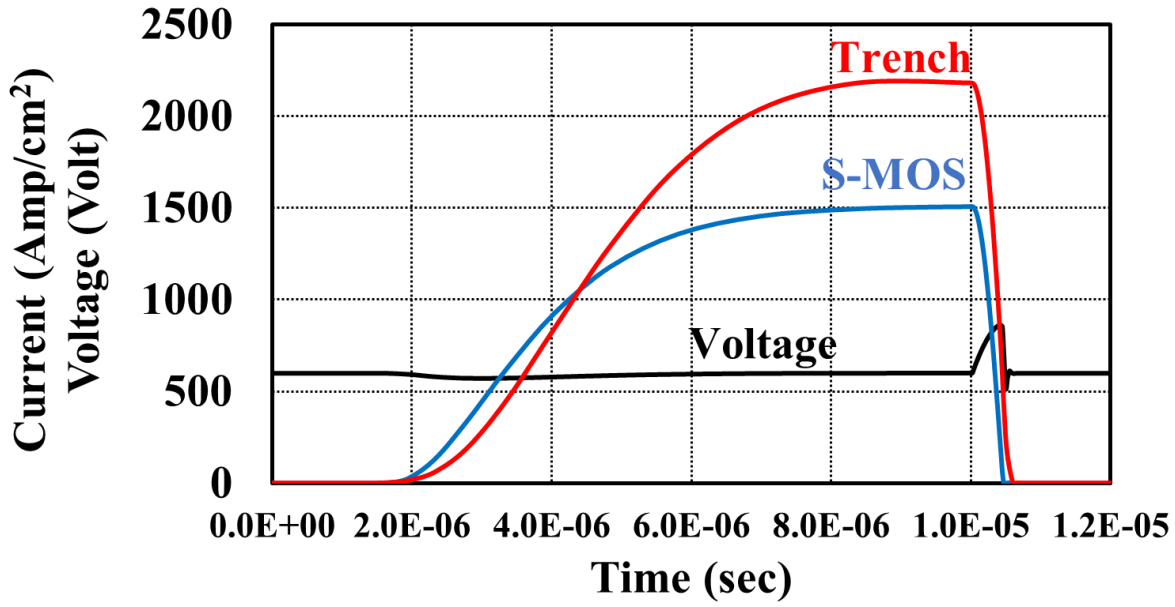


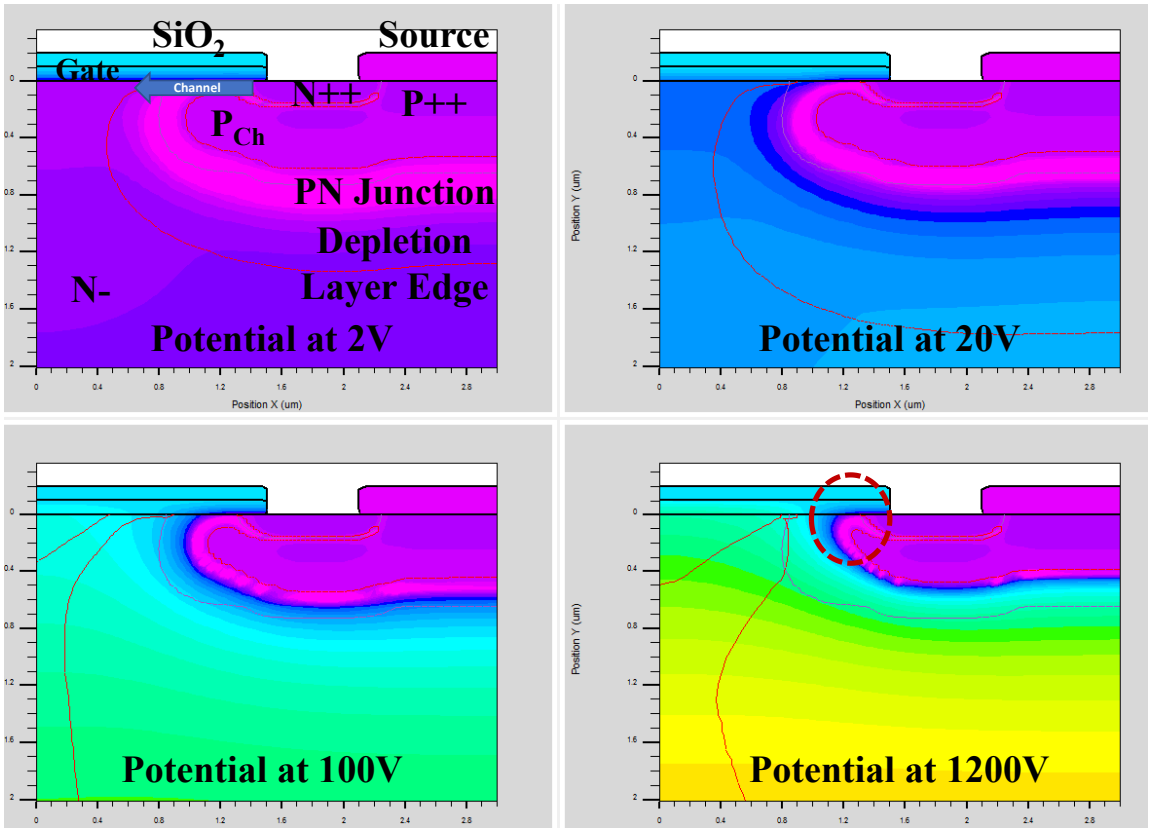
Fig. 3 1200V SiC MOSFET short circuit waveforms at 600V, V_{gs} = 15 V, 150 °C.

Reference devices show a pronounced Drain Induced Barrier Lowering (DIBL) effect due to an SCE leading to increased saturation currents with an increasing V_{ds}. This results in a higher and V_{ds} dependent short circuit current which must be taken into account for the circuit protection. Typical protection against DIPL using P+ shielding in such devices could lead to an increased JFET effect and high R_{dson} levels. On the other hand, the S-MOS shows lower losses while having a flat saturation current which is evidently due to a reduced SCE. Fig. 3 show a lower short circuit current for the S-MOS at 600V compared to the trench which leads to better design and performance trade-offs especially for next generation SiC MOSFETs with increased current density ratings (for 1200 V potentially reaching beyond 600 A/cm^2).

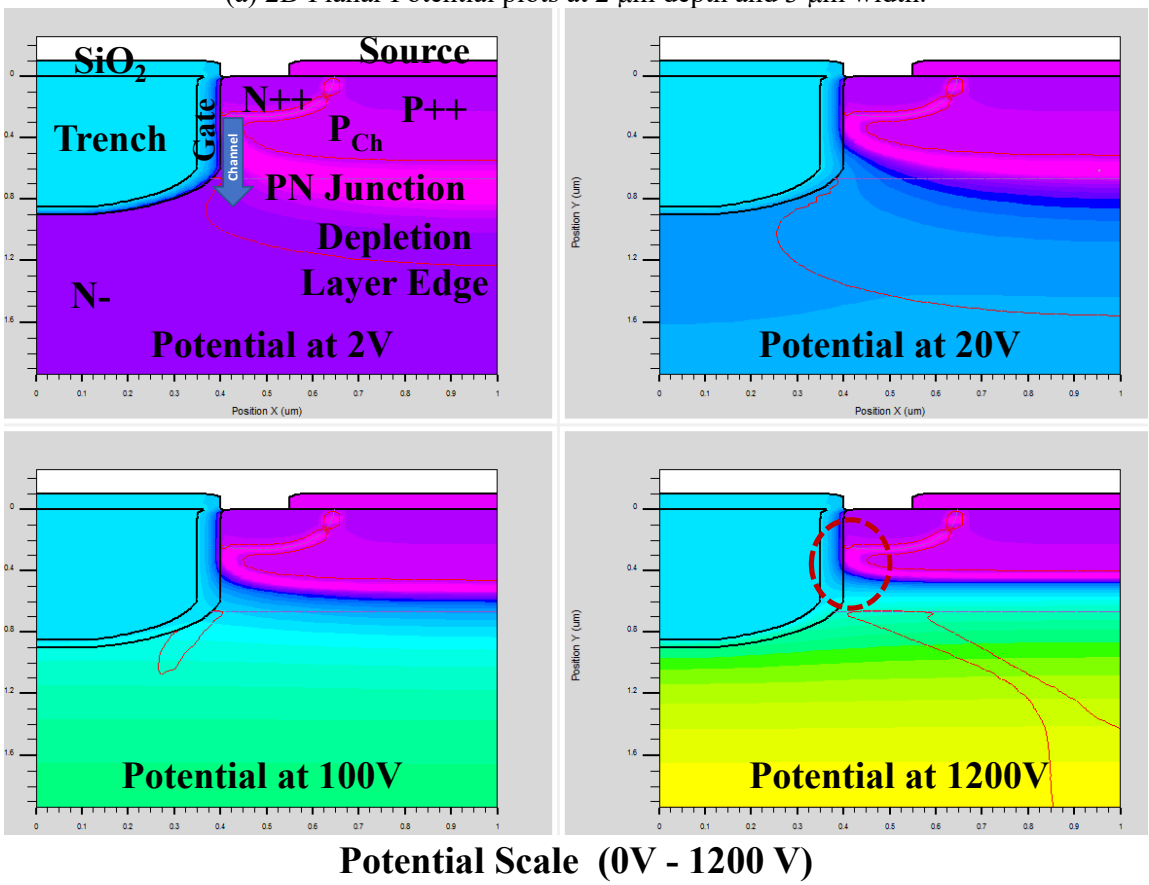
Analysis and Discussion

To carry out analysis of the structural design factors leading to a much-reduced SCE in an S-MOS cell, simulation model plots were obtained for the device at 2 V, 20 V, 100 V and 1200V for the output curves shown in Fig. 2 at 150 °C. Fig. 4 shows the 2D device POTENTIAL plots for the planar (a) and trench (b) device models at the previously mentioned voltages. The S-MOS 3D POTENTIAL plots are shown in Fig. 5a. A XZ cut-plane on the trench side-wall for the 3D plots are shown in Fig. 5b. The potential is plotted along the channel path depicted by an arrow in the 2D plots for the planar, trench and S-MOS devices at 2 V, 20 V, 100 V, 1200 V as shown in Fig. 6. The plots show that the planar device suffer from SCE with a clear shift in value for the potential curve from the P_{Ch} /N- junction towards the N++/P_{Ch} junction especially with increasing drain-source voltage levels up to 1200 V. This naturally is manifestoed in nearly a four-fold increase in saturation current levels between 100 V up to 1200 V. The SCE is also clearly visible in the 2D plot in Fig. 4 at 1200 V. On the other hand, the trench shows a much lower SCE but still substantial as demonstrated in the IV output curves when the voltage is increasing from 100 V up to 1200 V.

The S-MOS potential was plotted at the shortest channel path on the trench side-wall from the N++ source to the P_{Ch} /N- junction. Despite having a shorter channel, the potential plots show negligible potential shifts in value along the full channel length especially between 100 V and 1200 V. This explains the flat saturation current levels in the IV output curves. The 2D and 3D plots of the S-MOS also show that the N++ source remains protected with low potential levels in the vicinity of the N++/P_{Ch} junction.

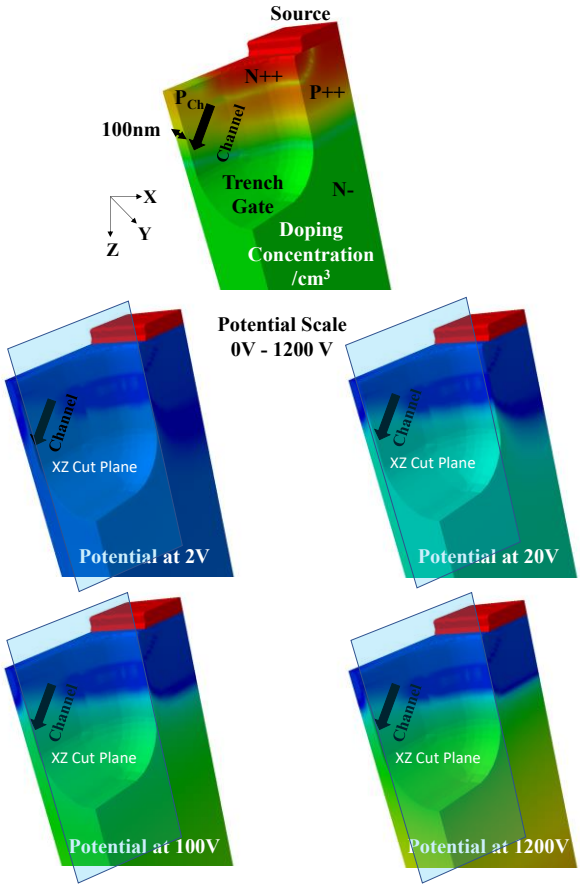


(a) 2D Planar Potential plots at 2 μm depth and 3 μm width.

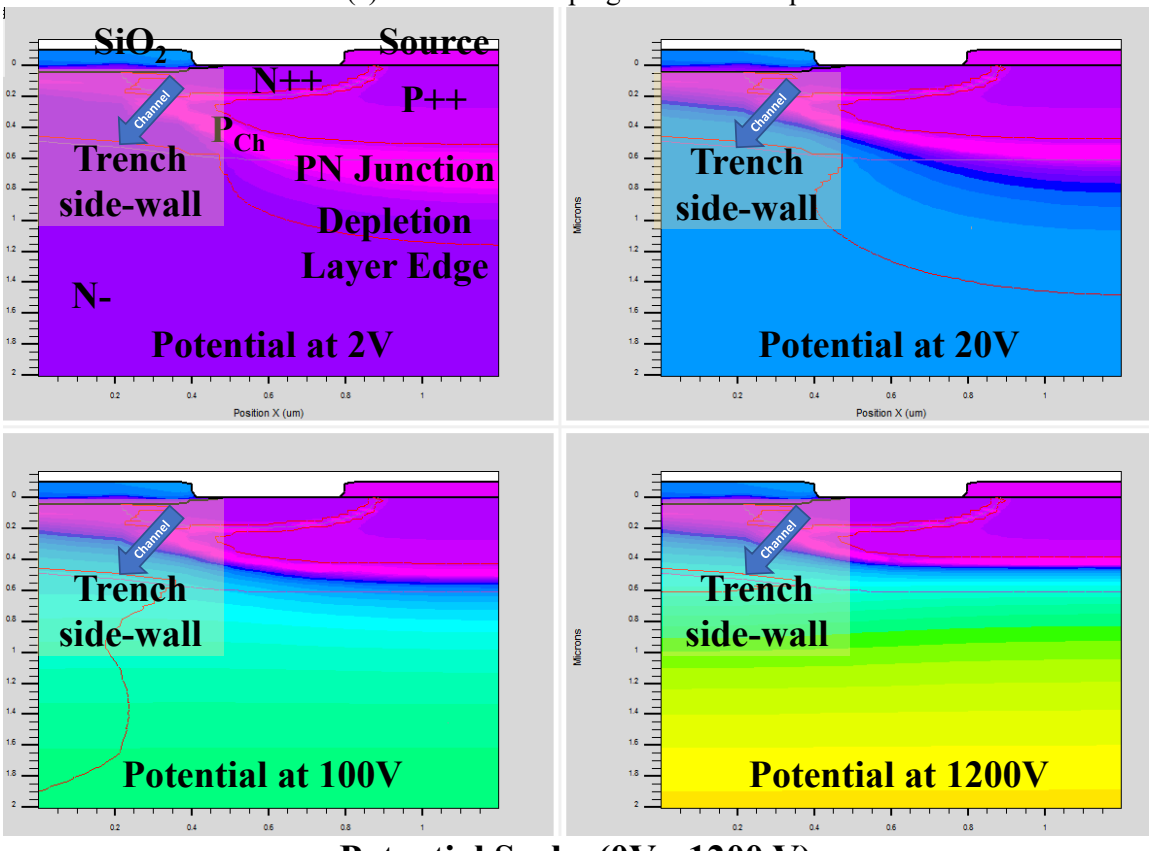


(b) 2D Trench Potential plots at 2 μm depth and 1 μm width.

Fig. 4 2D Planar (a) and Trench (b) potential plots of the 1200V SiC MOSFET at V_{ds}= 2 V, 20 V, 100 V, 1200 V at 150 °C.



(a) 3D S-MOS Doping and Potential plots.



(b) 2D S-MOS Potential plots XZ at at 2 μm depth and 1.2 μm width.

Fig. 5 3D (a) and 2D (b) potential plots of the S-MOS SiC MOSFET at V_{ds}= 2 V, 20V, 100 V, 1200 V at 150 °C (2D plot along the XZ cut-plane on the trench side-wall).

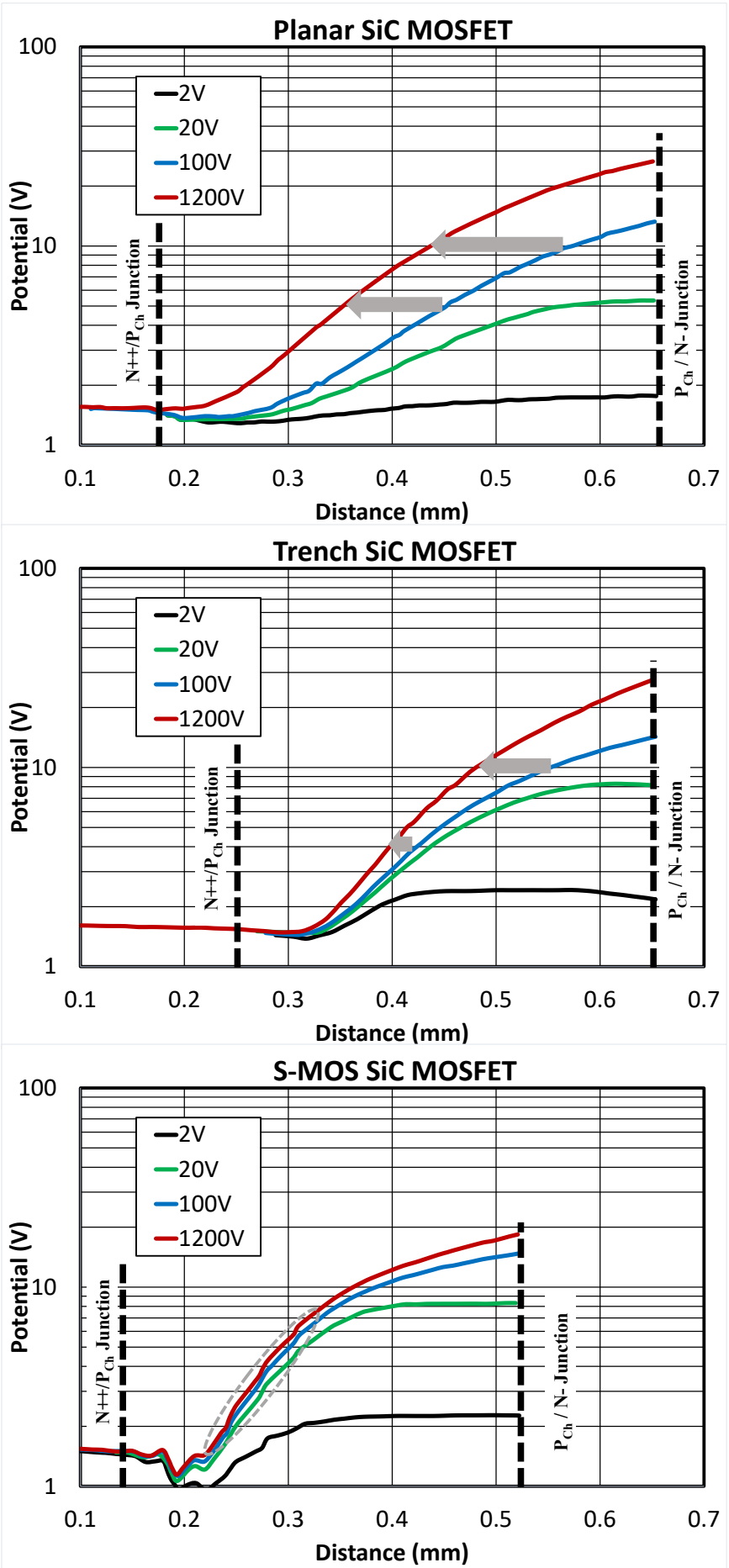


Fig. 6 Potential plotted along the channel for Planar, Trench and S-MOS SiC MOSFET at V_{ds}= 2 V, 20 V, 100 V, 1200 V and 150 °C.

The S-MOS has inherently two design features which lead to such advantageous characteristics. First, the channel has a shielding P++ region to protect the bottom edge of the N++ source region. Such design feature can be applied to planar devices but at the cost of increased losses and more complex processing. Secondly, the very narrow mesa between the two orthogonal trenches where the channel inversion layer is formed will provide another shielding effect as it leads to more gate control over the depletion layer spreading towards the inversion layer. This can be seen in the 3D S-MOS device sections in Fig. 7 for the doping, electric field and electron concentration from the IV output curves at 1200 V and 150 °C. The channel region is visible on the trench side-wall while the electric field shows a maximum value at the trench bottom.

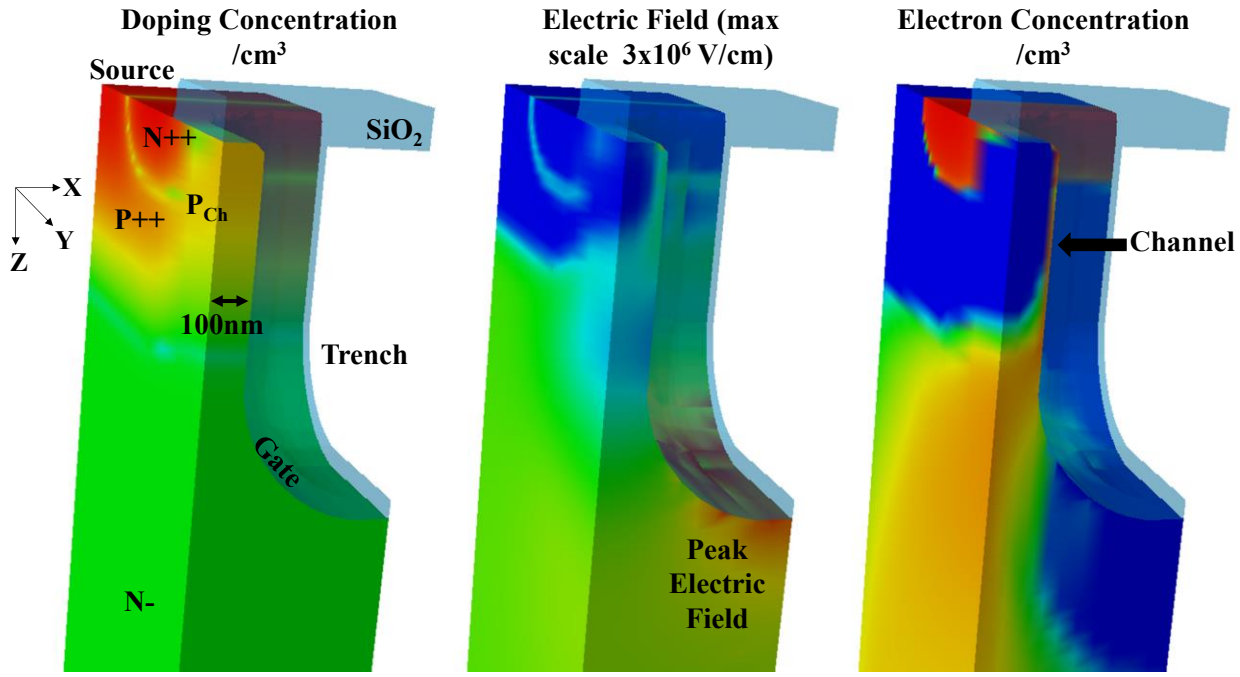


Fig. 7 3D S-MOS sections for doping concentration, electric field and electron concentration extracted from IV output curves at 1200 V.

Summary

The S-MOS device shows no short channel effect up to the rated voltage when compared to state-of-the-art planar and trench devices which exhibit strong SCE. This is due to the appropriate P++ protection of the N++ source region and the electric field shielding due to the narrow mesa dimensions between orthogonal trenches where the channel is located.

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