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Highly Efficient Floating Field Rings for SiC Power Electronic Devices - A Systematic Experimental Study

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Abstract. A systematic experimental study is conducted on floating field rings (FFR) incorporated into 4H-SiC junction barrier Schottky (JBS) diodes across four voltage ratings 650, 1200, 1700 and 3300V, in pursuit of highly efficient FFR designs. 30 designs of FFR in 3 categories are studied for each voltage rating, and the measured breakdown voltage (Vbr) of JBS divided by ring system width (W) is taken as the figure of merit (FOM) of each design. The influence of ring spacing, ring width and number of rings on Vbr is studied in detail. It is found that the initial ring spacing (S1) is critical in determining the highest Vbr achievable by a certain design, and its optimum value increases as voltage rating increases. TCAD simulation verifies the importance of S1. For designs with a small ring system width, subsequent ring spacing can also become important. Ring width does not have a definitive effect, and Vbr saturates beyond a certain ring number. The design with the highest Vbr may not render the highest FOM. Even style designs with appropriate ring spacings can be advantageous likely due to less susceptibility to variation of field oxide charge, and more tolerance to fabrication error, as well as ease of design.

Introduction

Semiconductor power devices feature high voltage blocking capability, primarily determined by avalanche breakdown of reverse biased junctions. However, premature breakdown occurs due to the shape of the actual junctions after processing, which is typically cylindrical instead of parallel planes, causing electric field crowding near the cylindrical part of the junction. The situation can be improved by using edge terminations. Traditional edge termination structures include floating field rings (FFR), field plates, junction termination extension, variation of lateral doping structure, and spiral junction termination [1], with FFR arguably the most practical and widely used termination [2]. FFR consists of isolated, heavily doped concentric rings surrounding the main junction or active area, working as a voltage divider at the surface, and minimizing the effect of curvature at the planar junction edges [3]. The rings can be conveniently formed at the same processing step as the main junction by diffusion or ion implantation through mask windows.

In recent years, SiC power devices have been gaining rapidly increasing attention due to the significant advantages over their Si counterparts in high power and high temperature applications based on their wide bandgap. For example, at the same doping concentration, the breakdown voltage of 4H-SiC can reach 67.4 times that of Si [4]. To guarantee high voltage and reliable operation, edge termination structures, quite often FFR, are indispensable in SiC devices. An efficient FFR design should meet several requirements: firstly, achieving high breakdown voltage (Vbr); secondly, maintaining small width of the ring system (W), which is the total width of the rings and their spacings, in order to reduce chip area so that more die can be laid out on a wafer. Thirdly, possessing process compatibility and reliability, which depends on oxide interface charge, packaging and the temperature [1] and tolerance to fabrication error. Moreover, when the device voltage rating changes,

FFR parameters need to change accordingly to retain high efficiency. In this work, we conduct a systematic experimental study to formulate general design guidelines and find highly efficient FFR designs for SiC devices with differing voltage ratings. Consequently, designers do not have to solely rely on simulations which tend to utilize theoretical models and deviate most of the time from the real results.

Designs of Floating Field Rings

To quantify the efficiency of FFR, we define the FFR figure of merit as the measured breakdown voltage (Vbr) of JBS divided by ring system width (W), i.e.

$$FOM = \frac{V_{br}}{W}. \quad (1)$$

A set of FFR has three basic (sets of) variables: ring widths (R), the spacings between two adjacent rings (S), and number of rings (N). There are various styles of FFR designs, such as i) constant R and S; ii) monotonically increasing S when the rings are farther away from the active area, in linear, quadratic, or other fashions, with constant or gradually increasing R [5]; iii) R and S divided in groups, where each group consists of several rings, and both R and S are constant within the group, but increase from one group to the next. The third type can be thought of as a combination of the first two.

In this work, 30 FFR designs have been implemented on JBS diodes for each voltage rating. The 30 designs are classified into 3 major categories: the first one has constant ring spacings (S=2, 2.5, 3, 3.25, or 3.5um) and ring widths (R=2 or 3um), with ring numbers N between 15 and 50 (even style, design labels starting with letters A, B, C, D, or G, example labels being A1, C5). The second one has S first increasing linearly, and then becoming constant (ramp style, with design label R1). R1 is the only ramp style. Specifically, it has a total of 15 rings, with ring spacing increasing from 1.2um to 1.8um at 0.1um intervals, and then staying constant at 1.8um for the last 9 rings. The last one has 2 to 4 groups, with spacings in the first group (S1) being 1.5, 2, or 2.5um, and increasing at intervals (Δs) of 0.1 or 0.5um from group to group (staircase style, design labels being F1 for Δs=0.1um, and starting with E for Δs =0.5um). Fig. 1 illustrates the ring spacing variation as ring number increases for the three categories. Tables 1 and 2 provide detailed information about the designs.

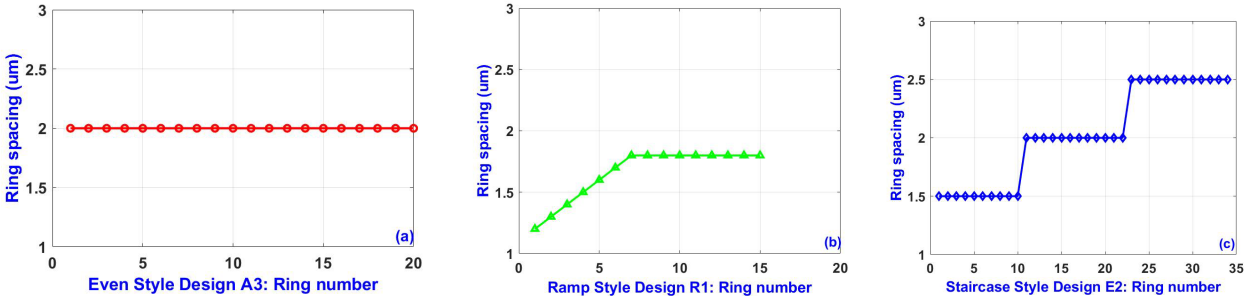

Fig. 1. Schematic of three major categories of FFR styles

Experiment

4H-SiC JBS diodes with voltage ratings of 650, 1200, 1700 and 3300V using Ti Schottky metal are fabricated. The Ohmic metal for front and back contacts is Ni silicide. Die size is 1.2mm*1.2mm. As voltage rating increases, epilayer dopant density (nitrogen) decreases, and layer thickness increases. The aforementioned 30 FFR designs have been applied to JBS diodes for each voltage rating. Breakdown voltage is measured with a FEC200E Diode Tester at 54uA for 650V devices, and 100uA for 1200V JBS. For 1700V and 3300V diodes, Vbr is read from an XJ4822 semiconductor device curve tracer. 10 diodes are measured for each design at each voltage rating. The average Vbr is taken for each design at each voltage rating.

Table 1. Design parameters of Even Style FFR

Design type	Ring width (um)	Ring spacing [um]	Labels	No. of Rings
A	2	2	A1-A5	15, 18, 20, 30, 50
B	2	2.5	B1-B4	15, 18, 20, 30
C	2 or 3	3	C1-C6	15, 15*, 20, 20*, 30, 50*
D	2	3.25	D1-D2	15, 24
G	2	3.5	G1-G2	15, 24

Note: Designs C2, C4 and C6 have ring width of 3um, as indicated by the *.

Table 2. Design parameters of Staircase style FFR

Design Label	Initial spacing S1 [um]	No. of groups	Ring width	Ring spacing
E1	1.5	3	2.5×10+3×12+3.5×3	1.5×10+2×12+2.5×3
E2	1.5	3	2.5×10+3×12+3.5×12	1.5×10+2×12+2.5×12
E3	2	2	3×12+3.5×12	2×12+2.5×12
E4	2	3	2.5×10+3×12+3.5×3	2×10+2.5×12+3×3
E5	2	3	2.5×10+3×12+3.5×12	2×10+2.5×12+3×12
E6	2.5	3	2.5×10+3×12+3.5×3	2.5×10+3×12+3.5×3
E7	2.5	3	2.5×10+3×12+3.5×8	2.5×10+3×12+3.5×8
E8	2.5	3	2.5×10+3×12+3.5×12	2.5×10+ 3×12+3.5×12
E9	2.5	4	2.5×10+3×12+3.5×12+4×5	2.5×10+ 3×12+3.5×12+4×5
F1	1.5	3	2×5+2×5+2×5	1.5×5+1.6×5+1.7×5

Note: Take E9 as an example, for ring width, 2.5×10+3×12+3.5×12+4×5 means there are 4 groups of rings: group 1 has 10 rings all with 2.5um ring width, group 2 has 12 rings all with 3 um ring width, and so on. For ring spacing, 2.5×10+ 3×12+3.5×12+4×5 denotes there are 4 groups of rings: group 1 has 10 rings all with 2.5um ring spacing, group 2 has 12 rings all with 3 um ring spacing, and so on.

Results and Discussion

The Importance of Initial Ring Spacing. Fig. 2 depicts Vbr vs. ring spacing S for all FFR designs at all voltage ratings. Each marker represents one of the 30 designs. For even style designs, S is constant, whereas for staircase designs, S means the first group ring spacing S1. The most obvious feature for all the four sub-figures is that for almost each voltage rating, there is an optimum initial ring spacing $S1_{op}$ rendering the highest possible Vbr. For 1200V through 3300V JBS, $S1_{op}$ is 1.5, 1.5 and 2um, respectively. For 650V JBS, $S1_{op}$ ties at 1.2 and 1.5um.

The existence of an optimum S1 is most obvious on Figs. 2 (b) and (c) for 1200V and 1700V JBS. Taking 1700V devices as an example, $S1_{op}$=1.5um, where Vbr peaks at 2450V for Design E2, with E1 slightly below E1. When S1 increases, Vbr drops rapidly. For instance, when S1=2um, the highest Vbr decreases to about 2180V for E3, and for S1=3.5um, the maximum Vbr degrades to around 1300V for G1. For all the designs with a certain S≥1.5um, even the design with the lowest Vbr beats the best design in the next group with a bigger S, even if the latter has significantly more rings, as highlighted by the red lines. This demonstrates that (the first group) ring spacing is the most important factor in determining Vbr, dominating ring number and other factors (such as ring spacings in subsequent groups for staircase designs). For staircase designs, the first group ring spacing is more important than those of other groups, probably because these rings are closer to the main junction (or active area), and thus have more influence on the electric field distribution at the main junction. The fact that there is an optimum value for S1 can probably be explained from two aspects: on the one hand, larger ring spacing makes pinch off from adjacent rings harder, making these rings less effective

in supporting voltage, and on the other hand, smaller ring spacing causes premature punch through between the rings, making the rings less efficacious. And for designs with the same S1, in most cases, Vbr clusters together with small differences given the measurement error, meaning that for even style designs, although the number of rings N varies, or for staircase designs, there are later groups of rings with bigger spacings, their influence is small, another evidence that S1 is the dominant factor for Vbr. F1 is an exception: although it has the optimum S1, its Vbr is the lowest among all 30 designs. This will be discussed later.

Similar trends are true for 650V and 1200V JBS, both of which also have E1 and E2 rendering the highest Vbr, except that for 650V diodes, there are two other designs tie with E1 and E2: F1 having the staircase style, which also has S1=1.5um, and R1 having a ramp style with S1=1.2um. Again, F1 is an anomaly for 1200V JBS: with the optimum S1, its Vbr is far below that of other designs in its own S1 group, and many designs in other groups.

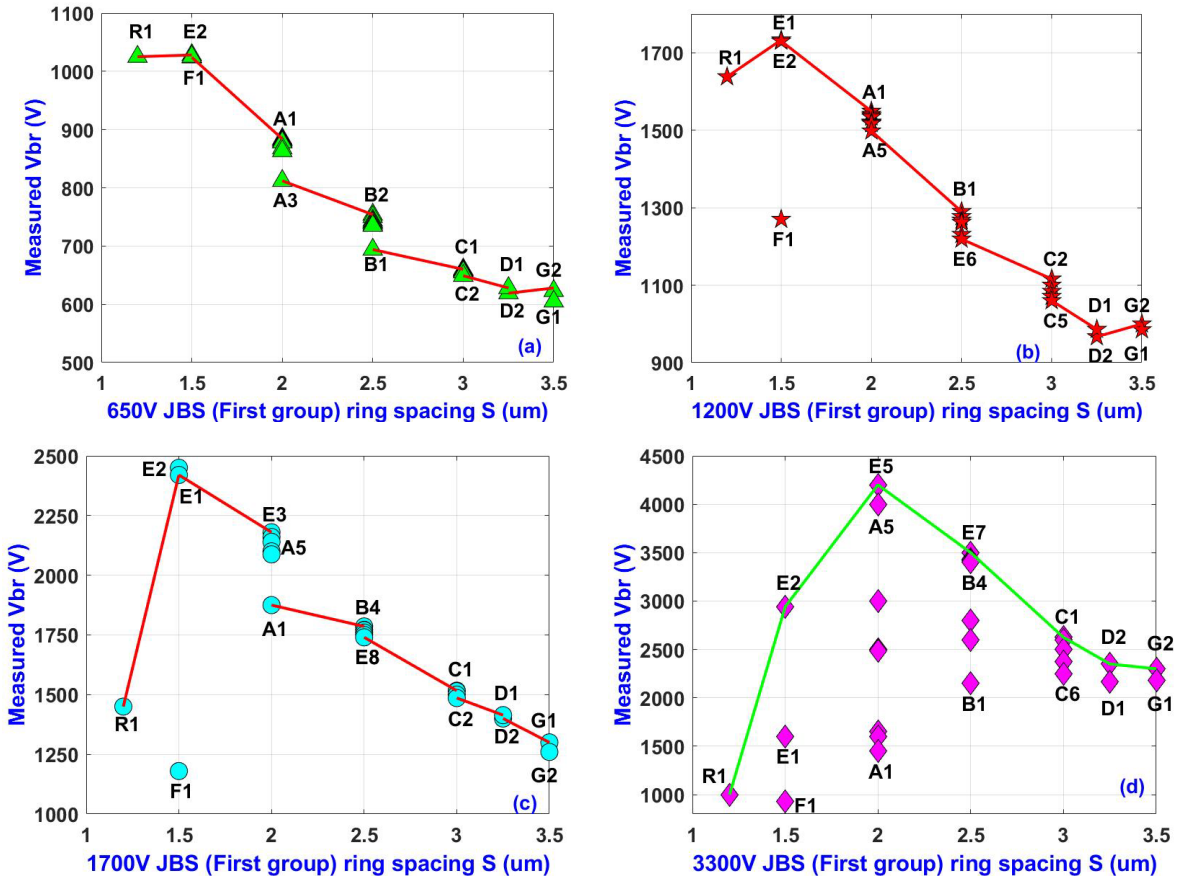

Fig. 2. Vbr vs (first group) ring spacing S. At a certain S, in most cases, only designs with the highest and lowest Vbr are labeled

Fig. 2(d) shows a more complicated picture for 3300V JBS. With the same S1, Vbr of different designs is more dispersed. It achieves the highest value at 4200V for Design E5 with the following parameters: R1=2.5um, S1=2um, N1=10; R2=3um, S2=2.5um, N2=12; R3=3.5um, S3=3um, N3=12, and W=189um. It is followed by Design A5 at Vbr=4000V with constant R=2um, S=2um, N=50, and W=200um. For S1≥2um, the outer envelope of Vbr, as shown by the green line, monotonically decreases as S1 increases, indicating that the highest Vbr that can potentially be reached by a certain S1 reduces with larger S1, similar to 1700V JBS for S1≥1.5um. Different from 1700V JBS, however, at a certain S1, the highest Vbr can still exceed Vbr accomplished by non-optimal designs (certainly the worst design) at a smaller S1. The fact that Vbr peaks at a bigger S1 for 3300V JBS than for JBS with lower voltage ratings is well expected, as the higher voltage rating necessitates a more lightly doped epitaxial layer with a bigger depletion width, and the pinch off distance increases. For a fixed

S1, the large dispersion of Vbr with different designs shows that the significance of S1 decreases, and the number of rings (and the ring spacing in subsequent groups) matters more compared to lower voltage ratings. Note that same as 1700V JBS, F1 has the lowest Vbr among all designs.

Influence of subsequent ring spacing. Although the initial ring spacing dominates Vbr, the subsequent (or ending) ring spacings can also play a role, and may become important when the total width of the ring system is small, as the rings are not far away from the main junction (or active area). This can be verified by examining the interesting performance of two designs, R1 and F1.

R1 is the only ramp style, and it has the smallest initial ring spacing of 1.2um among all the 30 designs, with a total of 15 rings. The ring spacing ramps up from 1.2um to 1.8um at a small increment of 0.1um, and then stays constant at 1.8um for the last 9 rings. The width of the ring system W is 55um, the second smallest among all designs. F1 has a staircase style, and it has the smallest final ring spacing of 1.7um among all the designs, also with a total of 15 rings. Specifically, F1 has 3 groups, each having 5 rings, with S1=1.5um, and the ring spacing increases at only 0.1um interval between adjacent groups, resulting in W=54um, the smallest of all designs. Incidentally, the 3rd smallest W is 60um for Design A1. For other designs, W increases at a relatively fast speed with ring number due to bigger ring spacing or faster increase of it.

For 3300V JBS, F1 has a Vbr below 1000V, the lowest among all 30 designs. This is not difficult to understand: for such a high voltage rating, big ring spacing is preferred. But F1 only has an S of 1.7um for the last 5 rings. R1 is slightly better, as it has 9 last rings with S=1.8um. For 1700V rating, both F1 and R1 obtain higher Vbr, because this rating needs a smaller ring spacing than required by 3300V devices. F1 is still the worst among all designs, and R1 behaves obviously better than F1. For 1200V rating, both F1 and R1 continue to rise in terms of absolute Vbr and their relative positioning among all designs. Now F1 beats a lot of designs, and R1 comes close to the best designs. For 650V rating, F1 and R1 tie with two type E designs in Vbr and simultaneously become the best designs, benefitting from their small ring spacings suitable for 650V. The improvement of the positioning of F1 and R1 among all designs as voltage rating continuously decreases vividly demonstrates the importance of subsequent ring spacings for designs with a small ring system width.

Influence of Ring Width. Among even style designs, there are only 3 with ring width of 3um, and all others have ring width of 2um. These 3 designs include C2 (N=15), C4 (N=20), C6 (N=50). C2 can be compared to C1 with the same S and N, but a narrower ring width. Similarly, the only difference between C4 and C3 is also the ring width. From Figs. 2(a) and 2(c), there is barely any difference between all Type C designs. Figs. 2(b) and 2(d) show that for Type C designs, fewer rings sometimes render slightly higher Vbr, likely due to measurement errors and some occasional bad die. No definitive difference in Vbr is found between C1 and C2, as well as C3 and C4, signifying that 2 and 3um ring width do not make a difference on Vbr.

Influence of Ring Number. It is found that for even style ring designs, when ring spacing is at or close to the optimum value, as ring number N increases, Vbr increases, and eventually saturates at a certain value, best illustrated by Fig. 3(a) for 1700V JBS. Consequently, when Vbr saturates, FOM keeps decreasing with N beacuse W keeps increasing. For comparison, for 3300V JBS, when N<50, Vbr of Type A design keeps increasing as N increases. It may saturate with even more rings. However, when the ring spacing is far away from the optimal value, increasing ring number renders insignificant change of Vbr, as can be seen from the clustered designs on Fig. 2 for the same S1. For staircase styels, within a certain group, similar relation exists between Vbr and number of rings.

Figure of Merit. As mentioned in the introduction, a good FFR design not only obtains high Vbr, but also maintains small ring system width, possesses tolerance to fabrication error, and has less susceptibility to process condition variation. Using the FOM defined earlier, and keeping in mind the quest for robust designs, Table 3 summarizes three classifications of designs across all voltage ratings: designs with the highest FOM and satisfactory Vbr (i.e. Vbr no less than 1.1 times the rated voltage), designs with the highest Vbr, and even style designs with highest FOM and satisfactory Vbr. Special

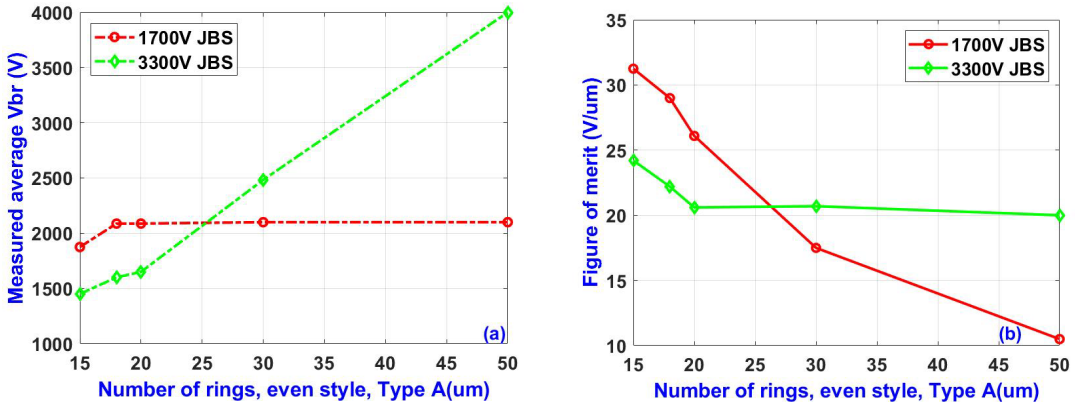

Fig. 3. Number of rings vs. Vbr and FOM for Type A designs at1700V and 3300V ratings

attention is paid to even style designs because we found that this type of designs seem to be more tolerant to change of fabrication environment or process variations. For example, Design R1 works well for 1200V JBS at Fraunhofer IISB in Germany, and often accomplished Vbr more than 1700V. However, when the same design was used at an external foundry for 1200V JBS with the same device design parameters, the results became unstable, and often failed to get 1200V. Ever since Design A1 was adopted at the foundry, Vbr has consistently exceeded 1500V for all the lots. According to Baliga, even style FFR can reduce the impact of variation in oxide charge [6], and hence more reliable. Furthermore, their ring spacing is relatively large and remains constant, and therefore less susceptible to fabrication errors compared to the ramp style R1 or staircase style F1, both having S increasing at 0.1um interval, which may be challenging to implement accurately. In addition, R1 also has a small starting ring spacing of 1.2um, which may not be as easy as larger spacing to realize precisely.

Table 3. Designs with the highest FOM, highest Vbr, and even style designs with the highest FOM

Voltage rating Vr (V)		**650**	**1200**	**1700**	**3300**
Designs with highest FOM and Vbr≥1.1*Vr	Design label	R1, F1	R1	A1	E5
	FOM [V/um]	19, 19	30	31	22
	Vbr [V]	1025	1638	1875	4200
	Ring system width [um]	55, 54	55	60	189
Designs with highest Vbr	Design label	R1,F1, E1, E2	E1, E2	E1, E2	E5
	FOM [V/um]	19, 19, 9, 6	15, 10	21, 14	22
	Vbr [V]	1025	1733	2420, 2450	4200
	Ring system width [um]	55, 54, 118, 172	118, 172	118, 172	189
Even style designs with highest FOM and Vbr≥1.1*Vr	Design label	A1	A1	A1	A5
	FOM [V/um]	15	26	31	20
	Vbr [V]	884	1549	1875	4000
	Ring system width [um]	60	60	60	200

Clearly, Type E designs acquire the highest Vbr for almost all voltage ratings, likely due to their extra freedom in choosing ring spacings: unlike an even style design which only has a fixed ring spacing, a staircase design has several ring spacings. Suppose the initial ring spacing is not big enough, the larger spacings in subsequent groups can partially compensate for it. Moreover, this type of designs also tend to have a large number of rings. In terms of FOM, the staircase style E5 excels for 3300V JBS, the even style A1 ranks the highest for 1700V, the ramp style R1 is the best for both 1200V and 650V devices, with R1 tying with staircase style F1 for 650V rating. For 1700V rating, Design A1 achieves a FOM of 31V/um, the highest across all voltage ratings among all designs.

Among all even style designs, A1 has the highest FOM for voltage ratings 650, 1200 and 1700V, and A5 is the best for 3300V JBS. Both designs have ring spacing of 2um. Although the even style designs may have Vbr below those designs with the highest FOM, or highest Vbr, their Vbr is sufficient, and their ring system width is close to those with the highest FOM.

Simulation

To better understand the significance of initial ring spacing, numerical simulation is performed using TCAD simulator Victory Device from Silvaco for 1700V JBS diodes with two FFR Designs: A3 and B3, both having 20 rings with 2um ring width, but differing spacing: 2um for A3, and 2.5um for B3. The measured Vbr is 2088V for A3 and 1786V for B3, and the simulated values are 2230V and 1890V, respectively. The less than 7% higher Vbr from simulation is reasonable considering that the oxide and nitride passivation is taken as ideal, a single implantation for the FFR is used to reduce simulation time, and the default materials database parameters are utilized. Simulation shows a Vbr difference of 340V between the two designs, close to the measured gap of 302V.

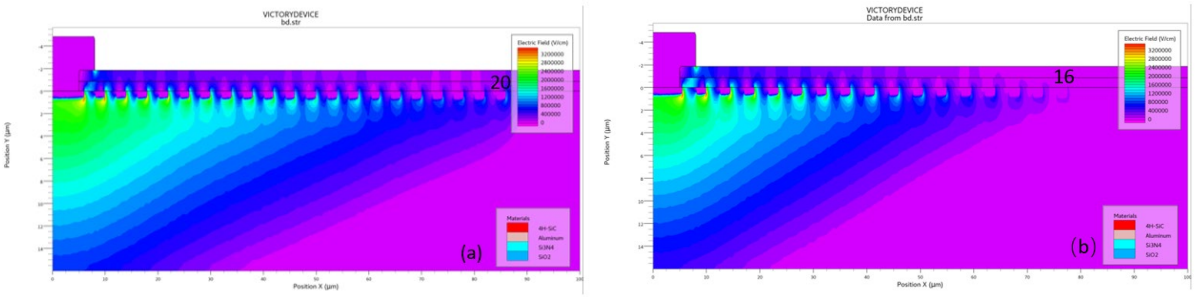

Fig. 4. 2D electric field distribution in edge termination region for JBS with FFR A3 (a) and B3 (b)

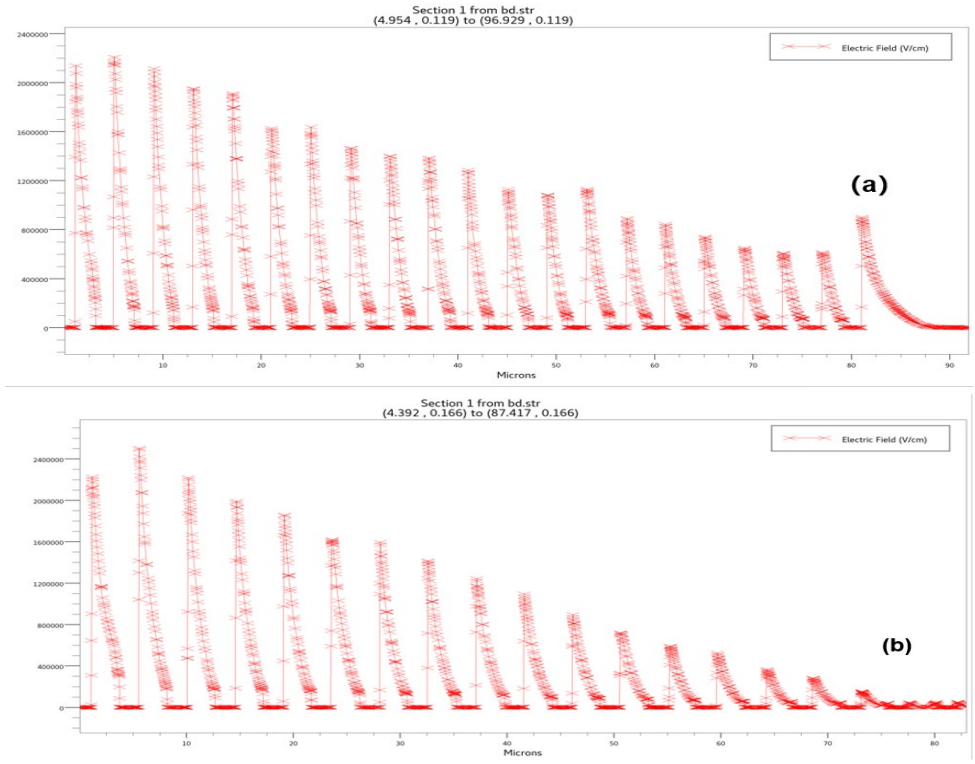

Fig. 5 Electric field profile along the surface in edge termination region for JBS with FFR A3 (a) and B3 (b).

Fig. 4 illustrates the 2D electric field distribution in the edge termination region on a cross section of the device integrated with FFR A3 and B3. Fig. 5 depicts the electric field profile along the surface of the device in the same region for JBS with the two aforementioned FFR designs.

Figs. 4 and 5 both display that the peak electric field decays along the rings going toward the edge of the die. In Fig. 5 (a), the highest peak is located at the 2nd ring spacing, measuring 2.2 MV/cm. Compared to Fig. 5 (b), peaks in Fig. 5 (a) decrease more slowly, and the very last peak has a field of 0.9 MV/cm, higher than those at the previous 6 rings. In Fig. 5 (b), the highest peak is 2.5MV/cm, also at the 2nd ring spacing, but the peak values decrease more rapidly, and at the 16th ring spacing from the active area, the field is already barely visible on the 2D figure 4 (b), where the 1D plot reads 0.3MV/cm. At the last 4 ring spacings, the field is almost 0, suggesting that these rings barely support any voltage drop. Undoubtedly, integration of the field in Fig. 5 (b) would render a higher Vbr.

Summary

Systematically designed 30 types of FFR in three major categories are studied experimentally in detail by implementing them on JBS didoes across 4 voltage ratings, in terms of Vbr and FFR efficiency quantified by Vbr divided by ring system width. It is found that the initial ring spacing is the most important factor in determining the highest Vbr potentially achievable by a certain design, and its optimum value increases as voltage rating increases. For designs with a small ring system width, subsequent ring spacing can be important as well. Ring width does not have definitive influence on Vbr. When ring spacing is at or close to the optimum value, as ring number increases, Vbr first increases, and eventually saturates. Staircase designs obtain the highest Vbr for all the voltage ratings, likely due to the extra freedom provided by their multiple ring spacings and large total number of rings. However, they often do not have the highest FOM. Design styles providing the highest FOM differ for different voltage ratings. Across all voltage ratings, the highest FOM is 31V/um, accomplished by Design A1 for 1700V devices. In addition to simplicity of design, even style designs may have the advantage of less susceptibility to variation of processing conditions and oxide charge, and more tolerance to fabrication errors. Among all even style designs, A1 with 2um ring spacing has the highest FOM for voltage ratings of 650, 1200 and 1700V, and A5, also with 2um ring spacing, is the best for 3300V JBS.

It is worth pointing out that all the results are dependent on the doping concentration of the epilayer, which is evidenced by the fact that when the voltage rating changes, the efficient FFR design changes accordingly. Similarly, while each voltage rating has a relatively small range of doping concentration to choose from, when epi doping changes, the best FFR design may also need to be tweaked to maintain high efficiency, but the design logic should still be valid. The principles found here are applicable to other types of power devices, such as MOSFET, IGBT, and other materials, for example, GaN and Si.

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