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Fabrication of an Open Gate-4H-SiC Junction Field Effect Transistor for Bio-Related and Chemical Sensing Applications

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Abstract. In this paper, a suitable process technology is employed to fabricate a new open-gate silicon carbide-based junction field-effect transistor (OG-4H-SiC-JFET) intended to be used for biochemical sensing applications. The main focus is dedicated to the fabrication steps and specifically the plasma etching of the SiC, as it is the key step to pattern the device components. All necessary I-V characteristics (I_{DS}-V_{DS} and I_{DS}-V_{GS}) have been derived showing acceptable electrical performance. Furthermore, the electrical characteristics of the OG-4H-SiC JFET were simulated using 3D Silvaco ATLAS and are in line with the experimental electrical characteristics. The efficacy and simplicity of the process described in this paper is the first step for the future development of bio- and chemical sensors based on SiC-FETs.

Introduction

Silicon is the leading material on which electronic transducers are realized and consequently, silicon technology was introduced in bio-chemical sensor production[1]. Field-effect transistors based on silicon as a CMOS-compatible device have been intensely developed over the last years and have proved to have major promise in label-free, real-time, selective and highly sensitive electrical measurements for bio-chemical sensing applications [1]–[6]. Biocompatibility is blocking the FET sensor devices from being adopted by biomedical applications and more specifically the in vivo sensors. The biocompatibility issue is not related to the FET itself but it is a general problem of the device material and encapsulation. The ready availability and low cost of Silicon (Si) have made it always the preferred substrate for the development of microdevices based on semiconductor materials (microelectronic devices). Ion Sensitive Field Effect Transistors (ISFETs) based on Si have been used as microchip-devices interfacing with living tissues or neuronal networks [7], [8]. Our group has compared the long-term stability of Si and SiC NWs under mimicked physiological conditions. The results emphasized a clear superior long-term stability of SiC nanowires over Si nanowires [9]. Therefore, the biomodification of SiC nanostructures and nanowires [10] has been investigated to perform the electrical detection of DNA hybridization on SiC NW-based FETs. SiC exhibits also enhanced biocompatibility proved by the absence of cytotoxic effects after interfacing with different mammalian cell cultures [11]. Moreover, it is easy to functionalize it in different ways due to the reactivity of the Si and C terminations on the surface. However, to further investigate the sensing performances of these devices, it is necessary to use optimized SiC-based FET devices with very well-suited intrinsic characteristics. The development of SiC-FET for biochemical sensing applications is presented in this work. The working principle of the device as a bio-chemical sensor is described based on the conventional FET sensing methods. The fabrication of the OG-4H-SiC-JFET is described in detail including all process steps, problems and solutions. The simulated electrical characteristics of the device are shown using the 3D ATLAS-SILVACO tool and compared with the electrical characteristics obtained experimentally.

The Device Expected Working Principle

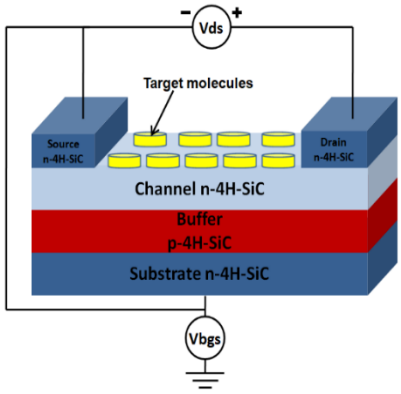


Figure 1. 3D schematic of the OG-4H-SiC-JFET, target charged molecules bound on the top of the silicon carbide channel results in the variation of the channel conduction

Fig. 1 shows the schematic cross-section representation of the investigated open gate microwire open gate 4H silicon carbide junction field effect transistor (OG-4H-SiC-JFET). The sensor works based on the conventional n-type JFET structure with an open front gate for introducing the electrolyte (sensing analyte). The n^- layer serves as the conduction channel between two ohmic contacted sources and drains regions. The total surface of the n^- layer (3 sides) can be covered with an oxide or any ion-sensitive material in the case of pH measurement and receptor biomolecules, DNA or antibodies for biosensor applications. The presence of the charges on the surface (positive or negative) results either in the accumulation of more electrons in the n-type SiC channel or carrier depletion which results in a shift of the transfer characteristic. The structure is suitable for many chemical and bio-related sensing applications and it is fabricated from 2x2 cm^2 4H-SiC samples as described in detail in a previous preliminary research work [12].

Device fabrication

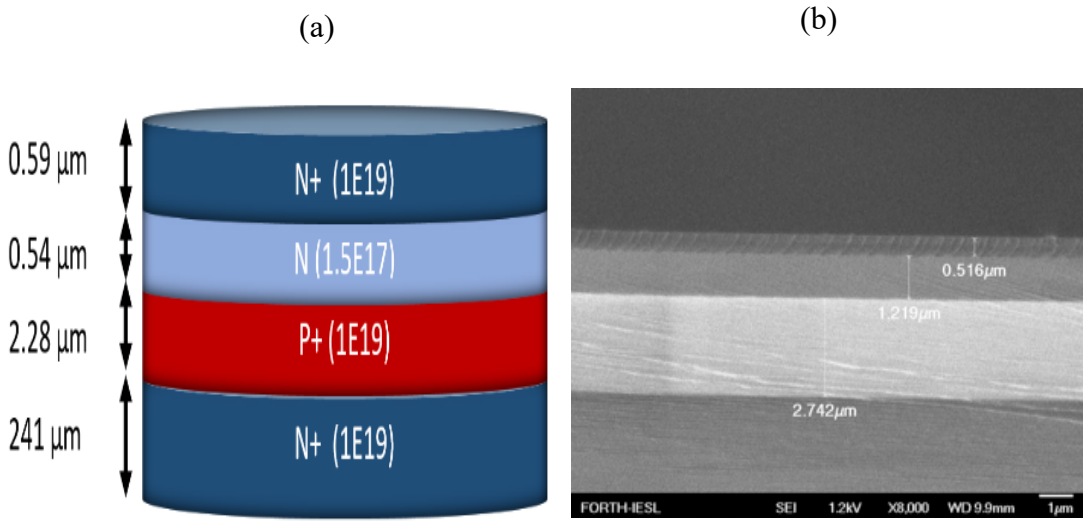


Figure 2. (a) Schematic of the epitaxial wafer showing doping concentration and thicknesses of the epilayers and (b) SEM cross section of NOVASIC epitaxial structure. The 0,5µm most top layer is a protective PR. Courtesy of FORTH

The device is fabricated from an epitaxial wafer and the regions (source/drain/channel/back-gate/mesa) are made from different layers of specific depth and doping (Fig. 2a). The fabrication of the OG-4H-SiC-JFET device is based on four main processing steps by using a mask set suitable for various types of biosensors (see [13]).

A Ni-based metal scheme both as plasma-etching-mask for the n^+ layer removal and as ohmic contact metallization for source/drain/interconnecting lines was imposed. In addition, a second metal scheme based on Al had to be employed to be used as a plasma-etching mask for the microwire-channel area definition. The process started with the first step which is the delimitation of the source and drain areas (Fig. 3). A Cr/Ni (10/100 nm) metal mask was patterned after reversal lithography and lift-off. The SiC n^+ layer was etched down to the n^- layer. The etching is made with RIE plasma in a CORIAL 200IL tool. A conventional etch recipe was used (provided by CORIAL technical support according to the used etching chamber) SF_6 100 sccm, O_2 6 sccm, Power 200 W, Pressure 50 mTorr, Temp 20°C, RF Bias 248.5 V. The etched depth was verified with a

profilometer and the measured etch rate is about 45 nm/min. No micromasking was observed on the etched surface. The second step is the delimitation of the channel area (Mask level 2) or patterning of the SiC-microwires was realized through a 100 nm Al metal mask (Fig. 4). The Al was chosen as an etch mask to guarantee the etch selectivity between Ni and Al, as we want to keep the Ni as a metal contact. The n^- layer was etched down to the surface of the p+ layer. The same etch recipe as the previous step was used. The Al mask used for the patterning of the SiC microwires should be removed at the end to leave the surface of the microwires (the channels) clean and ready for sensing function. Then, a commercialized Al-etch solution was utilized to etch the Al mask. However, a drastic etch of the Ni layer was observed. An alternative wet solution (5% KOH in an ultrasonic bath for 3min) resulted in better selectivity during the 100nm Al etch. The third step is the device annealing at 950°C for 2 min inside a rapid thermal annealing furnace from Jipelec JETFIRST to create the ohmic contact between the n^+ SiC and Ni. The annealing is happening after the RIE-etch steps to be sure about the integrity of Ni/Cr contacts. The fourth and last process fabrication step is the encapsulation of the device which is done with a SiO_2 passivation layer to isolate the metal contacts during aqueous sensing experiments and prevent short circuits through the solution (Fig. 5). A 600nm SiO_2 thick layer has been deposited by CORIAL PECVD. The deposition conditions are as follows SiH_4 35 sccm, N_2O 1000 sccm, Ar 500 sccm, working pressure 1800 mTorr, RF Power 250 W, Rate 5nm/s, Deposit time 100 s, deposit temperature 280°C.

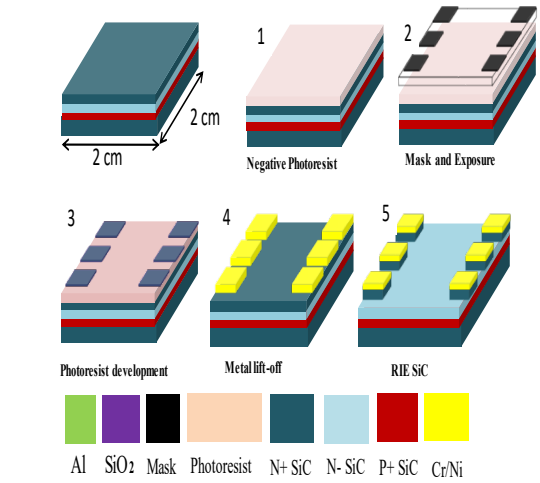


Figure 3. 3D schematic representation of the definition of the source/drain area from the top n^+ SiC layer (mask level 1) (the color code on the bottom of the graph applies to the following process)

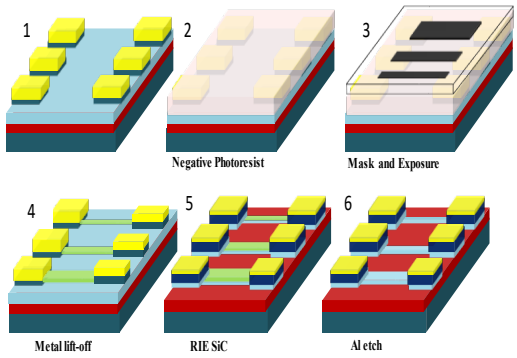


Figure 4. 3D schematic representation of the process fabrication step "definition of the SiC microwires" from the n^- layer (Mask level 2)

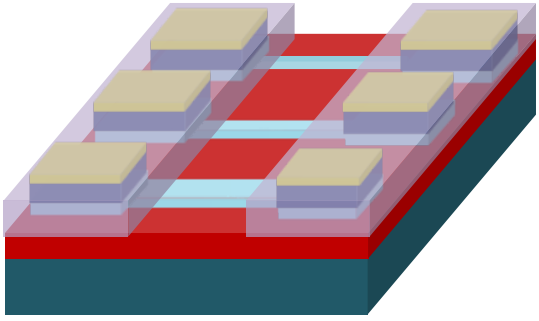


Figure 5. The final device with the areas covered with the passivation oxide (purple colour) for simplicity reasons only source and drain contacts localized on each SiC microwire extremity are shown, the metal lines are extended to the device edges as metal pads (metal pads are not covered with oxide allowing probing for electrical characterization, not shown on this figure)

To etch specific areas of the SiO_2 layer, we designed and printed a plastic/flexible mask for the photolithography. The resulting photoresist patterns realized with the plastic mask cover all the surface of the device except the microwire channel regions. The uncovered-with-photoresist SiO_2 areas were etched with a wet etching process using buffered HF (since the buffered HF is known for

not etching the photoresist). Fig. 5 shows the final architecture of the device. Table 1 resumes the designed and tested plasma-etch recipes by using Ni and Al masks which meet the needs (the non-presence of micro masking, high selectivity and vertical sidewalls). Considering that those recipes are created and tested specifically on the CORIAL 200IL, modifications of the parameters should be done in case using another RIE system (or chamber).

Ideally, the total depth of the p^+ SiC layer (depth 2.28 µm) should be also etched to create a mesa for each microwire device (separate channel) allowing the electrical isolation between the neighbouring devices. The depth of the p+ layer (2.28 µm) can be etched with the previously used etch recipe but the etch time will be more than 63 min (according to the measured etch rate). Thus, there is a need to test more efficient SiC etch recipes which guarantee an acceptable etch rate, the non-presence of micro masking (while using Ni or Al mask), high selectivity and vertical sidewalls. The selectivity is a primordial parameter to set before launching the device fabrication because the SiC and metal mask etch go in parallel and at least 100 nm thickness of the Ni mask should be kept till the end of the etch of the target total depth. In the case of SiC etch with Ni mask using recipe 1, the etch rate is 150 nm/min and the obtained selectivity is 40:1. Thus, since Ni mask is used to etch the SiC total depth of about 3410 nm (3500 nm) also the Ni mask is etched in parallel and the expected etched depth is about 94 nm (almost 100nm). Thus, 200 nm Ni should be deposited since 100 nm will be consumed during the SiC etching and 100 nm will be kept to form the ohmic contact with the n^+ SiC layer. Unlikely, since the thickness of the deposited Ni is high, problems of the photoresist peel-off appeared during the Cr/Ni evaporation. Fig. 6 illustrates the problem of the photoresist peel-off. The peel-off of the photoresist results in the deposition of the Ni in undesired areas. To avoid this problem, several tests were done with variable parameters. The Ni deposition rate was reduced from 0.5 nm/s to 0.2 nm/s, to reduce the stress on the photoresist during the metal evaporation. Also, the sample was heated to 70°C. Even with these modifications, the problem of the photoresist peel-off is not resolved. Fig. 7 shows the patterning of the device, the yellow lines are the areas where the photoresist is developed and metal is deposited (and remaining after the lift-off). One possible hypothesis here is, that as the line patterns are too close, this reduces the surface of the photoresist on those regions, which makes it more fragile and more sensitive to the stress during deposition. A possible solution is to change the layout of the metal contacts in a way they are spaced letting a bigger surface of the photoresist bounding on the SiC sample and instead of the sharp corner of the metal lines, rounded shapes are used. For sake of simplicity and to avoid the production of a new photolithography Mask, laser lithography in which only GDS files are required (i.e. no mask use) is adopted. Thus, metal lines are designed in a way that the mechanical stress that the photoresist receives during the metal evaporation is avoided. Fig. 8 shows the new metal lines layout (level 1). Ni/Cr was evaporated after finishing with the laser

Figure 6. Phototresist peeled-off from the surface of the SiC during Cr/Ni evaporation

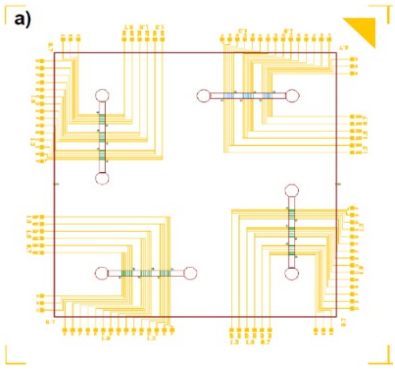


Figure 7. Top view schematic of the mask design, the device dimension is 2x2 cm (yellow lines is level 1 transformed into Cr/Ni lines after lift-off)

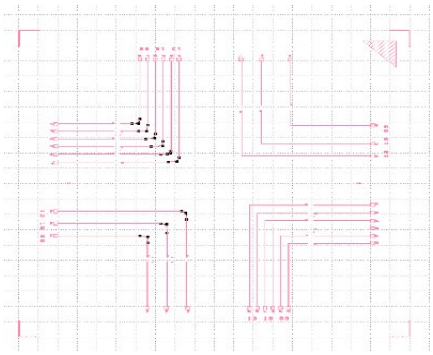


Figure 8. The new design of level1 (metal lines), four different arrangement are investigated to study the link between the stress and the shapes oft he patterns

lithography according to the new design and no peel-off of the photoresist was observed. Thus, the process of fabrication could be continued without problem. This new approach for performing the mesa-etch down to the substrate (etch of the total p+ layer thickness) will be used in the future for the fabrication of new devices.

Table 1. Designed and validated 4H-SiC reactive ion etching recipes

Recipe	Metal Mask type	Power (W)	Pressure (mTorr)	DC Bias (V)	SF6 (sccm)	O2 (sccm)	SiC etch rate (nm/min)
1	Ni	300	148	120	20	20	150
2	Al	300	100	195	50	10	90

Device Electrical Characterization

The electrical characterization of the device is a key step with which we can validate the suitability of the device for sensing applications. The electrical characterization of the fabricated devices is performed under ambient conditions using a manual probe station KarlSuss and HP 4155A semiconductor parameter analyzer. The characterized devices are those fabricated with the full-mask process without any mesa etch of the p^+ layer. Fig. 9a shows the measured output characteristics for different V_{GS} values. Fig. 9b shows the measured transfer characteristic in terms of I_{DS}-V_{GS} for different V_{DS} (0.1 V, 0.5 V and 1V). The threshold voltage V_{TH} is about -7 V according to the transfer characteristic (Fig. 9b). The output and transfer characteristics confirmed the good control over the channel conduction by the back-gate bias. These characteristics can degrade due to various reasons and more often due to the presence of interfacial/surface defects. These defects can be created during the fabrication process such as the reactive ion etching (RIE) and SiO_2 (passivation layer) deposition. All I-V curves of the tested devices in dry mode are consistent. Before performing any of the sensing measurements, the fabricated 4H-SiC-ISJFET is evaluated for fabrication-induced degradation of the sensor characteristics such as hysteresis and subthreshold swing (Fig. 9c). Fig. 9c shows the hysteresis evaluation in the transfer characteristics of the 4H-SiC-JFET (W = 1.3μm). The drain current I_{DS} was measured by scanning the gate voltage from -12V to +2V in the forward voltage sweep and +2V to -12V in the reverse voltage sweep, for V_{DS}= 1V. The gate voltage sweep was kept constant at 50 mV/s through the measurement. A small subthreshold swing is desirable since it implies the efficiency of the current drive or in other words that the device can rapidly switch from the off-state (where the drain current is very small) to the 'on' state with a small-applied bias. The latter is the desired quality in all the FET-based sensors. A steeper transfer characteristic with a low subthreshold swing SS is always preferred as it indicates lower trap densities and a cleaner surface [13]. The subthreshold slope is extracted from the subthreshold current as $SS = (\partial log_{10}(I_{DS})/\partial V_{GS})^{-1}$. The hysteresis (memory effect) which is the difference between the two gate-voltage sweep directions is a crucial parameter since the subsequent measurement of the surface charges for sensing relies on shifts of the threshold voltage [13]. The measured hysteresis and subthreshold swing value of the fabricated device are 498 mV at V_{DS}=1V and 121 mV/dec, respectively. Obviously, the value of SS is quite low while the threshold voltage hysteresis is very large for the targeted applications. Therefore, extra steps (such as annealing of sacrificial oxidation) should be added in the critical steps of the fabrication process for eliminating surface/interface defects the quantity of which is estimated [14] $2.05 \cdot 10^{11} cm^{-2}$. Furthermore, the realization of the mesa down to the substrate will render less sensitive the sensor structure to this type of defect.

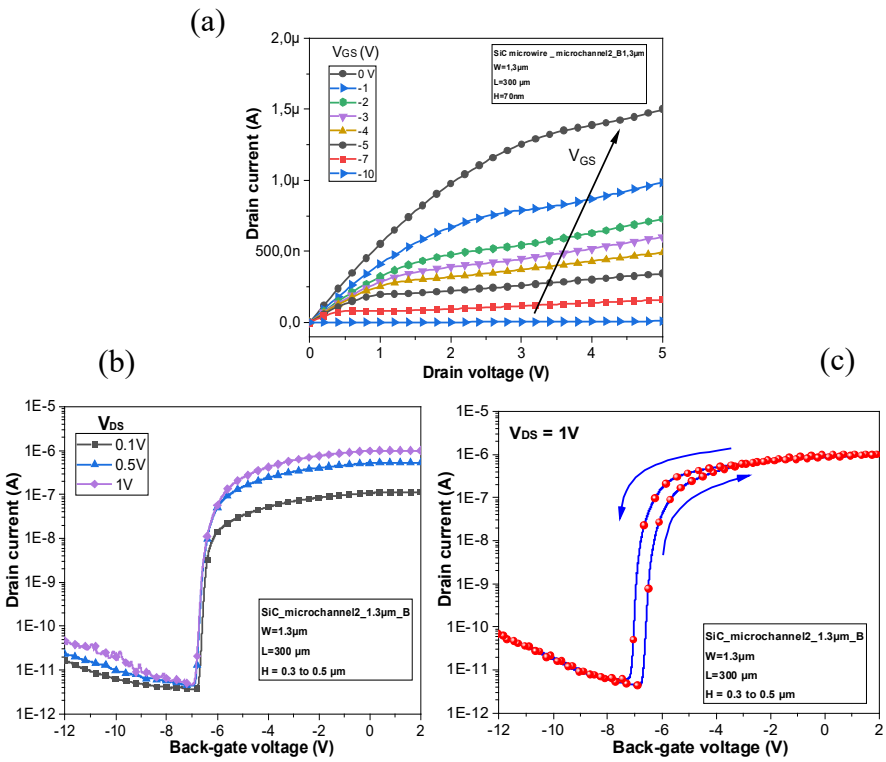


Figure 9. (a) Output characteristic in terms of drain voltage versus drain current at different gate voltages, (b) Transfer characteristic in terms of drain current versus back-gate voltage of the same microwire of width size 1.3µm at different drain voltage values 0.1V, 0.5V and 1 V and (c) transfer characteristic showing hysteresis of 498 mV at V_{DS}=1V

Device Numerical Simulation

The 3D ATLAS-SILVACO has been used for the simulation of the OG-4H-SiC JFET. For sake of simplicity, the n^+ substrate is not included in the simulation and it is replaced by a metal contact for the gate terminal. The channel length of the fabricated device is about 300 µm and it is set at 3 µm for the simulation to reduce the simulation time and reduce the simulator memory consumption. Fig. 10 shows the 3D meshed SiC 4H-SiC-JFET structure used for device simulation. In addition to the use of appropriate models and numerical methods for a particular device material, the accuracy of the simulation also depends upon the density of the mesh used to define the device. Fig. 10 shows a densely meshed p-n junction and channel regions. Such refinements are required to accurately determine the threshold voltage, Vt, and hence the currents and other physical quantities through the device. The simulated structure is simplified compared to the real structure. The doping concentrations of all regions of the fabricated device are respected during simulation. Fig. 11a shows the I_{DS}-V_{DS} curves of the OG-4H-SiC-JFET, which have been derived by the TCAD simulation. The saturation and the linear section are predicted from the simulated curves, the latter can be used for the sensor parametric analysis and comparison with the experimental results. The I_{DS}-V_{GS} curves for different V_{DS} values are demonstrated in Fig. 11b. The most noticeable difference between simulated and experimental transfer characteristics is a threshold shift (nearly 3V) between the simulation and measurements. This shift is due to the non-idealities during the device fabrication and mostly due to the n^- channel height changes due to the fact that pinch-off

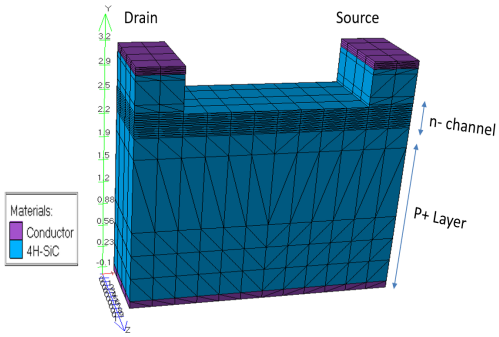
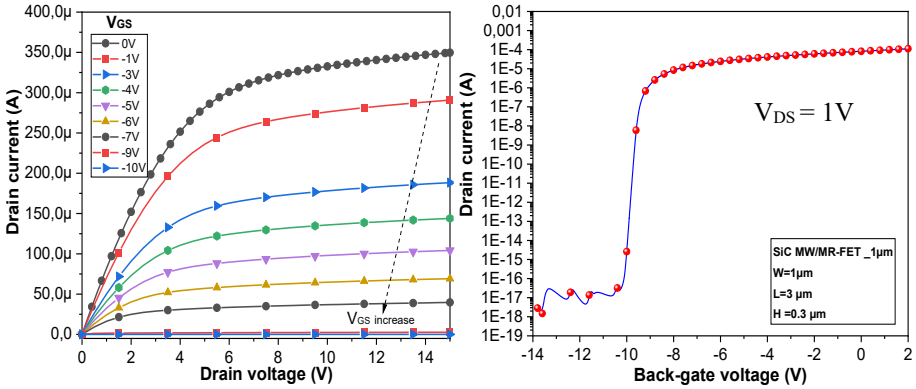


Figure 10. 3D figure of the simulated meshed device drawn with SILVACO Tonyplot

voltage is directly proportional to the square of channel-microwire height assuming abrupt junction formation. In simulations the n- channel height is 300 nm but for the fabricated device, the height is in the range between 250 and 350 nm. Even though there are many sources of non-idealities in the OG-4H-SiC-JFET system, which affect I-V characteristics, the numerical simulation is predicting an almost similar pattern of the experimental output and transfer characteristics.



(a) (b)

Figure 11. I-Vs characteristics of the SiC 4H-SiC DGISJFET determined based on ATLAS Silvaco simulations (left) output characteristics in terms on I_{DS}-V_{DS} at different V_{GS} and (right) Transfer characteristic at V_{DS}=1V

Summary

An OG-4H-SiC-JFET has been introduced as a possible chemical- and bio-sensing device for the first time. The silicon carbide microfabrication process is based mainly on the SiC reactive ion etching and can allow simplified and mass production of further sensor devices. The OG-4H-SiC JFET is electrically characterized and proved as a credible device for the targeted applications. In addition to the experimental measurements, a TCAD Silvaco simulation of the device was also performed to validate the obtained I-V characteristics. Moreover, further investigation is required to verify the effectiveness of the device for in vivo measurement. Based on the simulation and experimental studies, we put forward for the first time this OG-4H-SiC-JFET as a sensing device.

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