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10kV+ Rated SiC n-IGBTs: Novel Collector-Side Design Approach Breaking the Trade-Off between dV/dt and Device Efficiency

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Keywords: SiC IGBT, dV/dt, trade-off curves, design optimization, electromagnetic interface.

Abstract. 10kV+ rated 4H- Silicon Carbide (SiC) Insulated Gate Bipolar Transistors (IGBTs) have the potential to become the devices of choice in future Medium Voltage (MV) and High Voltage (HV) power converters. However, one significant performance concern of SiC IGBTs is the extremely fast collector voltage rise (dV/dt) observed during inductive turn-off. Studies on the physical mechanisms of high dV/dt in 4H-SiC IGBTs revealed the importance of collector-side design in controlling the phenomenon. In this paper we propose a novel collector-side design approach, which consists of four n-type layers with optimized doping densities and allows the control of dV/dt independently from the device performance. Further, we demonstrate a reduction of dV/dt by 87% without degrading the high switching frequency capability of the device, or the on-state performance, through the addition of two n-type epitaxial layers in the collector side, between the buffer and the drift regions.

Introduction

Silicon (Si) bipolar devices, IGBTs and thyristors, are currently the preferred devices in Medium and High voltage applications due to their reduced conduction losses. However, SiC MOSFETs rated up to 10kV have been extensively studied and with advancements in silicon carbide fabrication processing, SiC MOSFETs rated up to 3.3kV have become available commercially by multiple manufacturers with some manufacturers also offering functional devices and engineering samples at higher voltages, reaching up to10kV. Due to the improved high-frequency capabilities of SiC MOSFETs compared to Si bipolar devices, they started displacing them in certain applications. Nonetheless, the on-state resistance of unipolar devices increases quadratically with the device breakdown voltage and therefore SiC bipolar devices can be more favourable for Medium and High voltage applications, at above the 10 kV mark. SiC Punch Through (PT) IGBTs, combine the controllability of MOS devices while achieving a significantly reduced on-state voltage drop, making them attractive.

Although the operational principle of a SiC PT-IGBT is like that of its Si counterpart, the voltage and current transients are not. As shown in Fig. 1, during the inductive turn-off process, SiC IGBTs have two voltage rising phases (one slow and one fast) and one current decaying phase, whereas Si IGBTs have one voltage rise phase and two current decay phases (one fast and one slow). The fast voltage rising phase of SiC IGBTs produces an extremely high dV/dT, which is a major concern, affecting the possibility of adoption in the next generation power conversion applications. It poses significant challenges in utilizing gate drivers, cause EMI-related issues to adjacent circuits, increase wire insulation degradation in power machines and pose a challenge in packaging them. As a result,

many studies have been focused on understanding the origins of the high dV/dt in SiC IGBT and revealing methods of suppressing it.

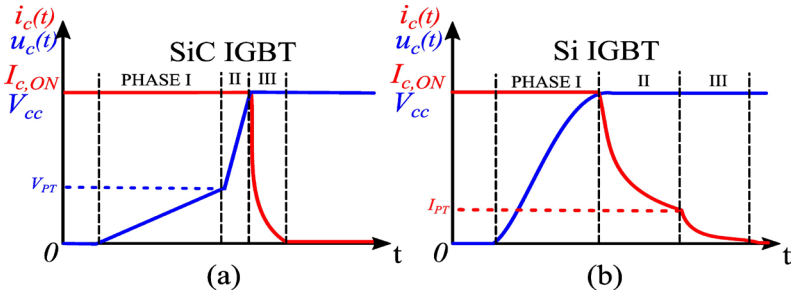


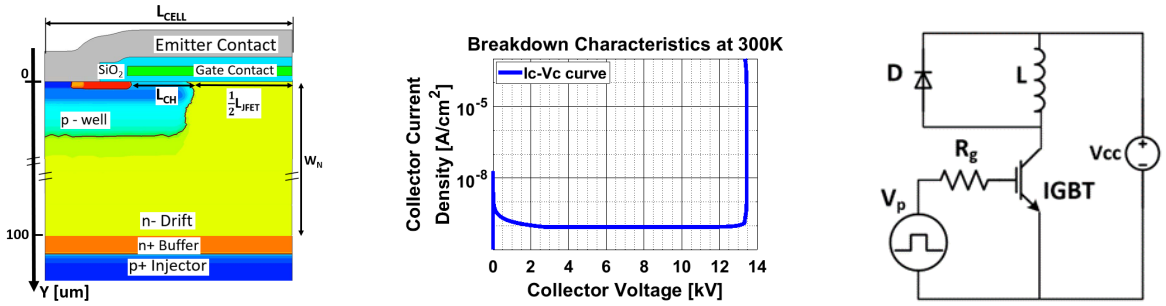
Fig. 1. I_c – V_c curves during inductive turn-off for (a) silicon carbide and (b) silicon IGBT.

Experimental results presented in [1]–[4] showed that by varying the buffer layer doping and thickness, the plasma injection can be controlled effectively, which can trade off the static performance for improvements in switching losses. However, the impact of these variations on dV/dt was not analysed. Several simulation studies focused on understanding the origins of the high dV/dt and finding ways to suppress it. It was found that external components have limited influence on the dV/dt, and they increase significantly the energy loss [5]. By adjusting the buffer design, a trade-off between switching energy and dV/dt was documented, but the impact on the on-state voltage drop was not studied. The drift layer characteristics were found to affect the turn-off behaviour until the buffer punch-through voltage was reached, i.e. influencing the slow voltage rise phase but not the fast. It was also found that by adjusting the drift layer doping, it is possible to lift the PT voltage above the DC bus voltage, but this results in a non-PT design which leads to significantly increased switching losses [5], [6]. More recently, the authors in [7] suggested a two-step buffer design to allow independent control of the breakdown and switching characteristics of the PT IGBT. However, the simulations were performed under low inductive load of 25A/cm^2, the dV/dt reduction was rather limited, from 200kV/μs to 120kV/μs, and the impact on the on-state voltage drop was not included in the study. Finally, there have been suggestions of some more complex solutions such as the usage of a multizone collector design [8] or the usage of trenches on the collector side [9]. However, these structures are difficult to be manufactured and they don't provide information on whether they can affect the dV/dt.

This paper analyses the inductive turn-off process of SiC IGBTs and reveal the origins of high dV/dt. After that, a comparison framework of different conventional buffer designs is presented to illustrate the trade-off between the on-state voltage drop, turn-off switching losses and maximum dV/dt under different current densities. Finally, a new collector-side design is proposed, featuring four n-type layers of optimised doping densities, which breaks the trade-offs, allowing for the control of dV/dT independently from other performance parameters.

Device Structure and Methodology

The fabrication process of a typical SiC PT n-IGBT was simulated using Synopsys Sentaurus Process. As shown in Fig. 2(a), the doping concentration (thickness) of the p+ injector, n buffer and n- drift layers are 1x10^{19} cm^{-3} (4 μm), 5x10^{17} cm^{-3} (3 μm) and 3x10^{14} cm^{-3} (100 μm) respectively. The p-well is featuring a retrograde profile which, as has already been described in previous works [10]–[13] improves the trade-off between breakdown, on-state and short-circuit characteristics. It achieves a breakdown voltage of about 13.5kV (Fig. 2(b)) at room temperature, thus allowing to rate the device at 10kV. For the dynamic simulations, a chopper circuit topology was used, coupling the finite element IGBT with a SPICE network shown in Fig. 2(c). The simulation uses previously calibrated models for critical semiconductor physics, including incomplete and impact ionization, Shockley-Read-Hall and Auger recombination, doping and temperature dependence of anisotropy, fixed charge and interface traps at the oxide-semiconductor interface etc [10], [11].



(a) (b) (c)

Fig. 2. (a) IGBT half-cell, (b) Breakdown waveform and (c) Chopper circuit topology.

Silicon Carbide Inductive Turn-Off Process

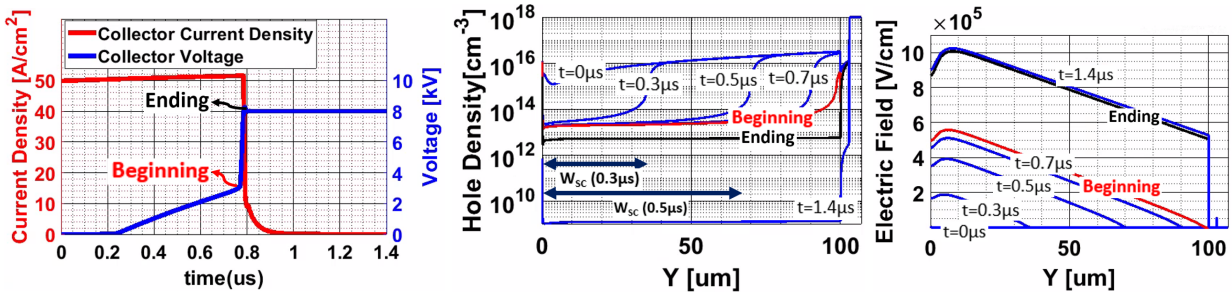
As has been already experimentally demonstrated in various papers [2]–[4], [15]–[18], the turn-off process of SiC PT IGBTs exhibit two different voltage rising phases followed by one current decaying phase as shown in Fig. 1(a). The first, slow, voltage rising period initiates when the gate voltage falls below the threshold voltage and the electron current ceases. As a result, the total current is sustained by hole current and the space charge region (or depletion region) starts expanding toward the collector side by removing holes at the space charge boundary. The collector voltage is related to the space charge width by Eq. 1, where the positive charge in the space charge region due to the hole current flow has been taken into account. This positive charge is given by Eq. 2, assuming that the holes are moving at their saturation drift velocity due to the high electric field in the space charge region. As a result, the space charge width and collector voltage are increasing at a slow pace determined by the injected hole concentration and the total current density. Additionally, the slope of the electric field is constant according to Poisson's equation 3.

$$V_c(t) = \frac{q(N_d + p_{SC})W_{SC}^2(t)}{2\varepsilon_s} \tag{1}$$

$$p_{SC} = \frac{J_{C,ON}}{q v_{sat,p}} \tag{2}$$

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s} = \frac{q(N_d + p_{SC})}{2\varepsilon_s} \tag{3}$$

The slow voltage rising phase ends when the space charge region reaches the buffer. The voltage at which this takes place (Punch-Through voltage, V_{PT}) is given by Eq. 1, where replacing the Wsc(t) with W_N. After that time, the electric field slope increases according to Eq. 3 due to the higher doping density of the buffer layer and the Electric field takes a trapezoidal shape. The origin of the high dV/dt can be explained by examining the hole density at the beginning and ending of the high voltage rising phase, shown in Fig. 3(b) with red and black colours respectively. It can be seen that the space charge region width inside the buffer layer and the amount of holes to be removed during this period are small, leading to a fast voltage transient after the Punch Through.

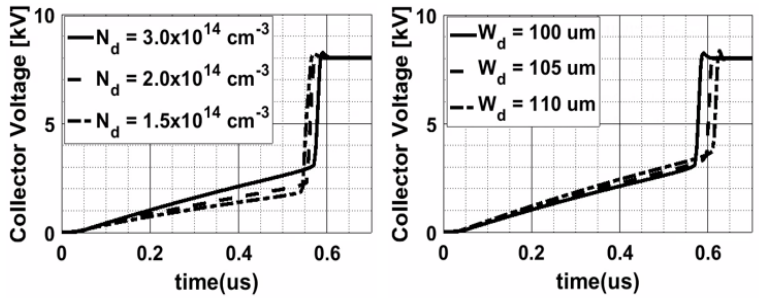


(a) (b) (c)

Fig. 3. (a) Typical $I_c(t)$ and $V_c(t)$ curves during inductive turn-off, (b) Hole distribution and (c) Electric field across the IGBT at various instants during the turn-off process.

Influence of the drift layer parameters

The drift layer parameters can adjust the punch-through voltage (V_{PT}) according to Eq. 1. Figures 4(a) and (b) show that the V_{PT} can be modified by either the drift region width or doping concentration. However, the high dV/dt during the fast voltage rising period remains relatively unaffected. This happens because the minority carriers injected into the buffer and drift layer are mainly dependent on the buffer layer characteristics, and as a result, the amount of holes to be removed from the buffer layer during the fast voltage rising phase is small for all drift layer variations. Nonetheless, it should be noted that drift layer doping concentration and width have opposite influences on the breakdown voltage, meaning that by increasing the doping density the breakdown voltage reduces, and by increasing the thickness the breakdown voltage increases. The table in Fig. 4(c) summarises the impact of the drift layer parameters on the static and dynamic performance of the IGBT.



W_d [um]	N_d [cm^{-3}]	BV [V]	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/us]
100	1.5x10^{14}	12749	4.47	38	389
100	2.0x10^{14}	12596	4.24	43	414
100	3.0x10^{14}	12191	3.96	53	416
105	3.0x10^{14}	12285	4.01	65	446
110	3.0x10^{14}	12738	3.98	59	426

(c)

Fig. 4. Collector voltage rising curves during turn-off for IGBTs with different (a) drift layer thicknesses and (b) drift layer doping concentrations, (c) Table summarising the static and dynamic characteristics of IGBTs with different variations of drift layer doping concentrations and thicknesses.

The role of the Buffer layer and the impact of its parameter's variation.

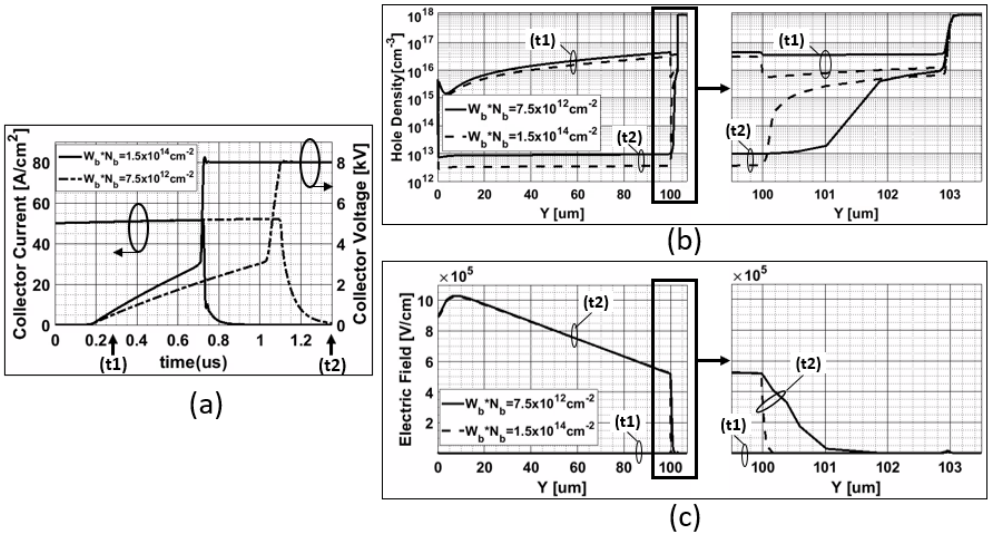
The buffer layer in PT-SiC IGBT plays a crucial role in the device's operation and affects the device's performance because it controls the plasma concentration in the drift layer. Higher buffer doping density and width lead to lower plasma concentration and as a result lower switching losses and higher on-state voltage drop. The minimum charge in the buffer layer to prevent reach-through to the injector layer can be obtained using Eq. 4[19]. Assuming a critical electric field (E_c) of 2x10^6 V/cm for typical drift layer doping concentrations, the minimum charge requirement is about 1x10^{13}cm^{-2}. A buffer layer with a thickness (W_B) of 3 μm requires a doping density (N_B) of 3.33x10^{16}cm^{-3}. By using a buffer layer charge higher than the minimum requirement, the plasma injection and therefore the on-state switching losses can be controlled.

$$N_B \cdot W_B = \frac{\varepsilon_s E_c}{q} \tag{4}$$

Fig. 5(a) compares the switching behaviour of two IGBTs with total buffer charges 1.5x10^{14} cm^{-2} and 7.5x10^{12} cm^{-2}, achieved by using 5x10^{17} cm^{-3} and 2.5x10^{16} cm^{-3} doping density in the 3 μm thick buffer layer. Figures 5(b) and 5(c) show the hole density and the electric field at the beginning (t1) and ending (t2) of the turn-off. As can be seen, the lower buffer charge leads to higher plasma injection in the buffer layer during the on-state and increases the depletion region width within the buffer layer. Both these effects lead to a higher amount of holes being removed from the buffer layer and thus lower dV/dt. However, higher plasma concentration in the drift layer leads to increased turn-off duration and higher switching losses. From the results in Fig. 5 for variation of the buffer charge can be concluded that the buffer design affects the three operational characteristics of interest (the on-state voltage drop, the switching losses and the maximum dV/dt), but in a way that they cannot be independently adjusted. Additionally, a more straightforward comparison framework is required to compare different IGBT designs. This comparison framework will be presented in the next section.

Comparison framework

In order to compare the performance of different IGBT designs directly taking into account the on-state, switching losses and maximum dV/dt, these quantities must be clearly presented. For silicon IGBTs, the traditional $E_{off} - V_{on}$ trade-off curves are sufficient because these two quantities are the most important. However, in SiC IGBT the maximum dV/dt is also a quantity that needs to be optimised. As a result, including the maximum dV/dt value during the turn-off, by using a colourmap, into the E_{off}-V_{on} trade-off curves for silicon IGBTs, all three parameters can be clearly represented. Figure 6 (a) compares thirty IGBTs with different buffer designs, by varying the buffer layer doping concentration and thickness. It can be concluded that the lower dV/dt always comes with the cost of higher switching losses and all three depicted quantities are strongly coupled. As a result, *the higher frequency operation comes with the cost of a higher maximum dV/dt*.



W_bN_b [cm^{-2}]	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/us]
$1.5x10^{14}$	3.94	53	420
$7.5x10^{12}$	3.75	115	91

(d)

Fig. 5. (a) $I_c(t)$ and $V_c(t)$ curves during the turn-off of IGBTs with different buffer layer charges (W_bN_b). Comparison of the (b) hole densities and (c) electric field inside IGBTs with different buffer charges at the beginning and ending of the turn-off process, and (d) table summarising their switching characteristics.

Another way of comparison of different IGBT designs is to calculate the maximum switching frequency that can be achieved for a given thermal limitation. Assuming that the maximum power that can be dissipated on losses (P_{max}) is limited by the packaging at 300W/cm^2 and with a duty cycle (δ) of 50%, the maximum switching frequency (f_{max}) can be calculated by using Eq. 5. In this way, the three-variable optimisation problem became a two-variable one, and the almost linear dependence of the maximum switching frequency and dV/dt can be observed easier, as shown in Fig. 6(b) for different IGBT designs and current densities.

$$f_{max} = \frac{P_{max} - \delta \cdot V_{on} \cdot J_c}{E_{off}} \tag{5}$$

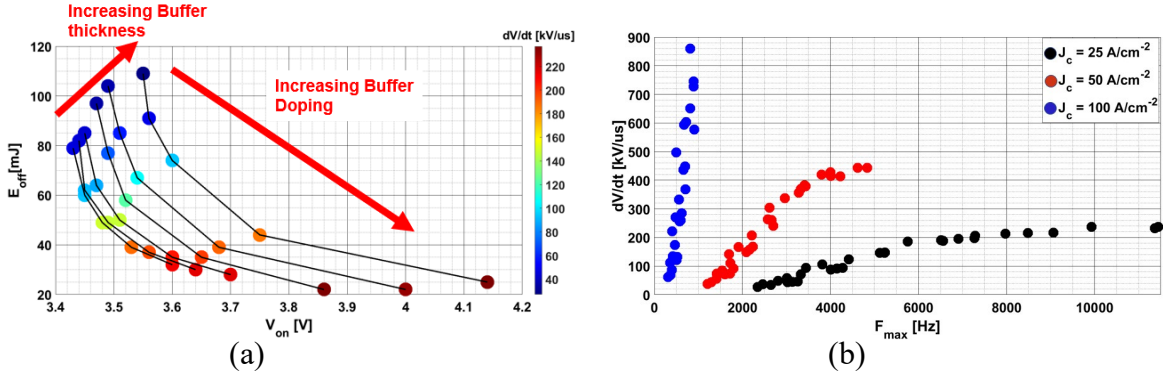


Fig. 6. (a) V_{on} –E_{off} –dV/dt trade-off curves for different IGBT designs and (b) relation between maximum achievable switching frequency and maximum dV/dt of conventional PT-IGBT designs under different current densities.

Proposed structure

After a detailed analysis of the behaviour of several IGBT designs under various operation conditions, we ended up with a novel device structure which achieves decoupling of the dV/dt from the trade-off between Von-Eoff. As a result, the increasing of the switching speed of the IGBT is not limited by the high dV/dt and EMI-related issues. The proposed structure is compared with the conventional one in Fig. 7. The role of the four n-type layers of the drift and buffer regions can be summarised as follows:

- The higher doped buffer region (HDB) prevents the depletion region from reaching through to the injector region during the forward (static) blocking. It provides the minimum buffer charge as described by Eq. 4.
- The lower doped buffer region (LDB) controls the plasma injection into the drift layer. Higher doping density or width leads to lower plasma injection into the drift region, and therefore the trade-off between on-state and switching losses can be adjusted.
- The higher doped drift region (HDD) is responsible for preventing the depletion region from punching through to the buffer layer during the voltage rising phase of the turn-off process. As a result, it controls the dV/dt by increasing the amount of minority carriers to be removed during the fast voltage transient phase.
- Finally, the lower doped drift region (LDD) controls the breakdown characteristics and the PT voltage of the IGBT.

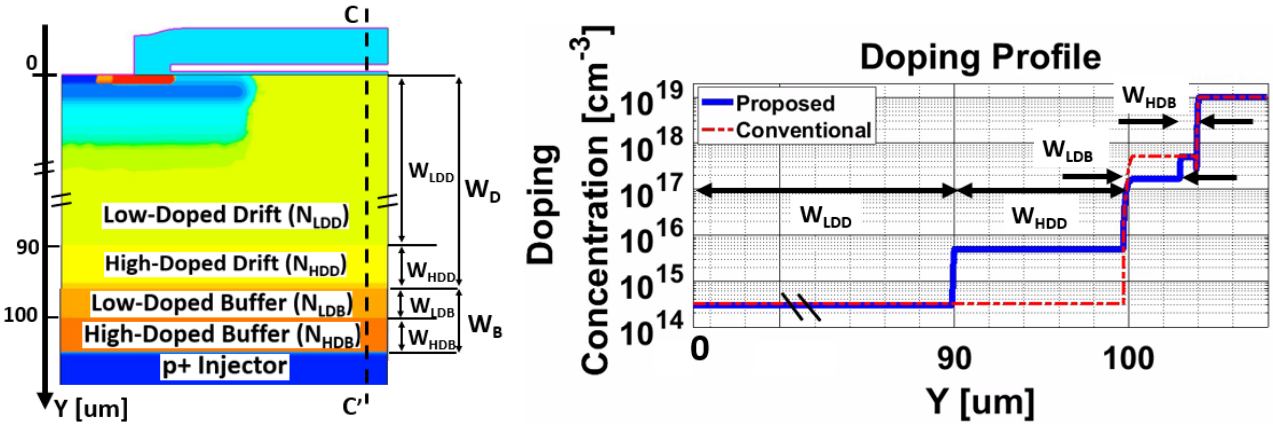
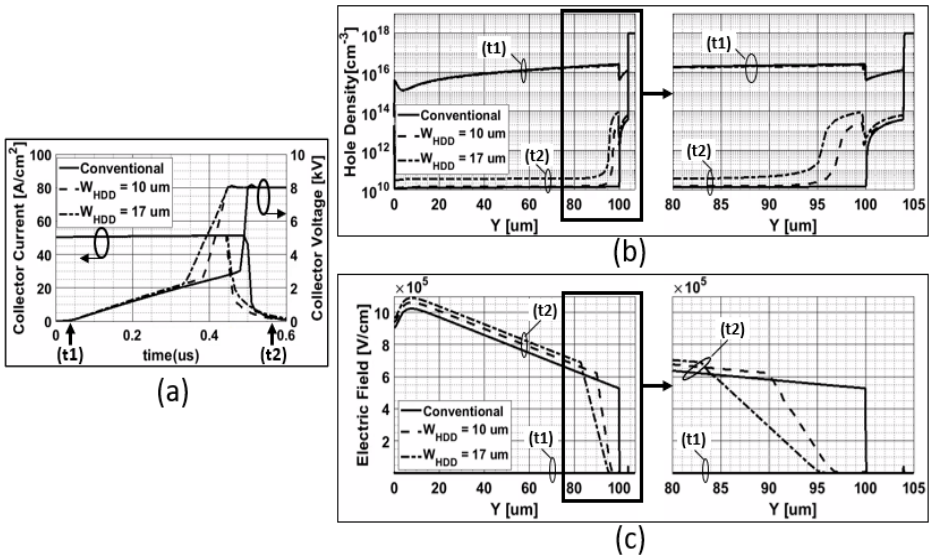


Fig. 7. (a) Novel collector side IGBT design featuring a step doping profile for the buffer and the drift layers, (b) doping profile comparison between the conventional and the proposed structure across the c-c' cut.

This simple device structure offers the advantage of almost independent control of the trade-off between on-state losses, switching losses and maximum dV/dt. Figure 8 shows how the high dV/dt phase during the inductive turn-off process can be modified with the appropriate selection of doping density and width of the higher-doped drift region (HDD). In this case, the electric field changes slope in the interface between the LDD and HDD regions, instead of the interface between the drift and buffer layer of the conventional structure. As a result, the depletion width during the fast voltage rising phase is much higher achieving an 87% reduction of the maximum dV/dt without affecting significantly the on-state voltage drop and the turn-off switching losses of the IGBT.

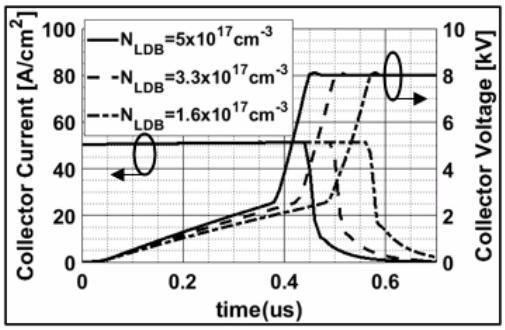


	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/us]	F_{max} [Hz]
Convent.	4.06	47	413	4223
W_{HDD}=10	4.1	49	86	4031
W_{HDD}=17	4.08	46	52	4304

(d)

Fig. 8. (a) Comparison of $I_c(t)$ and $V_c(t)$ curves during the turn-off between the conventional IGBT and IGBTs with different High Doped Drift regions (HDD) to reduce the dV/dt during the fast voltage rising phase. Comparison of the (b) hole densities and (c) electric field inside these IGBTs at the beginning and ending of the turn-off process, and (d) table summarising their switching characteristics.

Figure 9 shows how the lower-doped buffer region (LDB) affects the trade-off between Von-Eoff. As can be seen, the optimum Von-Eoff for a desired application can be chosen without affecting significantly the dV/dt.



N_{LDB} [cm^{-3}]	V_{on} [V]	E_{off} [mJ]	dV/dt [kV/us]	F_{max} [Hz]
$5x10^{17}$	4.1	49	86	4031
$3.3x10^{17}$	4.04	55	77	3618
$1.6x10^{17}$	3.95	64	67	3145

(b)

Fig. 9. (a) Comparison of $I_c(t)$ and $V_c(t)$ curves during the turn-off between IGBTs with different Low Doped Buffer regions (LDB) to control the V_{on}-E_{off} trade-off, and (b) table summarising their switching characteristics.

Comparison between the conventional and the proposed structure

The reduction of the maximum dV/dt achieved with the proposed device structure can be seen in figures 10(a) and 10(b). The coloured dots inside the diamond symbols in Fig. 10(a) represent variations of the proposed IGBT structures. It is obvious that the maximum dV/dt of all proposed IGBT structures is greatly improved when it is compared to the conventional designs. Furthermore, the reduction of the dV/dt for a given switching frequency achieved with the new design can be seen in Fig. 10(b), where the red points are for the conventional IGBT designs and the black and blue for the two different cases of the proposed design. Equation 5 was used to calculate the maximum switching frequency of each simulated device under inductive load of 25 A/cm^2.

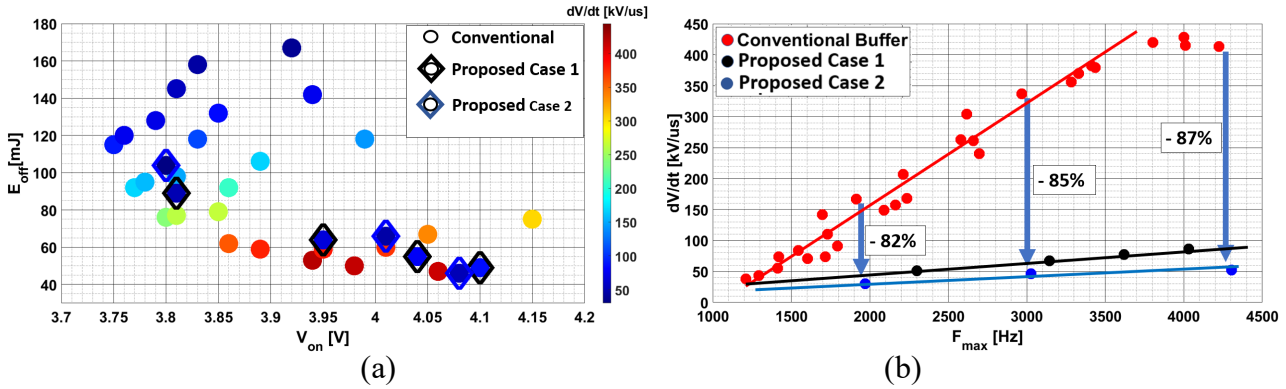


Fig. 10. Comparison between the conventional and the proposed structure using (a) the V_{on} – E_{off} – dV/dT trade-off curves and (b) F_{max} – dV/dt trade-off curves.

Summary

To conclude, this paper presented a novel device structure which can mitigate the high dV/dt produced during the turn-off process of SiC PT-IGBTs. By making use of a four-step n-type doping profile on the collector side, Fig. 7(b), the IGBT efficiency and dV/dt can be controlled independently. Furthermore, this device structure simplifies the IGBT optimization procedure because it provides a straightforward relationship between the device parameters and operational characteristics. As a result, an optimal device can be designed for specific application requirements.

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