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A Scalable SPICE Electrothermal Compact Model for SiC MOSFETs: A Comparative Study between the LEVEL-3 and the BSIM

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Abstract. In this paper, two implementations of a SPICE-based compact model for SiC MOSFETs are presented. The two versions rely on widely adopted LEVEL-3 and BSIM 4.6.1 models, respectively. The paper discusses the feasibility of adopting these two models for the description of SiC power MOSFETs. Furthermore, after calibrating the DC characteristics on target experimental data coming from 1.7 kV-60 A MOSFETs, a comparison between the accuracy of the two is presented.

Introduction

Compact modeling is a major field of research for the semiconductor industry and Simulation Program with Integrated Circuit Emphasis (best known as SPICE-like simulators) represent a fundamental tool for the modern circuit development. As it stands clear from the SPICE abbreviation, circuit simulation historically started to simplify the process IC design, but its importance rapidly extended into other areas of electronics, such as, analog circuit design, radio Frequency and power electronics. An acknowledgment of the significance of compact modeling for the power electronic world can be based upon the observation that most device manufacturers frequently release compact models along with their new products. Among all the SiC-based power devices, the MOSFET (in all its possible implementations) is probably the one that received the greatest attention from both research institutes and enterprises. The technological maturity of SiC MOSFETs gradually improved, during the last 20 years and, despite lower short circuit robustness, some devices also feature an inherently safe failure type [1], [2]. Therefore, the implementation of switching converters relying on both discrete SiC MOSFETs and power modules of various voltage ratings (from 650 V to 3.3 kV) remarkably increased in different market segments [3]. At the same time, there has been a higher demand for SiC MOSFETs compact models that are satisfactorily accurate and fast to allow a reliable validation of the design of complex converter machines. While device manufacturers usually provide compact models to allow the verification of their products, such models present several limitations. Some of them are based on polynomial fitting functions [4], with consequent possible inaccuracies when stimulated with electrical and thermal conditions exceeding those in which the model was tested. Furthermore, vendors encrypt [5] their model to protect the intellectual property, so not allowing to vary their internal parameters. In the last years, several examples of models for SiC power MOSFETs have been proposed in the literature. Good summaries can be found in [6] - [8]. The aim of this paper is that of presenting a SPICE-compatible model for SiC power MOSFETs that is based on a low number of parameters. The model is entirely based on SPICE standard components (i.e., that can be found in most SPICE versions and releases), thus making it compatible with any SPICE-like circuit simulator. Two versions of the model are presented and their static performances are validated on 1.7 kV-60 A-rated devices.

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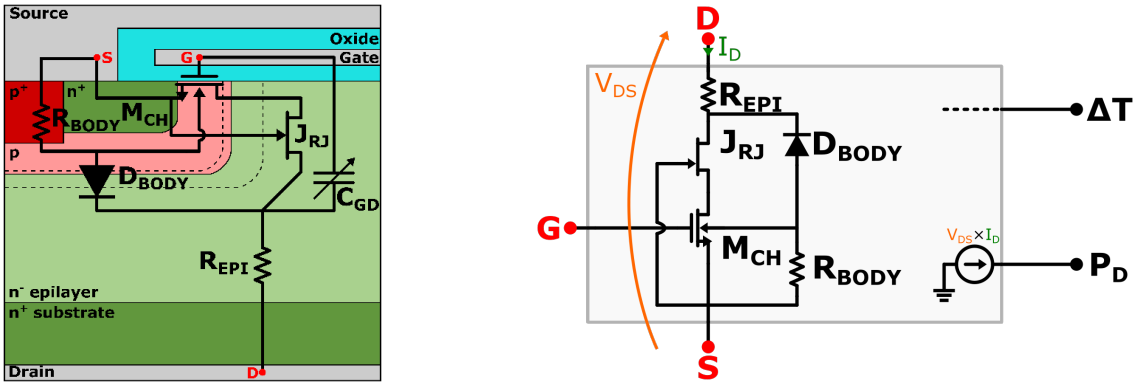
Implementation of the SiC MOSFET Compact Model

Introduction to the Modeling Technique. The compact electrothermal model described in this work is a variation of the one presented in [9], which has been previously tested on 1.2 kV- and 3.3 kV-rated devices [10] - [12], but it relies on a much smaller set of parameters. Fig 1a represents the schematic cross-section of a planar vertical diffused SiC MOSFET (VD-MOSFET). In it, several parasitic sub-structures can be identified, i.e., regions where the arrangement of the materials resembles that of other components (e.g., capacitors, resistors, and inductors) or semiconductor devices (e.g., diodes, BJTs, and JFETs). Therefore, the device under test (DUT) is modelled as a subcircuit where such simpler components are interconnected so that their concurrent operation describes the behavior of the DUT. Such an approach is oftentimes referred to as macro-modeling.



(a) (b)

Fig. 1. (a) Idealized (not-to scale) cross-section of the elementary cell of the active area of a SiC VD-MOSFET. The components associated to the different device regions are overlapped to the corresponding sub-structures.

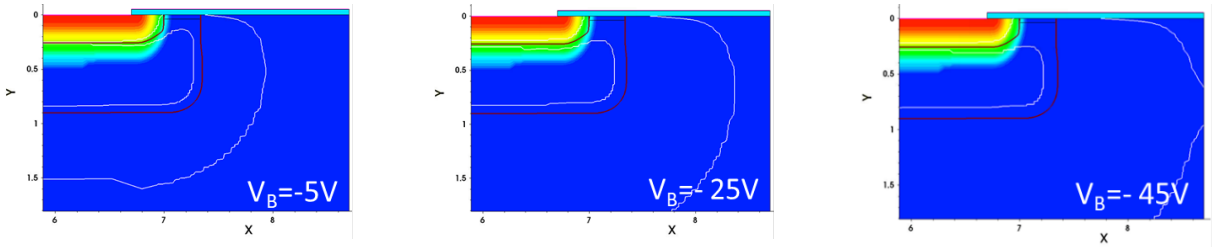
The channel layer forming in the p-doped well under the gate oxide is described through a standard SPICE MOSFET component, labelled as M_{CH}. In [9], such a MOSFET was implemented through a LEVEL 1 MOSFET connected to further behavioral current sources to the take into account additional phenomena (such as, the mobility degradation due to high horizontal and vertical electric fields). In this paper, two alternative models are considered for the description of M_{CH}: a LEVEL-3 and a BSIM 4.6.1. These are widely adopted models and implemented in most SPICE versions. A comparison of their DC performance is provided in the following subsections.

Within the semiconductor cross-section, the JFET region is the one extending between two p-implantations and has a significant impact on the on-state resistance. When the drain potential is higher than the source potential, the pn junction formed by the body and the epilayer is reversely biased. This causes the space charge region to expand more in the n-doped region than in the p-doped one (Fig 2) due to the lower doping concentration of the epi-layer. The moving boundary of the depleted layer pinches the current path and thus modulates the overall on-state resistance. In [9], such a phenomenon was formerly described by a voltage-dependent resistor based on a behavioral function. Here, a standard SPICE JFET (J_{RJ}) models the accumulation and JFET regions. Replacing the resistor with a JFET reduces the number of fitting parameters, improves convergence, and strengthen the physic foundation of the model.

The compact model is implemented as a SPICE subcircuit, a schematic of which is given in Fig. 1b. The terminals ΔT and P_D represent the temperature increment and the power dissipation, respectively, according to the temperature equivalent Ohm's law and enable the electrothermal feedback by connecting the model to a proper electrothermal network [13].

The behavior of the JFET region was characterized through TCAD simulations conducted on a reference structure [1] where a highly doped N++ layer (dummy channel) is added beneath the gate oxide. In this way, the source terminal acts as the anode-side contact of the parasitic JFET, thus allowing to isolate the impact of the JFET region on the total on-state resistance by suppressing the contributions given by the accumulation and channel regions. Fig. 2 reports the extension of the

depletion region around the body/epi-layer pn junction obtained at different values of the body potential and shows that, in the JFET region, the pinch-off occurs around V_B = -45 V. This clarifies that the JFET acts as a voltage-controlled resistor smoothing the transition from the linear to the saturation region.



(a) (b) (c)

Fig. 2. Cross sections depicting the potential distribution and the expansion of the boundaries of the space charge region for different values of body potential: (a) V_B = -5 V, (b) V_B = -25 V, (c) V_B = -45 V. The remaining terminals are grounded.

Description of Channel MOSFET with LEVEL-3 and BSIM MODEL. Both the LEVEL-3 model and the BSIM feature a vast number of parameters. Specifically, the LEVEL-3 relies on 87 parameters, while the equations of the BSIM 4.6.1 are based on 300 parameters. Such a high number of parameters is necessary to take into account all the effects governing the behavior of very short-channel integrated MOSFETs like the ones adopted in the digital industry. However, it is interesting to understand if a reasonably small set of parameters is sufficient to describe the DC behavior of SiC power MOSFETs. In this paper, 7 and 11 featuring in the DC-equations of the LEVEL-3 and BSIM were considered, respectively. On the other hand, 3 parameters were considered to describe the JFET. Despite being much smaller than the original number of parameters, their manual tuning is not a trivial task since they often mutually affect the DC characteristics. Therefore, a MATLAB graphical user interface (Fig. 3) was developed to assist the model calibration. After an initial selection of the main parameters, the fine tuning is performed through automatic optimization cycle, a flowchart of which is reported in Fig .4.

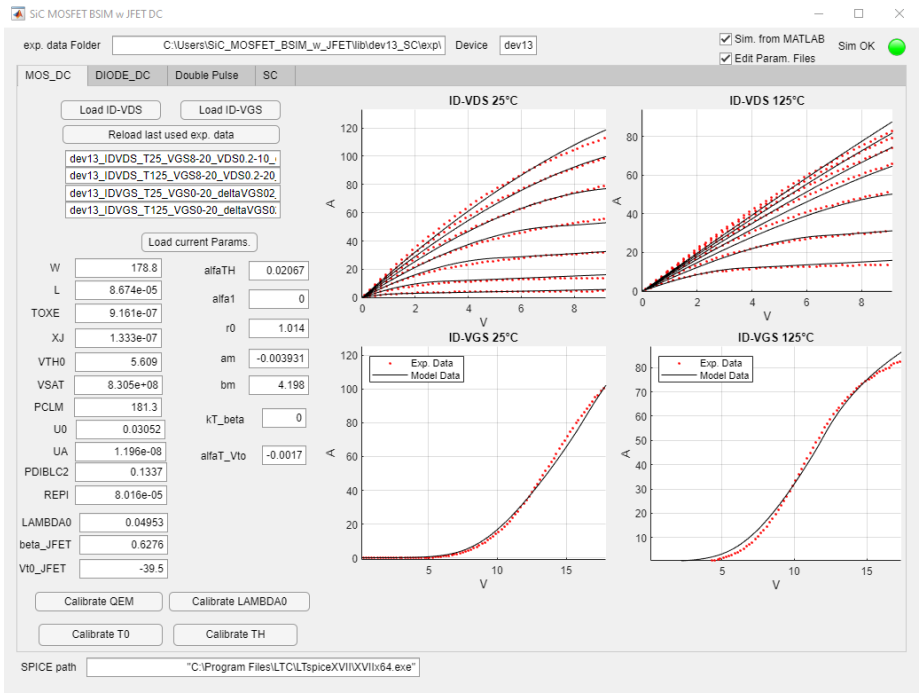


Fig. 3. Example of the MATLAB-based graphical user interface developed to assist the calibration of the parameters of the SiC MOSFET compact model.

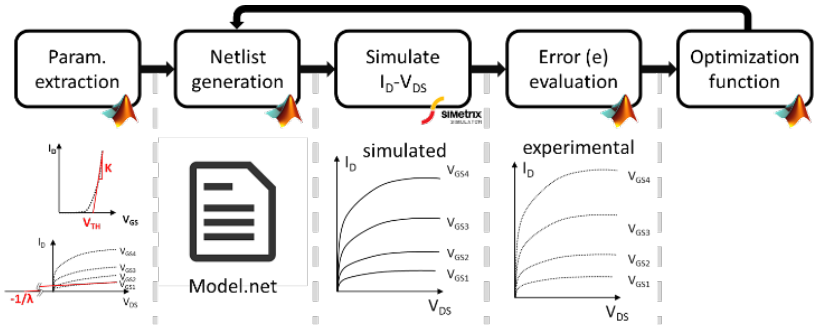


Fig. 4. Flowchart of the automatic routine for the optimization the parameters and the calibration of the static curves.

Comparison of DC Accuracy. The model was calibrated on 1.7 kV/60 A-rated SiC MOSFETs. The target data for the optimization routine are the isothermal static current-voltage characteristics (I_D - V_{GS} and I_D - V_{DS}), both at 25 °C and at 125 °C. These were measured through a pulsed curve tracer developed in-house. The overlap with the experimental DC characteristics (Fig. 5a-b) highlights that excellent agreement was achieved at room temperature by the model where M_{CH} is implemented as a LEVEL-3. Subsequently, the optimization procedure was repeated to evaluate the temperature coefficients of the static parameters. The comparison reported in Figs. 5a and 5c shows that the model can accurately reproduce the DC characteristics also at 400 K, with only a slight deviation in the I_D-V_{GS} curve at high V_{GS}. Therefore, the selected subset of parameters of the LEVEL-3 MOSFET and LEVEL-1 JFET allows to provide a good description of the I_D-V_{DS} and I_D-V_{GS} of the tested SiC power MOSFET.

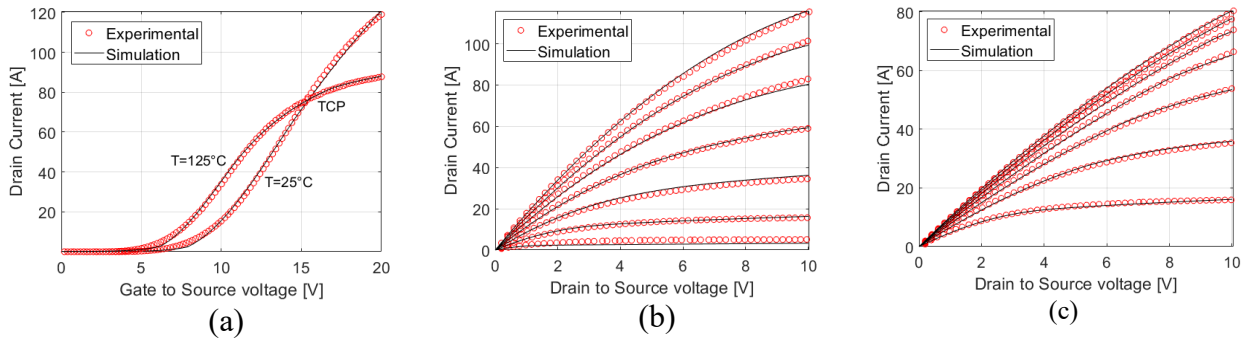
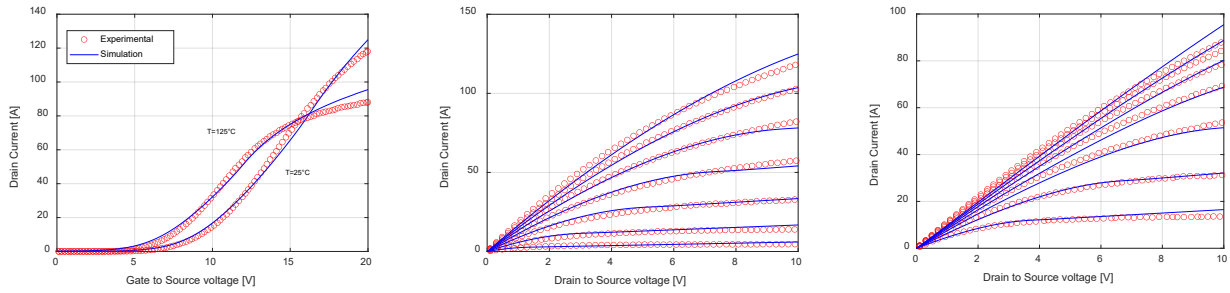


Fig. 5. Comparison between the experimental and simulated data obtained by implementing the channel MOSFT with the LEVEL-3 model: (a) isothermal transfer characteristics at 25 °C and 125 °C, (b) output characteristics at 25 °C and (c) 125 °C.

A comparison between the experimental and DC characteristics simulated when M_{CH} is implemented with BSIM 4.6.1 is reported Fig. 6. In general, the agreement between the simulated measured data is satisfactory, However, the simulated curves deviate from the measured ones at high V_{GS} values. On the other hand, it is worth specifying that, although both models never encountered convergence issues during the calibration routine, the model implemented with the BSIM always gave curves with smooth transitions between the various regions. On the other hand, the model implemented via the LEVEL-3 provided characteristics with sharp variations when the parameters were ill-selected. It is therefor worth exploring if adopting a relatively bigger set of parameters of the BSIM can provide better accuracy.



(a) (b) (c)

Fig. 6. Comparison between the experimental and simulated data obtained by implementing the channel MOSFT with the BSIM 4.6.1 model: (a) isothermal transfer characteristics at 25 °C and 125 °C, (b) output characteristics at 25 °C and (c) 125 °C.

Summary

In this manuscript, two implementations of a SPICE-based compact model for SiC MOSFETs have been presented: one based on the LEVEL-3 MOSFET model, the other relying on the BSIM 4.6.1. to assist the calibration of the DC characteristics to the experimental data of a 1.7 kV-60 A-rated SiC MOSFET, a graphical user interface and a semi-automated calibration procedure have been developed. The comparison between the simulated and measured characteristics has shown that the LEVEL-3-based model can provide adequate accuracy. The BSIM-based model provided lower accuracy yet giving smoother characteristics. Further investigation are needed to understand whether a wider set of parameters can improve the accuracy obtained by the latter model.

References

[1] G. Romano *et al*., "A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 978-987, Sept. 2016, doi: 10.1109/JESTPE.2016.2563220.

[2] A. Castellazzi *et al*., “Gate-damage accumulation and off-line recovery in SiC power MOSFETs with soft shortcircuit failure mode,” in *Microelectronics Reliability*, vol. 114, 2020, doi: 10.1016/j.microrel.2020.113943.

[3] L. Spaziani and L. Lu, "Silicon, GaN and SiC: There's room for all: An application space overview of device considerations," *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2018, pp. 8-11, doi: 10.1109/ISPSD.2018.8393590.

[4] 25 March 2022. [Online]. Available: https://www.wolfspeed.com/document-library?format=ltspice-models.

[5] 25 March 2022. [Online]. Available: https://www.onsemi.com/design/resources/ design-resources/models?rpn=NVBG020N120SC1

[6] H. A. Mantooth, K. Peng, E. Santi and J. L. Hudgins, "Modeling of Wide Bandgap Power Semiconductor Devices—Part I," in *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 423-433, Feb. 2015, doi: 10.1109/TED.2014.2368274.

[7] B. W. Nelson *et al*., "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Static Behavior," in *IEEE Open Journal of Power Electronics*, vol. 1, pp. 499-512, 2020, doi: 10.1109/OJPEL.2020.3036034.

[8] B. W. Nelson *et al*., "Computational Efficiency Analysis of SiC MOSFET Models in SPICE: Dynamic Behavior," in *IEEE Open Journal of Power Electronics*, vol. 2, pp. 106-123, 2021, doi: 10.1109/OJPEL.2021.3056075.

[9] M. Riccio, V. d'Alessandro, G. Romano, L. Maresca, G. Breglio and A. Irace, "A Temperature-Dependent SPICE Model of SiC Power MOSFETs for Within and Out-of-SOA Simulations," in *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 8020-8029, Sept. 2018, doi: 10.1109/TPEL.2017.2774764.

[10] A. Borghese *et al*., "Statistical Analysis of the Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1527-1538, Sept. 2019, doi: 10.1109/JESTPE.2019.2924735.

[11] A. Borghese *et al*., "An Experimentally Verified 3.3 kV SiC MOSFET Model Suitable for High-Current Modules Design," in *Proc. IEEE-ISPSD 2019,* pp. 215-218, doi: 10.1109/ISPSD.2019.8757576.

[12] C. Scognamillo *et al.*, "Compact Modeling of a 3.3 kV SiC MOSFET Power Module for Detailed Circuit-Level Electrothermal Simulations Including Parasitics," *Energies*, vol. 14, no. 15, p. 4683, Aug. 2021, doi: 10.3390/en14154683.

[13] A. Borghese *et al.*, "An Efficient Simulation Methodology to Quantify the Impact of Parameter Fluctuations on the Electrothermal Behavior of Multichip SiC Power Modules," in *Silicon Carbide and Related Materials 2018*, 2019, vol. 963, pp. 855–858. doi: 10.4028/www.scientific.net/MSF.963.855.