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A Fully Self-Aligned SiC Trench MOSFET with 0.5 µm Channel Pitch

Madankumar Sampath[1,a*], Dallas Morisette[1,b], and James A.Cooper[2,c]

[1]School of Electrical and Computer Engineering and Birck Nanotechnology Center
Purdue University, 1205 W. State St., West Lafayette, IN 47907 USA

[2]Sonrisa Research Inc., Santa Fe, NM 87506 USA

[a]msampath@purdue.edu, [b]morisett@purdue.edu, [c]cooperj@purdue.edu

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Abstract. SiC power MOSFETs have made great progress since the first commercial devices were introduced in 2011, but they are still far from their theoretical limits of performance. At blocking voltages above 1200 V the specific on-resistance is limited by the drift region, but below 1200 V the resistance is dominated by the channel and the substrate, with smaller contributions from the source and JFET regions. Trench MOSFETs have smaller cell area than planar DMOSFETs, and are inherently more scalable. Both Rohm and Infineon devices have cell pitches of about 3 µm per active channel. In this paper we demonstrate a highly self-aligned fabrication process to realize deeply-scaled trench MOSFETs with a cell pitch of 0.5 µm per channel. Since the narrow gate trench is shaped like a letter "I", we refer to these devices as "IMOSFETs".

Introduction

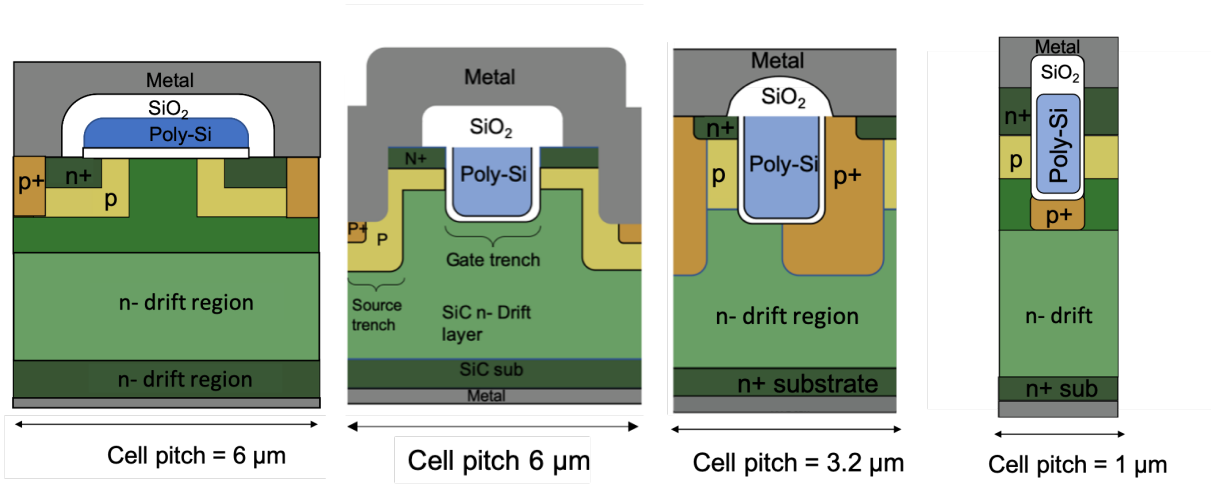
Recently it was demonstrated that 4H-SiC trench UMOSFETs can significantly improve the performance of power conversion units in hybrid-electric vehicles (HEV) [1]. Due to the high integration density of trench-gate devices and low conduction losses, they offer the opportunity to reduce the size and weight of power control units, key components in HEVs. The most critical issue in the design of SiC trench UMOSFETs is shielding the gate oxide from high electric fields at the bottom of the trench. The single-trench oxide protected UMOSFET [2] was first reported in 1998. This structure inserts a grounded p-type region below the gate trench to protect the oxide in the blocking state. In 2012, Rohm Semiconductor reported a novel double-trench UMOSFET with separate gate and field-protection trenches [3]. In 2017, Infineon introduced their "Cool-SiC" UMOSFET which demonstrated high gate oxide reliability [4]. The Rohm and Infineon MOSFETs each have a cell pitch of about 3 µm per active channel. In this paper we describe a fabrication process and provide electrical results for a deeply-scaled fully-self-aligned IMOSFET with a cell-pitch of 0.5 µm per channel, with improved oxide shielding compared with commercially available UMOSFETs [5].

Comparison with Existing SiC MOSFETs

Traditionally, one of the major challenges in trench MOSFETs is contacting the trench-shield implant. Rohm's double trench [3] and Infineon's Cool-SiC MOSFETs [4] use different methods to shield the gate oxide on bottom of the trench. As shown in Figure 1b, Rohm uses a separate trench to shield the gate trench. This provides a contact directly to the trench implant in every unit cell but also increases the cell pitch and thus $R_{on,sp}$. In the case of Infineon's Cool-SiC device, shown in Figure 1c, the channel on one side of the trench is sacrificed and replaced with a deep *p*+ implant which acts as a trench shield. This leads to higher on-resistance due to the loss of one channel, and also leaves one corner of the trench relatively unprotected, leading to higher oxide electric field than occurs in a fully shielded trench bottom.

Fabrication of the IMOSFET

The initial epitaxial layers of the IMOSFET are shown in Figure 2a. The advantage with an epitaxially grown *p*-type region is that the doping is constant in the channel region, and the base/CSL junction is abrupt. The disadvantage is that the *p*+ floating field rings will be shorted together by the *p*-base epi



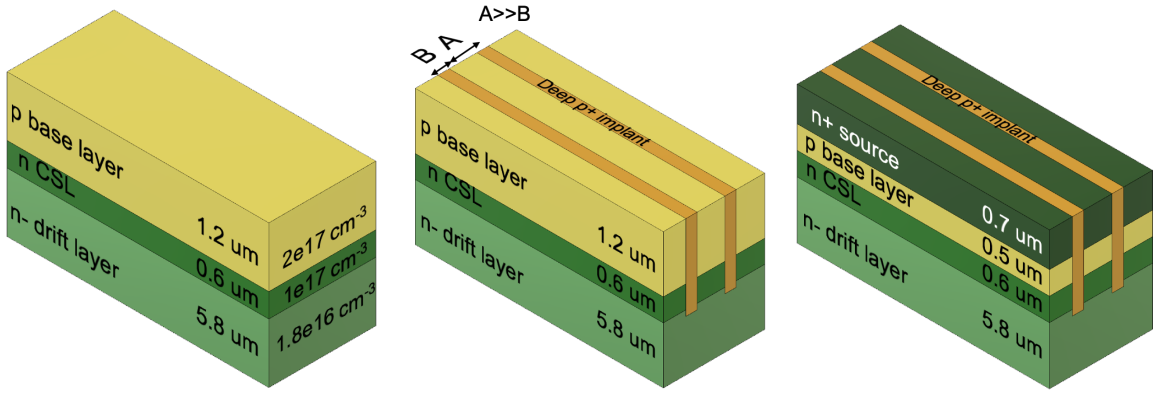
(a) DMOSFET (b) Rohm UMOSFET (c) Infineon Cool-SiC (d) IMOSFET

Fig. 1: Current MOSFETs and the proposed IMOSFET

region, requiring the field area needs to be etched. After this etch, the surface is no longer planar, and subsequent lithography must be done on a trench geometry. A new implanted base process is currently under development that will not require this field area etch, and which will significantly simplify the IMOSFET process.

Source and base contact implants: The first fabrication step in the IMOSFET process is a deep *p*+ ion implantation that contacts the base and trench shield regions as shown in Figure 2b, and also forms a floating field ring (FFR) edge termination and source implant uses the inverse mask as shown in Figure 2c. To achieve an implanted junction depth of 1.8 µm, high energy implantation in the MeV range is needed. The top section of the profile is heavily doped to produce a good *p*+ ohmic contact, while the bottom portion of the profile is optimized for the dose required for the FFR. The FFR region is subsequently etched to remove the *p*-base epitaxial layer, which would otherwise short the floating field rings together. Figure 3a shows a 4 µm polysilicon mask patterned using e-beam lithography for the *p*+ implant, and Figure 3b shows the Al implant profile (using pearson distribution) that will contact the trench shield implant below 1.5 µm.

SiC trench etch: The most critical step in the fabrication of the IMOSFET is the SiC gate trench etch. This step is challenging due to the required high aspect ratio and verticality of the sidewalls, and due to the sensitivity of the etch geometry to the mask profile. The trenches are 0.5 µm wide and 1.5 µm deep as shown in Figure 4. The Ni etch mask is patterned using an e-beam lithography lift-off process.



(a) Starting wafer (b) Deep *p*+ contact (c) Source implant

Fig. 2: Source and base contact implantation

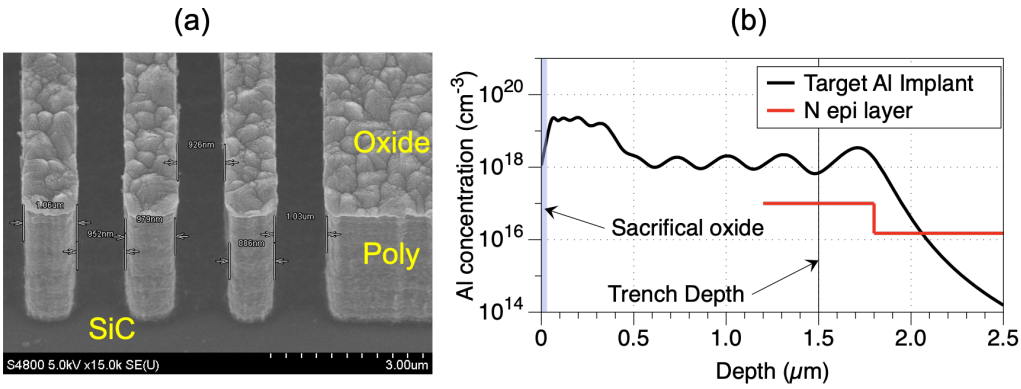
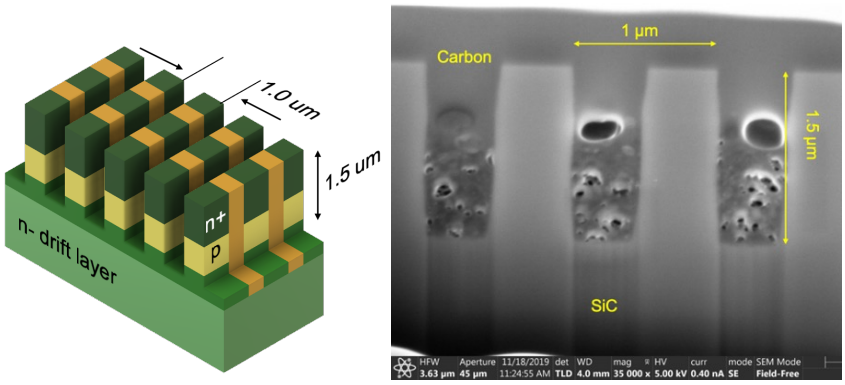


Fig. 3: Deep *p*+ implantation mask (a) and implant profile (b)

The electron mobility on the a-face in 4H-SiC is reported to be as much as 4 times higher compared to the Si-face [7], which could contribute to reduced specific on-resistance. To take advantage of this mobility anisotropy, the trench sidewalls are aligned with the $11\bar{2}0$ crystal faces and should have a smooth surface. Immediately after the trench etch, a self-aligned *p*+ shield is implanted. If the sidewalls of the trench are not vertical, the sidewalls of the trench may also be unintentionally implanted during this step, which in the worst case could lead to the loss of functional transistors. Figure 5 shows the results of a process simulation of the shield implant, and illustrates the potential for counter-doping of the sidewalls in the channel and CSL regions. A thin sidewall oxide is used to prevent unintentional implantation into these areas.



(a) (b)

Fig. 4: (a) IMOSFET structure after source and base contact implants and trench etch, (b) FIB cross-section after trench etch

Hydrogen etch: The reactive ion etching process used to form the gate trenches is known to create surface roughness that reduces the mobility of electrons in the inversion layers formed on these surfaces. Since the performance of the IMOSFET in the < 1 kV regime depends strongly on the channel resistance, it is critical to reduce this roughness and recover the sidewall mobility after the trench etch. One possible method to improve the sidewall mobility is to etch a thin layer of the RIE etched surface using a high temperature (1300-1700°C), low pressure (150-250 mbar) anneal in a hydrogen ambient (H_2 etch). Liu *et al.* [8] recently reported a $3\times$ improvement in peak mobility after hydrogen etching an RIE etched a-face surface at 1400°C. The reported etch removed approximately 100 nm of SiC, which would significantly alter the trench dimensions and the shield implant of the IMOSFET. Therefore we performed a study of the etch rate and trench shape transformation to optimize the hydrogen etch.

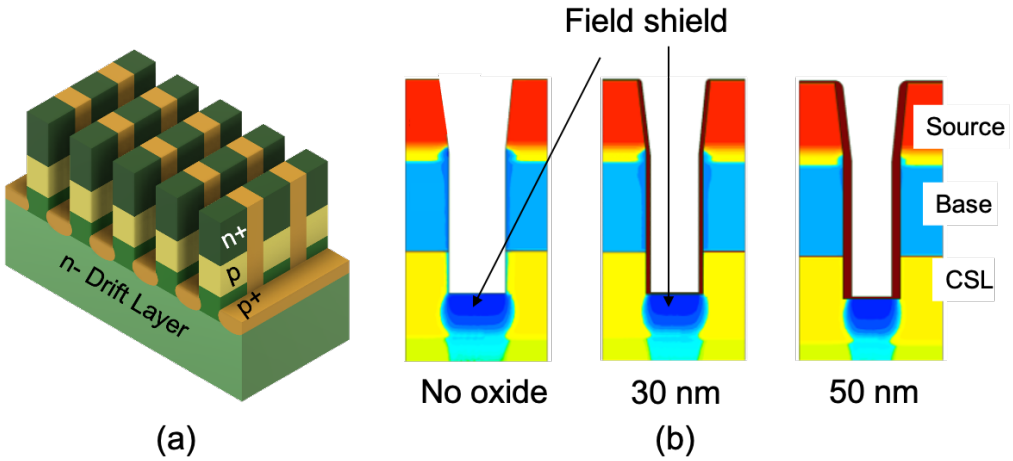
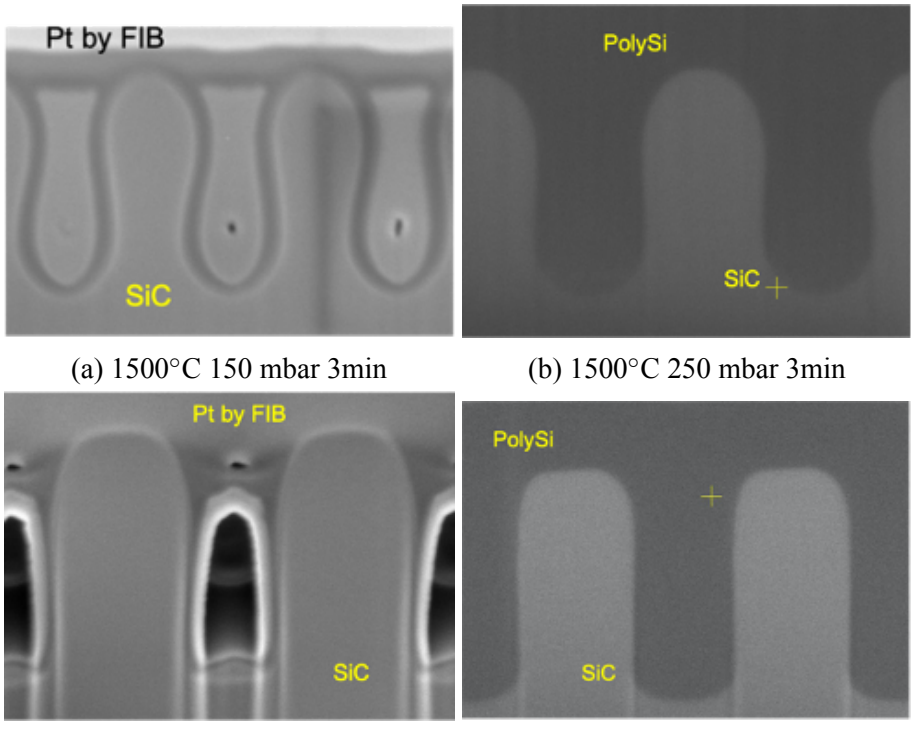


Fig. 5: (a) IMOSFET after trench shield implant, (b) simulated shield implant process with and without sidewall screening oxide



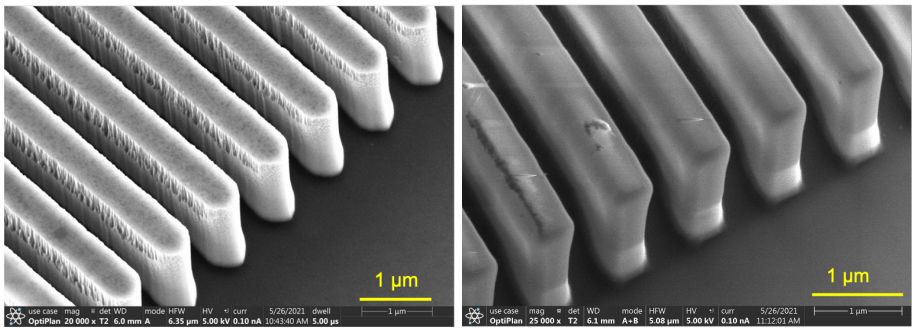
(a) 1500°C 150 mbar 3min (b) 1500°C 250 mbar 3min

(c) 1400°C 250 mbar 3min (d) 1350°C 250 mbar 3min

Fig. 6: FIB cross-section SEM of IMOSFET structures images for different H_2 etch conditions

At 1500°C, the trenches are completely rounded and the trench depth is reduced as shown in Figure 6a. The initial trench depth was 1.8 µm and was reduced to 1.6 µm after the 1500°C H_2 etch. This suggests that hydrogen etches the top and bottom surfaces differently due to high aspect ratio of the trenches. Figure 6b shows that at 1500°C and 250 mbar, there is still significant rounding of the corners, and the trench depth is reduced by 200 nm. Figure 6c and Figure 6d show the H_2 etch at 1400°C and 1350°C respectively. The trench depths in these two samples are very close to the original trench depth. The 1350°C H_2 etch exhibits more vertical sidewalls and less corner rounding, and therefore was used in subsequent IMOSFET prototype fabrication. Figure 7b shows the angled view of (a) non-H_2 etch samples and (b) 1350°C H_2 done on the devices.

Gate oxide and polysilicon deposition: The formation of a reliable, high-quality gate oxide is one of the keys to successful fabrication of all MOSFETs. To avoid the oxidation rate anisotropy of



(a) Non H_2-etched sample (b) H_2-etched sample

Fig. 7: RIE etched trenches with and without H_2 etching, which significantly reduces sidewall surface roughness

thermal oxidation of SiC [7], we form the gate oxide by thermally oxidizing a layer of polysilicon deposited by LPCVD at 580°C and 150-200 mTorr. To achieve a gate oxide with low leakage current, high breakdown field, and a low density of traps at the SiC-SiO_2 interface, the polysilicon layer is thermally oxidized in a clean pyrogenic tube at 1100°C, and subsequently annealed in a nitric oxide (NO) ambient at 1175°C. After the gate oxide is formed, polysilicon is deposited by LPCVD at 580°C to fill the gate trenches and planarize the surface [7].

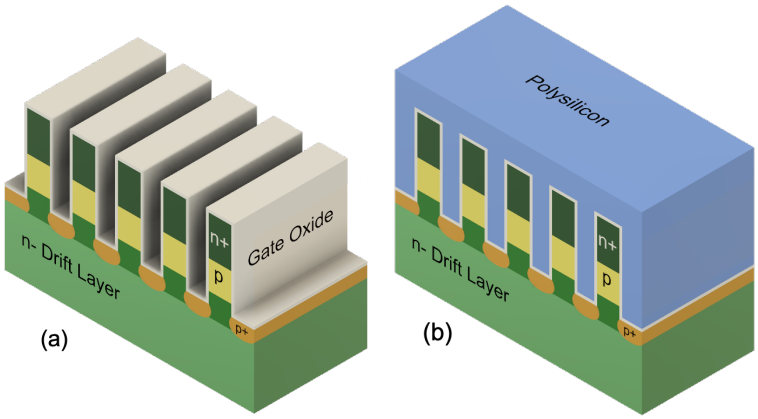
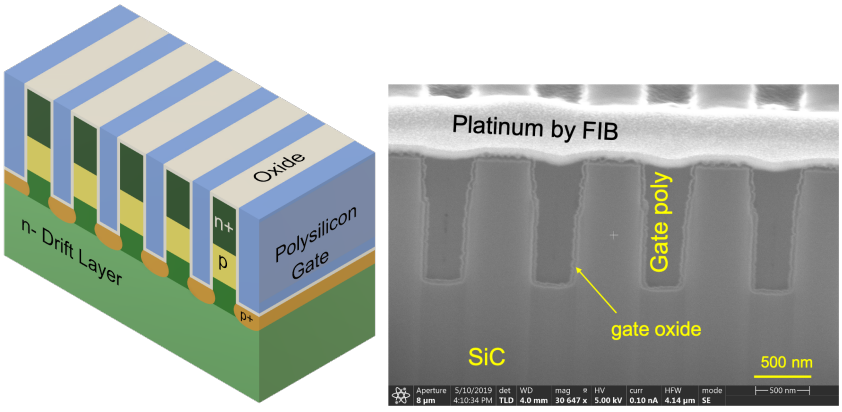


Fig. 8: IMOSFET after (a) gate oxide and (b) polysilicon deposition

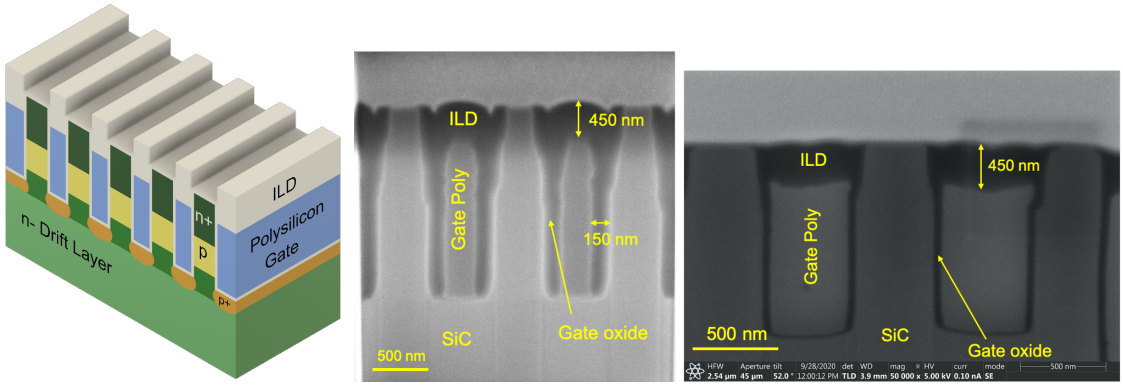


(a) (b)

Fig. 9: (a) IMOSFET after etch-back of planarized polysilicon to the SiC surface. (b) FIB cross-section after this step

The polysilicon is doped with phosphorus by diffusion at 1000°C from a spin-on dopant source (Filmtronics P509), then etched back to the level of the SiC mesa as shown in Figure 9a. Accurately stopping the polysilicon etch at top of the mesas is critically important because the polysilicon is subsequently oxidized to form the interlayer dielectric (ILD). If the polysilicon is etched far below the SiC surface, the ILD oxide growth will reduce or eliminate the gate-source overlap. A FIB cross-section of the resulting structure is shown in Figure 9b. Due to the fully-self aligned process, no mask is required in the active area during polysilicon planarization.

Self-aligned inter-layer dielectric: To form the inter-layer dielectric (ILD), we use a self-aligned process similar to that first developed for DMOSFETs [10], but we apply it to trench MOSFETs for the first time. The ILD layer is grown by thermal oxidation of the gate polysilicon without the need for a source contact mask. However, during this step oxygen diffuses vertically through the sidewall oxide and oxidizes the polysilicon laterally, increasing the gate oxide thickness as shown in Figure 10b. A detailed process simulation for the diffusion of oxygen with temperature is described in [10]. To prevent this, a thin layer of silicon nitride (~5 nm) is deposited by LPCVD over the gate oxide



(a) (b) (c)

Fig. 10: (a) IMOSFET after thermal oxidation of the gate polysilicon to form the interlayer dielectric. (b) FIB cross-section without and (c) with nitride diffusion barrier

just before gate polysilicon deposition. The FIB cross-section shown in Figure 10c demonstrates that this thin nitride layer is sufficient to block oxygen diffusion through sidewalls and oxidation of the adjacent polysilicon. MOS capacitors fabricated with and without the thin nitride layer showed no significant differences in interface state density or gate leakage.

Self-aligned ohmic contacts:The self-aligned process we use to form the source ohmic contacts takes advantage of the difference in oxidation rates between SiC and polysilicon during ILD formation. This makes it possible to remove thin oxide on top of the SiC fins by a short unmasked BOE dip while leaving thicker oxide on the polysilicon gates mostly unetched [10]. Nickel is then deposited and annealed at 750°C to form nickel silicide in areas where the Ni is in contact with SiC. At this temperature nickel does not react with the ILD, and is subsequently removed by a blanket piranha etch. To achieve low source contact resistance, a second ohmic anneal is then performed at 1000°C as shown in Figure 11. The final step in the fabrication of the IMOSFET is contacting the gate and source areas with top metal, which is deposited by sputtering and patterned by optical lithography and a wet chemical etch. An optical image of the final completed device is shown in Figure 12a, and a FIB cross-section in the active area is shown in Figure 12b. More detailed processing information of the IMOSFET device are shown in [9].

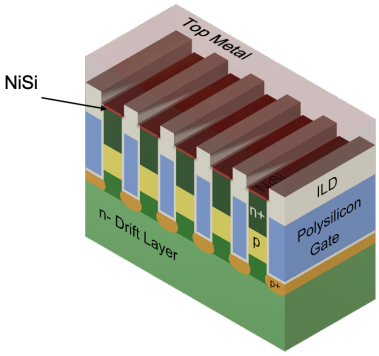
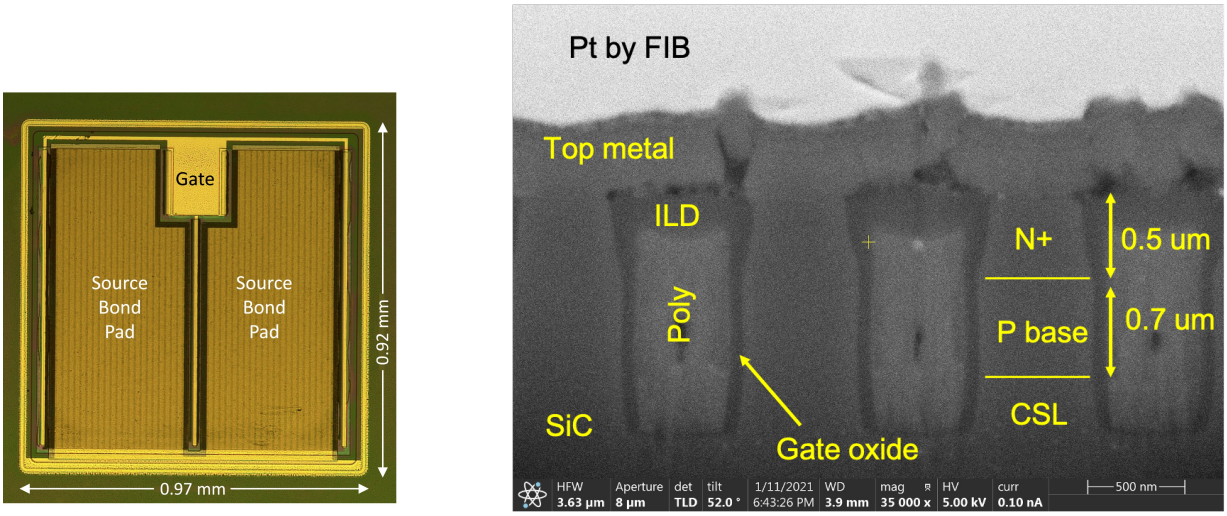


Fig. 11: IMOSFET after ohmic and top metal



(a) (b)

Fig. 12: (a) Optical and (b) FIB cross-section of the completed IMOSFET device

Electrical Characterization

On-state characteristics were measured using a Keithley 4200A-SCS parameter analyzer in a Kelvin configuration, with the source grounded and a voltage sweep applied to the drain. A plot of drain

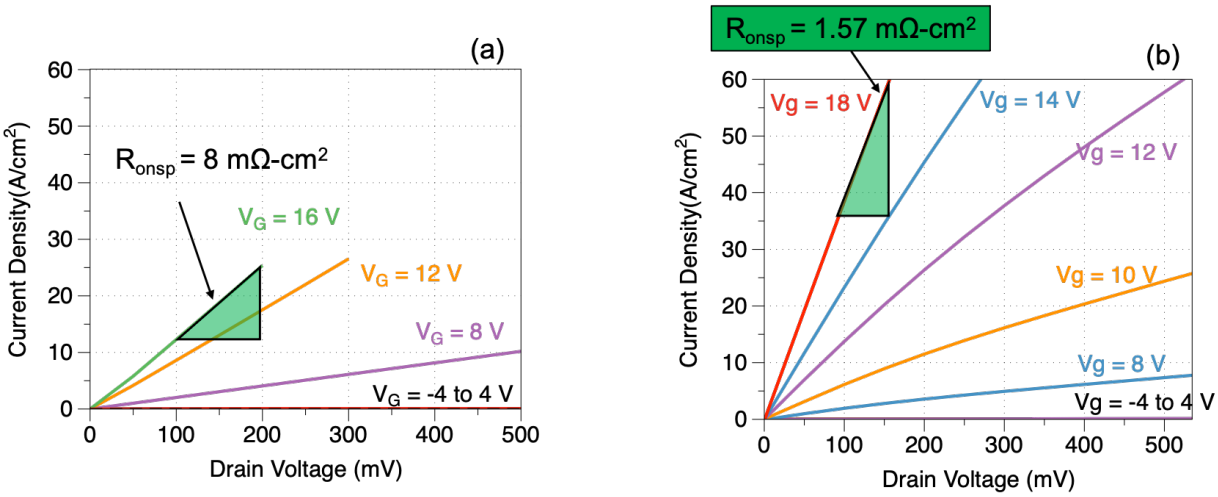


Fig. 13: Output characteristics of (a) non-H_2 etch and (b) H_2 etch device

current density vs. drain voltage for a standard device without a H_2 etch is shown in Figure 13a. The minimum specific on-resistance was 8 mΩ cm^2 at an applied gate bias of 16 V, corresponding to an oxide field of 4 MV/cm. Figure 13b shows I-V characteristics of a device that received a H_2 etch to smooth the sidewalls. The minimum $R_{on,sp}$ was 1.57 mΩ cm^2 at V_G = 16 V. This significantly lower $R_{on,sp}$ is likely due to improved mobility and smoother sidewalls resulting from the H_2 etch.

The blue curve in Figure 14 shows the reverse characteristics of *PiN* diodes on the same wafer as the IMOSFETs, which entered avalanche breakdown at 950 V. The floating field ring (FFR) edge termination consists of an array of 25 1 µm wide concentric rings with an initial spacing of 0.7 µm and a spacing expansion ratio of 7% per ring. The red curve in Figure 14 shows the blocking characteristics of the IMOSFET devices with a gate voltage of -5 V. Drain leakage current at 550 V was high, but the device did not exhibit avalanche breakdown. The leakage has been traced to processing issues during fabrication, and is not expected to impact future devices.

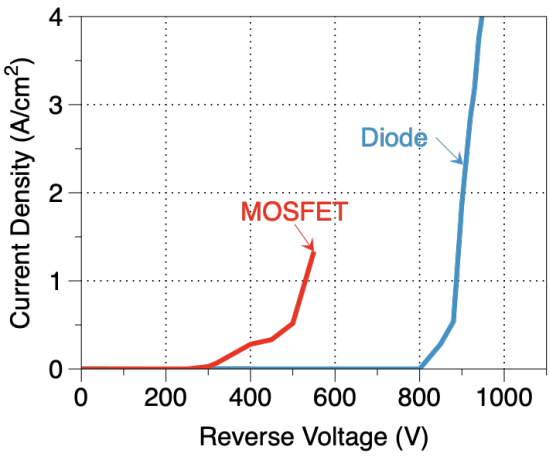


Fig. 14: Off-state leakage of the IMOSFET(red) and reverse breakdown of a *PiN* diode(blue) on the same sample

Summary

For SiC power MOSFETs with blocking voltages in the 400-900 V regime, the MOS channel resistance is the most serious limitation on device performance. We have described a novel, fully self-aligned trench MOSFET with a channel density six times higher than today's commercial SiC MOSFETs. With a 6x higher channel density, the specific channel resistance is reduced by 6x and the overall device specific resistance by 1.5-2.5x, depending on the temperature. A lower resistance allows more devices per wafer, directly reducing die cost. This makes SiC trench MOSFETs ideal candidate to replace SiC DMOSFETs in the main traction inverter of electric vehicles, a market projected to exceed $10 billion USD by 2035.

Aknowledgement

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