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Threshold Voltage Adjustment on 4H-SiC MOSFETs Using p-Doped Polysilicon as a Gate Material

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Abstract. To scale digital circuits, symmetric threshold voltages (V_{th}) for n-type transistors (NMOS) and p-type transistors (PMOS) are important. One step towards this in silicon carbide (SiC) is selecting a p-doped polysilicon (pPolySi). This implementation has been shown in this work with V_{th} being evaluated by five different methods. Furthermore, operating temperatures up to 500 °C and their impact on V_{th} were investigated. It has been successfully demonstrated that elevated temperature shifts V_{th} of both transistor types towards 0 V, whereas changing the gate electrode from n-doped PolySi (nPolySi) to pPolySi shifts V_{th} of both transistor types to more positive values. Both effects are complementary for the PMOS, reaching V_{th} below 4 V.

Introduction

High-bandgap materials like SiC, especially with the 4H-SiC polytype as the most mature one [1], can address operation temperatures beyond silicon's (Si) 200 °C limit [2], making them promising for metal-oxide-semiconductor (MOS) transistors which can operate in harsh environments such as high temperature [2, 3].

Doped polysilicon (PolySi) is a known gate material for transistors due to its favorable interface to the silicon dioxide (SiO_2) gate oxide [4]. Due to the similarity to Si technology, gate stacks of PolySi and SiO_2 are also utilized for SiC transistor fabrication. The selected gate material of a transistor has an essential impact on its V_{th}, which depends on the work function difference between gate and semiconductor material and is, therefore, affected by type and concentration of the corresponding dopants [1]. The work function difference between SiC and PolySi is about 0.9 eV higher with pPolySi compared to nPolySi [5]. The exact value depends on the specific doping concentrations of SiC and PolySi. Consequently, pPolySi increases flat band voltage and thus V_{th} [4]. NMOS have an increased V_{th} with pPolySi, whereas PMOS gain an absolute reduction of V_{th} due to utilizing negative drain and gate voltages.

In summary, utilization of pPolySi for NMOS and PMOS is recommended for more symmetrical V_{th}. Separately doped PolySi or channel implantation [6, 7] are further possible methods to optimize V_{th} for both transistor types individually. Originating from SiC NMOS power technology, absolute V_{th} for NMOS is lower than for PMOS partly due to a development lead of NMOS over PMOS. Hence, symmetrical V_{th} is not yet state of the art for SiC complementary MOS (CMOS). Thus, further research to improve PMOS V_{th} is essential.

This work targets the reduction of the absolute value of V_{th} for SiC PMOS transistors, which were analyzed using five different methods. This enables the option to reduce supply voltage (V_{DD}), making thinner gate oxides possible due to lower power loss on electrical field scaling, and more symmetric V_{th} matching for digital circuits. One example benefitting from this is an inverter [6]. Such change is realized by utilizing pPolySi, similar to the recent work of Hung et al. [7], but focusing on

pure boron ions instead of BF_2. Additionally, implantation and annealing parameters were varied to further improve pPolySi sheet resistance.

Sample Fabrication

To identify a suitable p-doped gate electrode, unstructured Si wafers with 530 nm to 550 nm undoped amorphous polysilicon on top of a low pressure chemical vapor deposition oxide layer with about 650 nm were processed. Afterwards, different combinations of ion implantation and annealing parameters for the pPolySi fabrication were investigated.

Two reference samples were processed as first and last wafer in the batch to monitor tool stabilities. These references have boron implantation with an energy of 50 keV and a dose of $5 \cdot 10^{15}$ cm^{-2} and a subsequent 5 s first annealing step at 1070 °C after 20 s acclimatization at 800 °C. An additional second annealing step at 980 °C for 2 min was performed on all wafers to emulate contact silicidation from the CMOS fabrication process for comparable temperature budgets. Sheet resistance has been monitored across all wafers on 49 data points after both annealing steps.

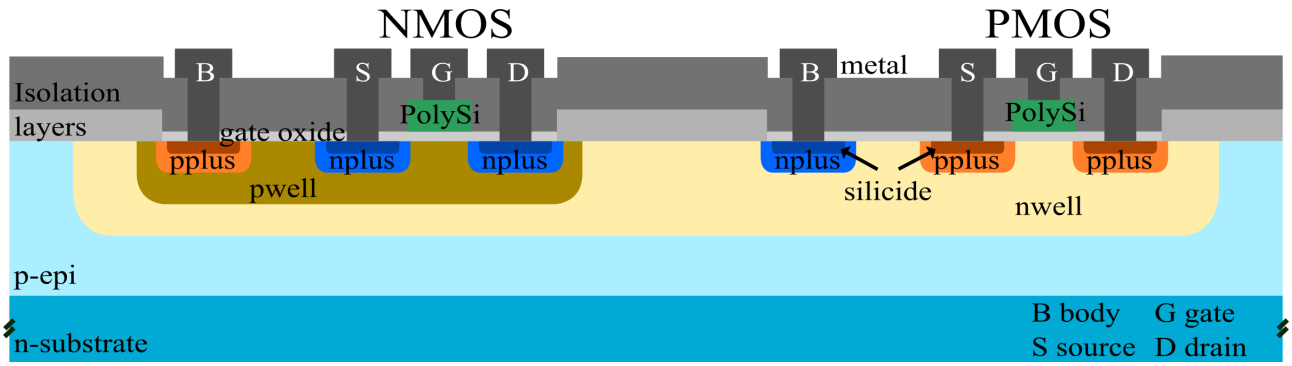

Fig. 1: Schematics of fabricated SiC MOSFETs in cross view.

Transistors, schematically depicted in Fig. 1, were fabricated using a 4H-SiC 1 µm double-well CMOS process with 13 mask layers. Device wells and highly doped contact regions were realized via ion implantation and activation annealing [8]. The resulting surface concentration for nplus and pplus is $5 \cdot 10^{19}$ cm^{-3}, whereas pwell has about $1 \cdot 10^{17}$ cm^{-3} and nwell features roughly $1 \cdot 10^{16}$ cm^{-3}.

The two PolySi doping types were split into separate wafers. In-situ nPolySi and undoped amorphous polysilicon were both deposited at 570 °C with applying higher pressure and higher SiH_4 concentration during nPolySi deposition. Furthermore, PH_3 and Ar were employed in the chamber, while these gases were not present for the undoped amorphous polysilicon. The reference parameters for ion implantation and annealing were applied for pPolySi fabrication.

Table 1: Mean sheet resistance of pPolySi with different parameter variations including the two reference wafers (Ref. I & II). For the other wafers, one parameter each was changed. Energy was varied to 75 keV (↑), dose to $2.5 \cdot 10^{15}$ cm^{-2} (↓) and $7.5 \cdot 10^{15}$ cm^{-2} (↑), temperature to 1150 °C (↑) and time to 10 s (↑) and 15 s (↑↑).

	Ref. I	Energy ↑	Dose ↓	Dose ↑	Temp. ↑	Time ↑	Time ↑↑	No 1st anneal	Ref. II
Average measured after 1st anneal [Ω/sq]	41.4	41.3	76.5	34.1	38.7	40.2	39.7	0.2	41.4
Average measured after 2nd anneal [Ω/sq]	43.1	41.5	76.6	36.7	40.1	41.9	41.3	45.5	42.9
TCAD modelled after 2nd anneal [Ω/sq]	45.2	44.8	65.4	38.3	44.9	45.1	45.0	45.6	45.2

Results and Discussion

Sentaurus Process from Synopsys TCAD was used to simulate different combinations of ion implantation and annealing parameters for the pPolySi, which were then realized on Si wafers with 500 nm undoped amorphous polysilicon on top of a SiO_2 layer. The mean values of the PolySi sheet resistance are listed in Table 1.

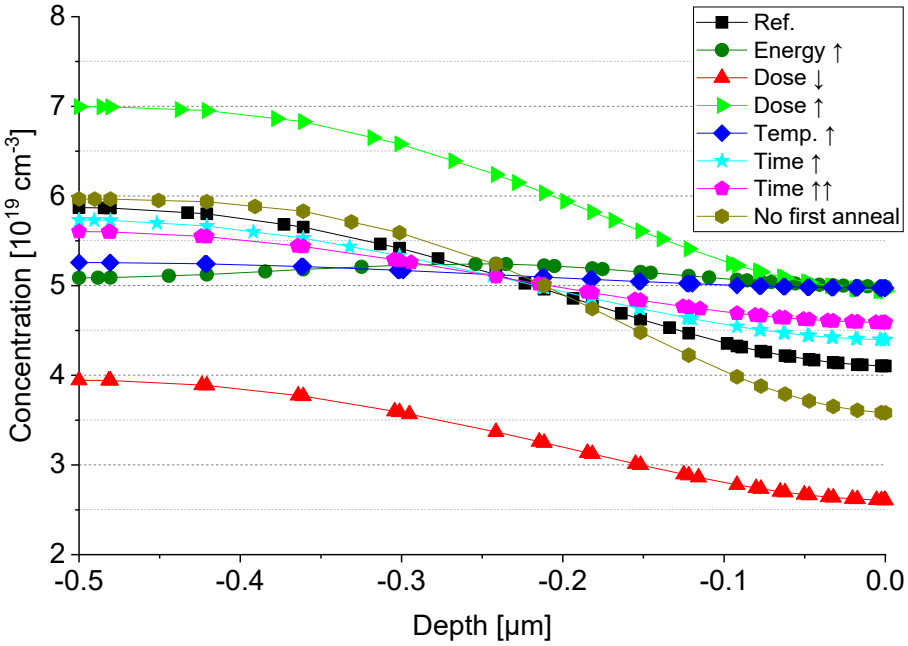

Fig. 2: TCAD modelled active boron concentration in the polysilicon after second annealing step with the polysilicon/SiO_2 interface at 0 µm depth.

A higher implantation dose results in a higher active dopant concentration on the polysilicon surface and thus lower sheet resistance compared to the reference samples. Increasing annealing time or temperature distributes the ions more equally across the whole thickness, as shown in Fig. 2. This is also possible by adapting the energy to shift the peak of the implantation profile deeper into the PolySi layer, from near the surface towards about half of its total thickness.

Differences in sheet resistance between simulation and processed wafers could be attributed to varying PolySi thickness, which was up to 10 % higher than targeted. Additionally, the actual heating and cooling process in the annealing chamber were not included in the simulation. Nevertheless, the investigated parameter variations could already successfully reduce the sheet resistance to about 37 Ω/sq, around 14 % lower than the references. Subsequent experiments could combine different parameter variations for further reduction to try to match nPolySi sheet resistance of about 14 Ω/sq.

Both PolySi variants show reasonable transfer characteristics in MOS transistors, presented in Fig. 3. The transistors used in this experiment have a similar gate width and length of 20 µm each. Therefore, short and narrow channel effects on threshold voltage can be neglected. At higher V_G, the impact of drain and source resistance results in I_D saturation. Consequently, the first section of the transfer characteristics should be considered for V_{th} comparison.

Even at 500 °C, temperature stability is successfully demonstrated using this approach. Increasing temperature shifts the graphs, and thus V_{th}, towards 0 V. Substituting nPolySi for pPolySi with the reference parameters increases V_{th}, shifting it to more positive values for both transistor types. However, this increase of V_{th} for NMOS provides more symmetric V_{th} values towards low voltage 4H-SiC CMOS technology, which is also a prerequisite for voltage scaling following Moore's law.

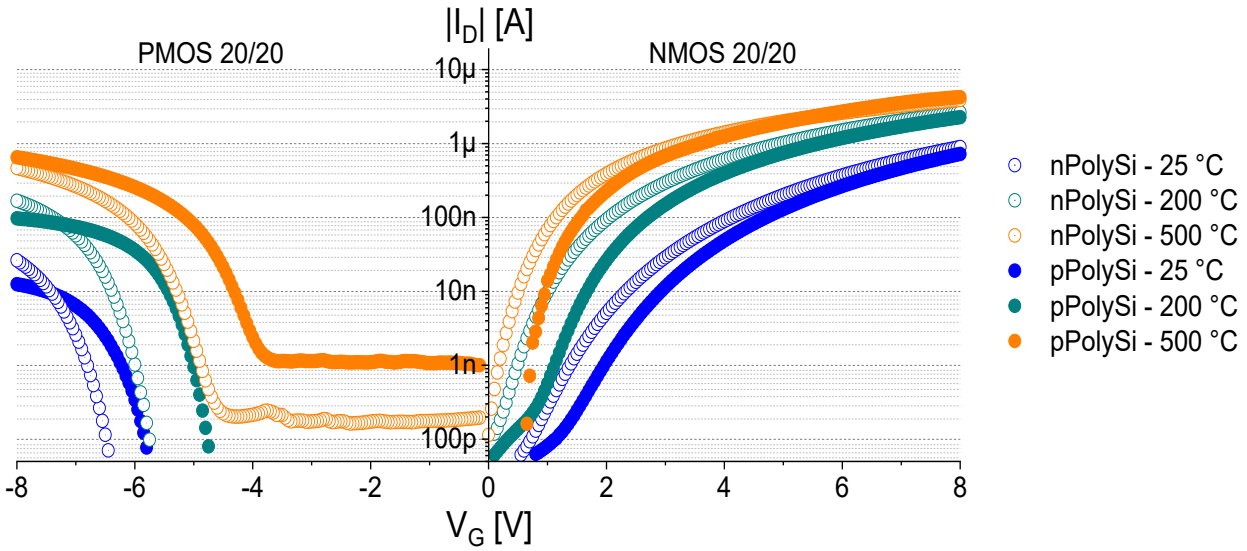

Fig. 3: Transfer characteristics at V_D = 0.5 V of PMOS and NMOS with differently doped gate material at selected temperatures.

To calculate V_{th} for each data set, literature provides numerous different methods based on Si [9]. In this work, five different methods were selected for the evaluation, namely extrapolation in the linear region method (ELR), transconductance extrapolation method in the linear region (GMLE), second-derivative method (SD), ratio method (RM) and extrapolation method in the saturation region (ESR). The resulting V_{th} values for each graph from Fig. 3 are depicted in Table 2.

Table 2: Threshold voltages of the experimental data evaluated by five different methods according to Ortiz-Conde et al. [9]. Values are listed as absolutes.

			V_{th} [V]				
			ELR	GMLE	SD	RM	ESR
NMOS	pPolySi	25 °C	8.98	3.26	6.75	7.44	3.03
		200 °C	6.31	1.44	2.90	5.98	1.41
		500 °C	2.97	0.68	1.68	7.42	0.75
	nPolySi	25 °C	8.46	2.68	6.00	6.47	2.44
		200 °C	4.56	0.77	2.15	5.50	0.74
		500 °C	2.11	0.19	1.20	1.70	0.31
PMOS	pPolySi	25 °C	6.22	5.55	6.25	18.73	5.77
		200 °C	5.05	4.38	5.00	7.41	4.65
		500 °C	4.73	3.84	4.55	10.39	3.98
	nPolySi	25 °C	7.22	6.43	7.15	12.03	6.57
		200 °C	6.54	5.78	6.45	13.59	5.96
		500 °C	5.73	4.79	5.55	6.88	4.94

With ELR, a tangent at the maximum slope of the I_D-V_G curve is extrapolated to I_D = 0 V. Thus, parasitic series resistances and mobility degeneration can cause the linear region to deviate from its ideal form, which will cause shifted V_{th}. While yielding plausible results for the PMOS, NMOS results seem to be overestimated. Therefore, it is not ideal for the measured devices.

RM eliminates parasitic series resistances and mobility degeneration by utilizing $I_D/gm^{0.5}$-V_G characteristics, with gm being the transconductance, and extrapolating the linear region to the x-axis intersection for determining V_{th}. However, for the measured devices, the linear region is not clearly distinguishable due to noise enhanced by dividing the current by the square root of its first derivative.

This causes some results to be significantly wrong, e.g., the PMOS with pPolySi at room temperature. Also, the clear trend of lower V_{th} at higher temperature is not consistently present, making this method not applicable for the devices.

The remaining three methods are the following: GMLE, which extrapolates the tangent on the maximum slope of the gm-V_G curve to I_D = 0 V, SD, where V_{th} is the maximum of the derivative of the gm-V_G curve, and ESR, where the tangent at the maximum slope of the $I_D^{0.5}$-V_G curve is extrapolated to the x-axis intersection. All three methods show similar trends, as depicted in Fig. 4. For better comparison, V_{th} of PMOS, while being negative, is displayed as absolute values.

It is assumed, that the absolute V_{th} differences between NMOS and PMOS shifts are at least partially attributed to the different SiC doping. The pwell has approximately one order of magnitude higher dopant concentration at the surface compared to the nwell, which impacts the SiC work function.

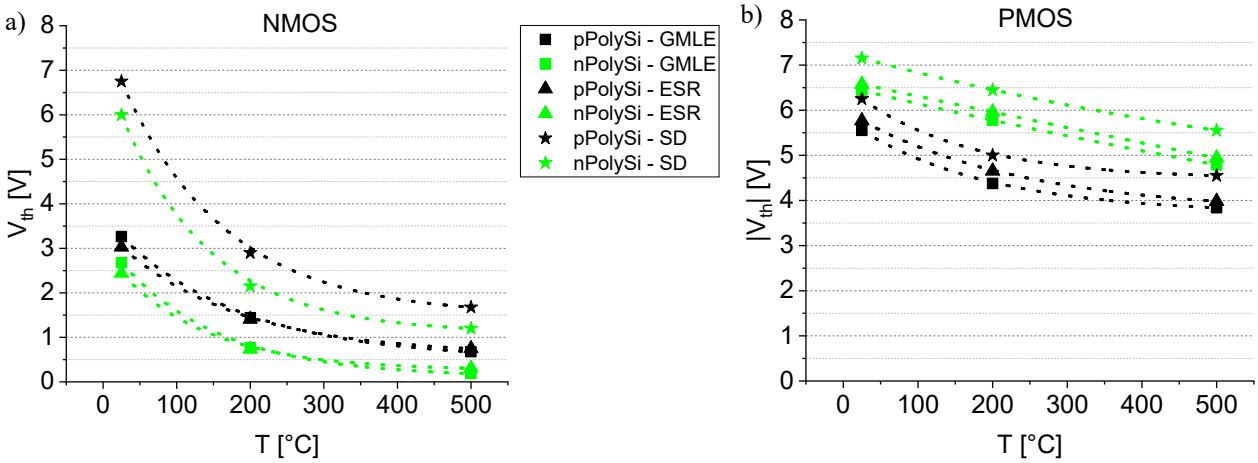

Fig. 4: Evaluated threshold voltages for a) NMOS and b) PMOS with differently doped PolySi gate by GMLE, SD and ESR at selected temperatures. Dotted lines represent an exponential decay fit.

It is evident that V_{th} is shifted towards 0 V with increasing temperature, consistent with physics. This temperature dependence of V_{th} results from two of its components, the contact potential difference between substrate and gate electrode and the band bending, being affected by temperature. For equal doping types of substrate and gate, such as NMOS and nPolySi, these effects are working against each other, yielding a negative temperature coefficient. However, when changing the channel doping type to form a PMOS, an addition happens, resulting in a positive coefficient [10].

From the limited number of measured temperatures, this trend seems to decay exponentially with increased temperature for NMOS. For PMOS, the same trend with noticeable lower reduction at the beginning is observed on pPolySi, whereas the nPolySi follows near linear decrease.

SD values are only slightly higher for PMOS, but have, like ELR, noticeably higher results for NMOS, especially at lower temperatures. A possible explanation for this overestimation could be the high sensitivity to measurement error and noise. Interestingly, ESR has very similar results as GMLE despite being an evaluation method in the saturation regime, compared to the other four working in the linear regime. In conclusion, all three methods are applicable for the measured PMOS devices, whereas only GMLE and ESR should be used for the measured NMOS ones. In addition, these two provide results with the highest conformity for both NMOS and PMOS among the methods.

Compared to nPolySi, pPolySi increases V_{th} for PMOS by roughly 1.05 V ± 0.3 V across all measured temperatures, consistent with the work function difference described in literature [5]. For NMOS, a shift of approximately 0.6 V ± 0.15 V across all measured temperatures is observed. Currently, the reason for the relatively lower V_{th} shift compared to PMOS is still under investigation.

Further data from additional devices including variations in channel width and length are required to gather more precise statistics. Besides, higher temperature resolution is needed to describe the

changes over the temperature in more detail. For precise comparison, SiC dopant concentration should be comparable for both transistor types.

Nevertheless, for digital circuitry, it would be possible to reduce the required V_{DD} with pPolySi by about 1.65 V ± 0.45 V when only taking V_{th} into account and other conditions are excluded. Additionally, devices like an inverter will benefit by the symmetric matching of V_{th} using pPolySi.

Summary

To summarize, pPolySi has been integrated into the SiC CMOS technology with optimized parameters regarding reduced sheet resistance being available for future fabrication runs. The intended absolute V_{th} reduction for pPolySi PMOS and V_{th} adjustment between NMOS and PMOS with pPolySi gate material has been successfully demonstrated, thus, contributing to the research towards symmetrical V_{th} on SiC CMOS for digital circuits such as an inverter.

Furthermore, five different evaluation methods for V_{th} have been compared and their applicability for the processed SiC transistors has been discussed. GMLE and ESR are the recommended choices for both measured MOS types while ELR and SD are also suitable for PMOS but resulting in slightly overestimated values. Finally, high temperature measurements up to 500 °C have been successfully performed for SiC transistors and the V_{th} shift towards 0 V at higher temperatures has been highlighted.

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