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Demonstration of SiC Trench Gate MOSFETs with Narrow Cell Pitch Using Source Self-Aligned Process

Shinichi Kimoto[1,a*], Ryosuke Iijima[2,b] and Shinsuke Harada[1,c]

[1]National Institute of Advanced Industrial Science and Technology, 16-1 Onogawa, Tsukuba, Ibaraki 305-8569, Japan

[2]Toshiba Corporation, 1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, Kanagawa 212-8582, Japan

[a]shinichi1.kimoto@toshiba.co.jp, [b]ryosuke.iijima@toshiba.co.jp, [c]s-harada@aist.go.jp

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Abstract. The SiC trench gate MOSFET with narrow cell pitch is demonstrated using a process in which the n^+ source is self-aligned to the trench gate. A minimum cell pitch of 1.6 μm, which is difficult to achieve using the conventional device structure, is easily fabricated by applying a deep n^+ source and a buried interlayer dielectric structure. The cell pitch reduction indicates a beneficial trend that contributes to a decrease in the specific on-resistance and an increase in the breakdown voltage. The process and structure are promising for further improving SiC power device characteristics.

Introduction

SiC trench gate MOSFETs are generally more suitable than planar gate MOSFETs for cell pitch (W_{cell}) reduction. A narrow W_{cell} is desirable to reduce the specific on-resistance ($R_{on}A$), especially below the 1200 V-class, where the ratio of the channel resistance is high. However, a W_{cell} reduction causes difficulties in the alignment and patterning processes. The self-aligned process is utilized to overcome these issues. Recent studies have reported the conventional type of single-trench gate MOSFETs (ST-MOSFETs) using the self-aligned process, such as the p^+ shielding region under the gate trench and the segmented contact regions [1-4]. With further reduction in W_{cell} in the ST-MOSFETs, difficulties in establishing ohmic contact appears due to the contact aperture limit are observed next. In this study, we developed an n^+ source self-aligned process adjacent to the gate trench, which realizes the stable fabrication with narrow W_{cell} = 2.0 μm or less, and demonstrated deep-channel MOSFETs (DC-MOSFETs) fabricated using this self-aligned process. This device has a deep n^+ region and a buried interlayer dielectric (ILD), which allow for a significantly narrow W_{cell}.

Design Concept and Fabrication

Figure 1 shows the schematic cell structures of (a) ST-MOSFET and (b) DC-MOSFET. The structural differences between ST-MOSFET and DC-MOSFET are n^+ source depth and ILD aperture width. For the ST-MOSFET, W_{cell} is represented by

$$W_{cell} = W_t + 2W_n + W_p = W_t + 2W_{nf} + W_p + 2W_{GS}, \quad (1)$$

where W_t is the trench width; W_n is the n^+ width; W_p is the p^+ width; W_{GS} is the gate-source (GS) distance; and $W_{nf} = W_n - W_{GS}$ is the n^+ footprint width. W_{GS} requires a certain thickness to obtain a low GS failure rate and low GS capacitance. Additionally, if the ILD width and its aperture width are defined as W_{line} and W_{space}, respectively, W_{cell} reduction sacrifices W_{space} owing to the constraint $W_{line} = W_t + 2W_{GS}$. Consequently, the ILD aperture and metal coverage failure associated with W_{space} reduction, and ohmic contact failure where $W_{nf} < 0$, are likely to occur because of $W_{space} = 2W_{nf} + W_p$. On the other hand, W_{cell} in the DC-MOSFET is given by

$$W_{cell} = W_t + 2W_n + W_p = W_t + 2W_{nf} + W_p. \quad (2)$$

It follows that $W_{nf} = W_n$. Because the n^+ source is formed deeper than that in the ST-MOSFET, the gate electrode is formed deeper, and the ILD is buried in the trench. Thus, a certain thickness of W_{GS} is retained in the vertical direction, and W_{GS} is excluded from the cell parameters, which allow the DC-MOSFET to reduce the W_{cell} significantly. Furthermore, the strict alignment control at the ILD aperture is unnecessary because W_{line} only needs to satisfy $0 \leq W_{line} < W_t$. The ILD aperture, metal coverage, and ohmic contact failure do not occur easily because W_{space} is maintained wider than that in ST-MOSFET. As stated above, the DC-MOSFET is advantageous in reducing the W_{cell} with stable processes.

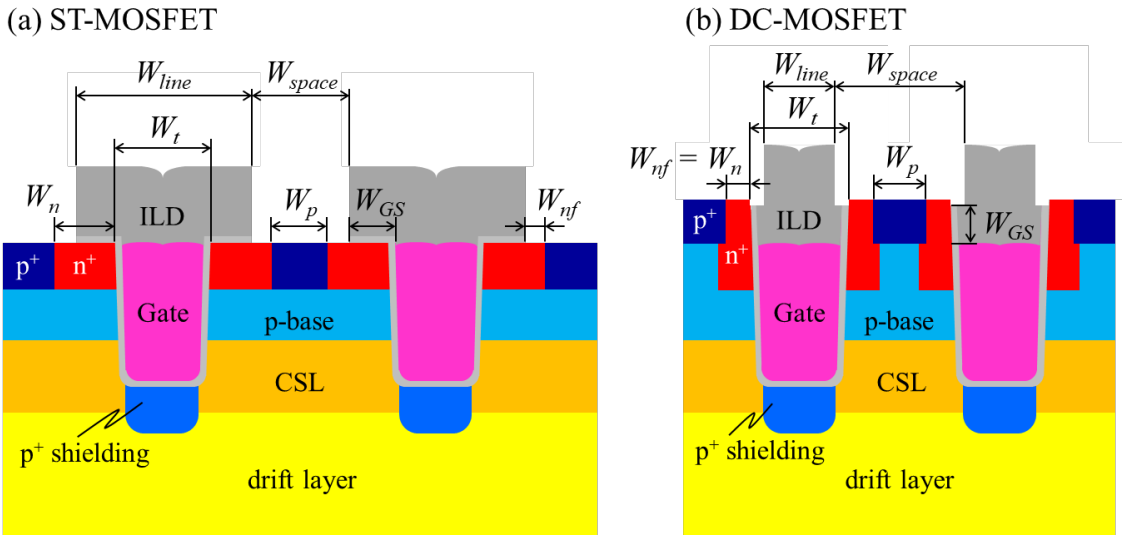

Fig. 1. Schematic cell structures of (a) ST-MOSFET and (b) DC-MOSFET.

Figure 2 illustrates the main fabrication procedure for the DC-MOSFETs. A drift layer, which concentration and thickness were 1.5×10^{16} cm^{-3} and 4.7 μm, was prepared on a substrate for the 650 V-class, and a current spreading layer (CSL) was then stacked on the drift layer. The bottom half of the n^+ and p-base regions were formed via ion implantation in the first in-process epitaxial growth layer, whereas the upper half of the n^+ source region was formed via ion implantation in the second in-process epitaxial growth layer. Subsequently, without removing the SiO_2 hard mask, the first SiO_2 sidewall was formed, and a SiC trench narrower than the width of the P implantation was formed by dry etching. A p^+ shielding region was then formed by Al implantation with the second SiO_2 sidewall. Therefore, both the p^+ shielding region and n^+ source region were formed using the self-aligned process to the trench gate.

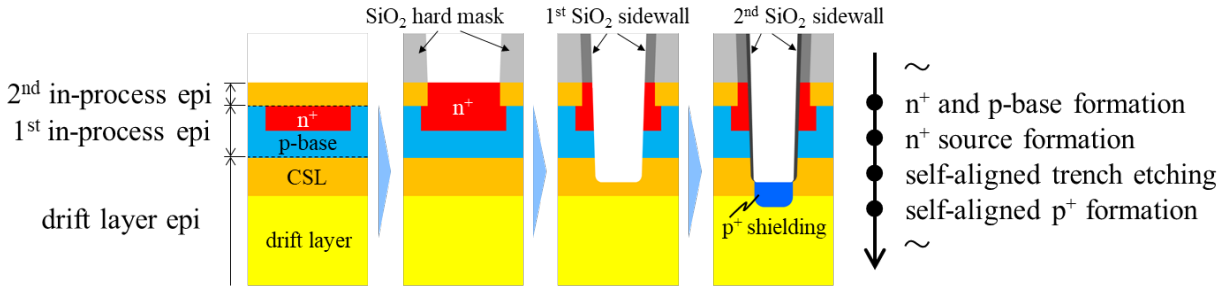

Fig. 2. Main fabrication procedure including the n^+ source self-aligned process for the DC-MOSFET.

Experimental Results

Demonstration. Figure 3 shows the cross-sectional SEM image of (a) ST-MOSFET with W_{cell} = 2.0 μm and (b) DC-MOSFET with W_{cell} = 1.6 μm. The DC-MOSFET was fabricated using the n^+ source self-aligned process, whereas the ST-MOSFET did not use the process. For the ST-MOSFET, an Al void and a short W_{nf} due to the narrow W_{space} were observed. Moreover, because W_{nf} is slightly different on the left and right sides of the trench gate owing to the misalignment of both the upper half of the n^+ source region and the ILD aperture to the trench gate, there is a concern that $W_{nf} < 0$ μm on at least one side when $W_{cell} < 2.0$ μm. However, for the DC-MOSFET, the Al coverage is satisfactory because of the relatively wide W_{space}, and W_{nf} is also wide enough. W_{nf} is formed equally on both sides of the trench gate because it is not affected by the misalignment of the ILD aperture when $W_{line} < W_t$. Thus, owing to the ability to form the W_{GS} in the vertical direction, trench gate MOSFETs with $W_{cell} < 2.0$ μm are easily realized.

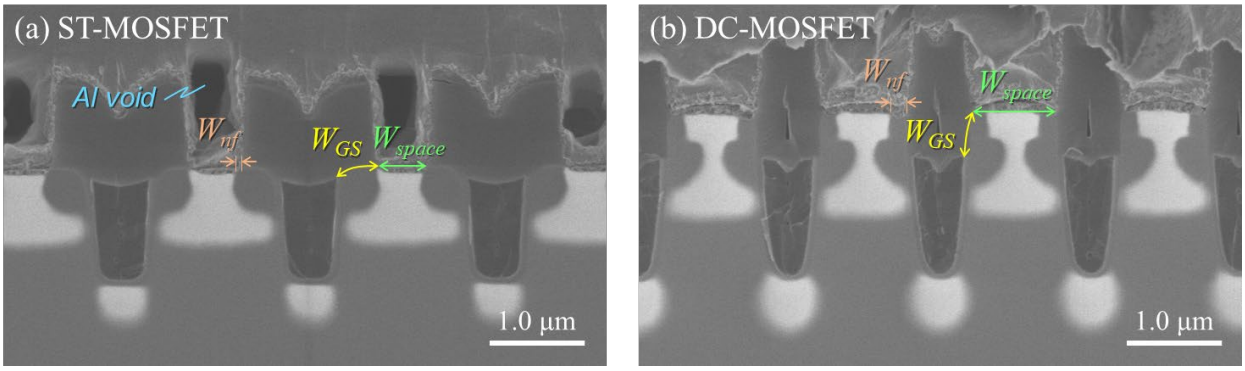

Fig. 3. Cross-sectional SEM images of (a) ST-MOSFET with W_{cell} = 2.0 μm and (b) DC-MOSFET with W_{cell} = 1.6 μm.

Figure 4 shows (a) the J_D-V_{DS} and (b) J_D-V_{GS} characteristics for a DC-MOSFET with W_{cell} = 1.6 μm. The J_D-V_{DS} curves display five levels at V_{GS} = 0, 5, 10, 15, and 20 V. At V_{GS} = 20 V, R_{onA} = 1.22 mΩcm^2 was obtained at J_D = 18.9 A/cm^2 (I_D = 1 A). The J_D-V_{GS} curve for the same device represents V_{th} = 3.2 V at V_{DS} = 1 V and J_D = 0.3 A/cm^2 (I_D = 18 mA). The DC-MOSFET using the n^+ source self-aligned process demonstrated desirable static characteristics.

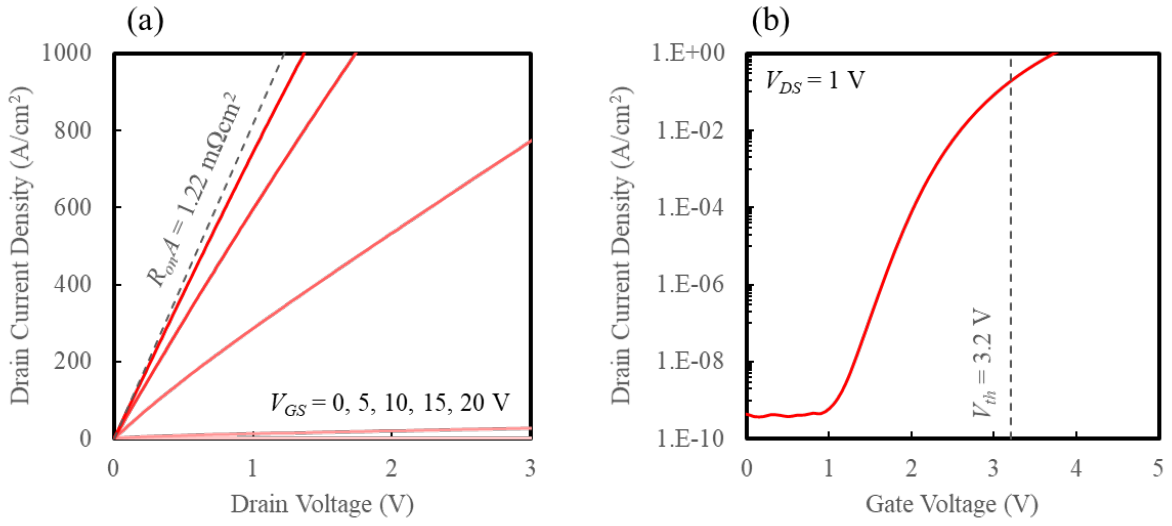

Fig. 4. (a) J_D-V_{DS} and (b) J_D-V_{GS} characteristics for a typical DC-MOSFET with W_{cell} = 1.6 μm.

Cell Pitch Dependence of Static Characteristics. Figure 5 (a) depicts the W_{cell} dependence of R_{onA} (the median value of approximately 30 devices) at V_{GS} = 20 V when the JFET width is varied for both the ST-MOSFETs and DC-MOSFETs. The median values of V_{th} for the ST-MOSFETs and the DC-MOSFETs with W_{cell} = 2.0 μm are 3.9 V and 3.1 V, respectively. The reduced cell pitch shows a trend toward reduced R_{onA}, especially for the DC-MOSFETs, where the smallest R_{onA} was obtained. This suggests that the effect of the decrease in R_{ch} owing to the increased channel density is larger than that of the increase in the JFET resistance (R_{JFET}) owing to the wide JFET width, even at W_{cell} = 1.6 μm. The solid lines representing the measurement results include the substrate resistance (R_{sub}) with thickness of 360 μm and 333 μm for ST-MOSFETs and DC-MOSFETs, respectively. The dotted lines represent the case where the substrate thickness is reduced to 100 μm (R_{sub} = 0.20 mΩcm^2). Particularly, for the DC-MOSFETs with W_{cell} = 1.6 μm, the R_{onA} is reduced to 0.75 mΩcm^2. Figure 5 (b) presents the simulated results of the R_{onA} components for the DC-MOSFET with W_{cell} = 1.6 μm. Excluding the removable substrate resistance of 0.47 mΩcm^2, R_{ch} is regarded as the largest component despite the high channel density. It suggests that further R_{onA} reduction is possible by reducing W_{cell} less than 1.6 μm, shortening the channel length (L_{ch}) and improving the mobility (μ_{FE}). For example, in DC-MOSFETs with W_{cell} = 1.4 μm, if L_{ch} is halved and μ_{FE} is doubled, R_{onA} is expected to be 0.55 mΩcm^2. In this study, L_{ch} and μ_{FE} are about 0.46 μm and 23 cm^2/Vs, respectively.

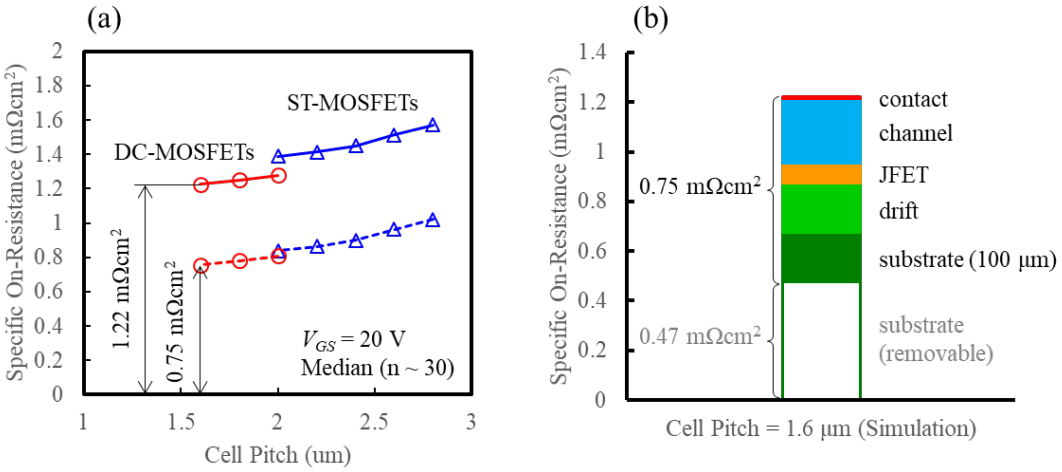

Fig. 5. (a) Cell pitch dependence of R_{onA} at V_{GS} = 20 V for both the ST-MOSFETs (blue triangle) and DC-MOSFETs (red circle). The solid and dotted lines indicate the actual measurement results and expectation for a substrate thickness of 100 μm, respectively. (b) Simulated results of R_{onA} components for the DC-MOSFET with W_{cell} = 1.6 μm.

Figure 6 (a) shows the breakdown characteristics at V_{GS} = 0 V for the DC-MOSFETs with W_{cell} = 2.0, 1.8, and 1.6 μm. The breakdown voltage (V_B) tends to increase with the W_{cell} reduction (JFET width reduction), and the device with W_{cell} = 1.6 μm has V_B = 750 V. However, it is lower than 900 V of PiN diode. Figure 6 (b) shows the simulated results of the electric field at V_{DS} = 650 V for the DC-MOSFETs with each W_{cell}. The cell pitch reduction suppresses the electric field for the shielding structure at the bottom of the trench gate. This is attributed to the suppression of the potential drop near the channel. Additionally, a reduction in the W_{cell} also contributed to the relaxation of the electric field for the gate oxide at the bottom corner of the trench gate, which is advantageous for improving the reliability of the trench gate structure.

Figure 7 exhibits the R_{onA} and V_B trends for the W_{cell} reduction. The results up to W_{cell} = 1.6 μm demonstrated in this study indicate that both the R_{onA} and V_B characteristics improve simultaneously with the W_{cell} reduction. The R_{JFET} does not increase under this CSL concentration of 6.0×10^{16} cm^{-3} because the JFET width of 0.9 μm is wide even with W_{cell} = 1.6 μm. The novel structure and process for DC-MOSFETs which enable easy fabrication of the device with W_{cell} < 2.0 μm reveal that further W_{cell} reduction and characteristics improvement are possible in the future.

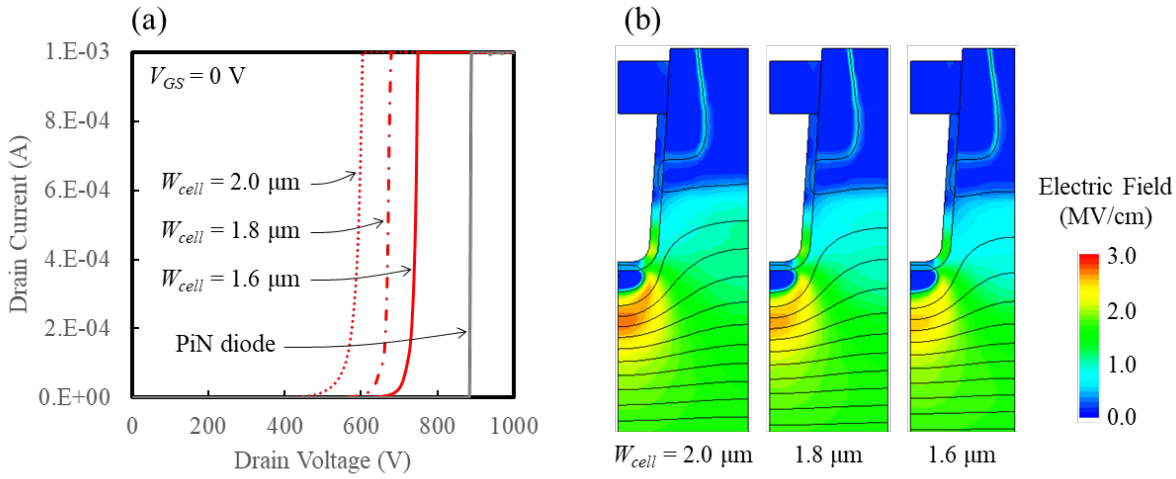

Fig. 6. (a) Breakdown characteristics at V_{GS} = 0 V for the DC-MOSFETs with W_{cell} = 2.0 (dotted), 1.8 (dashed), 1.6 μm (red solid) and PiN diode (gray solid). (b) Simulation results of the electric field at V_{DS} = 650 V for the DC-MOSFETs with each W_{cell}.

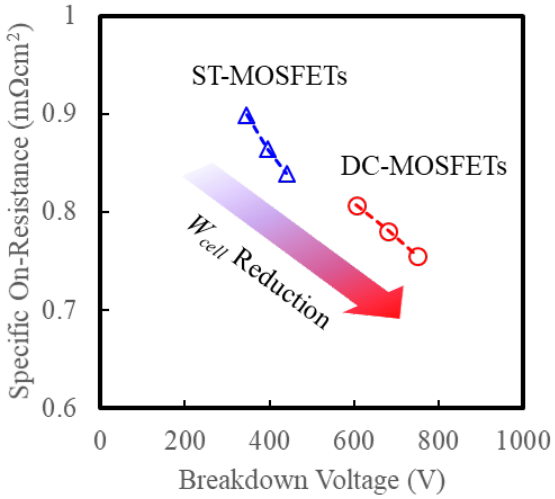

Fig. 7. Trend of R_{onA} and V_B for W_{cell} reduction.

Summary

The first prototype DC-MOSFET applying the n^+ source self-aligned process was demonstrated. DC-MOSFETs with a deep n^+ source and buried ILD can reduce the W_{cell} efficiently than conventional ST-MOSFETs, and are less prone to process failures. The DC-MOSFET with a minimum W_{cell} of 1.6 μm was demonstrated, and it exhibited R_{onA} = 0.75 mΩcm^2 (in the case of a substrate thickness of 100 μm) and V_B = 750 V. Because the reduced W_{cell} can simultaneously improve the R_{onA} and V_B characteristics, the DC-MOSFET using the n^+ source self-aligned process is one of the promising structures for further development in SiC power MOSFETs.

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