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Assessing, Controlling and Understanding Parameter Variations of SiC Power MOSFETs in Switching Operation

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Abstract: Semiconductor manufacturers and researchers have recently revealed that under specific bipolar gate switching conditions SiC MOSFETs exhibit parameter drift dynamics different from those typically observed in static qualification stress tests. In response to this finding, we present an approach for assessing the worst-case drift of data-sheet-relevant electrical parameters in a simple and transparent manner for a large variety of application profiles. We also introduce an empirical model that may explain the drift dynamics observed under gate switching stress; and discuss a recently developed interface characterization technique that has the potential to reveal the nature of point defects at the SiC/SiO_2 interface presumably related to the gate switching instability in SiC MOSFETs.

Introduction

SiC power MOSFETs enable operation at much higher switching frequencies and at lower losses compared to silicon-based power semiconductors. This makes it possible to build power electronic circuits with smaller cooling units, and reduced size in passive components. For fast switching operation, a wide and flexible gate drive operation window is required including margins for over- and undershoots and negative gate turn-off voltages to allow save turn-off. Within their lifetime, SiC MOSFETs are exposed to a large number of bipolar gate-switching events that can lead to systematic degradation of electrical parameters such as the threshold voltage and the on-resistance due to gate switching instability (GSI) [1-7].

To secure reliable operation of SiC MOSFETs in different applications and/or mission profiles, it is crucial to assess the worst-case drift that can occur till the end of the application profile [5]. This allows for the consideration of potential variations in electrical parameters in the system design, if required. In this paper we present an approach for assessing worst-case drifts and illustrating them flexibly for arbitrary mission profiles.

Along with the ability to determine the worst-case drifts, it is also crucial to have in mind a microphysical model that is consistent with the observed stress parameter dependencies. Based on this model one can arrive at the most critical application conditions and derive approaches to contain the problem in the device manufacturing. This would help in keeping parameter variations due to GSI under control and within acceptable limits. We will discuss our model in detail later in this paper and explain how it fits the recent experimental observations of various groups [4-7].

Another important step towards a deeper understanding of the gate switching stress (GSS) degradation mechanism is to study the nature of point defects that are involved in bipolar switching events. These defects are predominantly recombination centers at the SiC/SiO_2 interface that promote the transition of large numbers of conduction band electrons into the valance band in every single switching cycle. We recently discovered that a small fraction of these recombination events is radiative [8]. Emitted photons from the SiC/SiO_2 interface can be detected at the reverse side of fully processed chips after etching away parts of the backside metallization. Their spectrum is virtually a

fingerprint of the interface and the peaks in the spectrum can be correlated to the density functional theory (DFT) simulations to reveal the microphysical structure of the point defects [8-10].

Assessment and Illustration of Worst-Case Drift

Like the classical bias temperature instability (BTI), GSI is also an intrinsic degradation mechanism of the SiO_2/SiC interface that is inherently present in all SiC MOSFETs. The mechanism affects the threshold voltage of devices in a very systematic and reproducible way. This means that same stress conditions typically lead to similar and predictable drift dynamics within one device technology. There can be, however, large differences in GSI induced drifts seen on devices from different manufacturers [4,7]. Thus, it is evident that the device structure and/or the device processing may significantly impact GSI.

One key finding of previous studies was that at any given gate switching and temperature conditions, the resultant V_{th} drift depends exclusively on the number of switching events [1,3,5,11]. The total stress time as well as the duty cycle is only of minor or even no importance [3,4]. Consequently, stress frequencies higher than normal operation can be used to reach the end-of-mission-profile drift for a certain application within a timeframe much shorter than the targeted product's lifetime. By simply stressing devices up to their maximum number of switching cycles, a frequency-accelerated GSS test can directly determine the evolution of GSI induced V_{th} drift for arbitrary application profiles. An exemplary V_{th} drift evolution curve using a stress frequency of 500 kHz and maximum data sheet conditions for gate voltage and temperature is shown in Fig. 1.

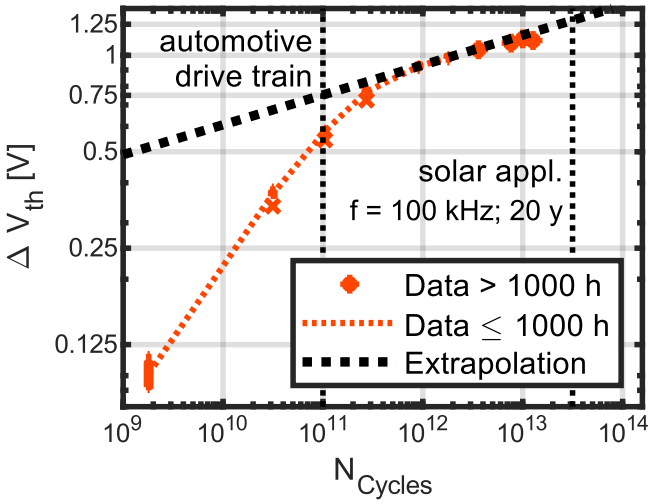

Fig. 1: Example of a worst-case V_{th} drift evolution curve due to GSS performed at maximum data sheet conditions and 500 kHz. The vertical dashed lines indicate the total number of switching cycles of a typical automotive drive train application and a typical solar application. The dashed line in bold indicates the power-law fit of data points in the saturation regime but within 1000 h of total stress time. Additional data points >1000 h fit very well with the power-law extrapolation. At lower number of switching cycles ($< 10^{11}$) the power-law fit overestimates the V_{th} drift due to GSI, and thus can be considered the worst-case scenario

Fig. 1 shows that the slope of the V_{th} drift evolution curve of the tested SiC MOSFET devices is higher for lower number of switching cycles ($< 10^{11}$ cycles) and tends to saturate when exceeding 10^{11} – 10^{12} switching cycles. In the saturation regime, we may conservatively approximate the drift of applications that reach even higher numbers of switching cycles during their lifetime by extrapolating the measured drift evolution curve using a power-law fit. For the fit shown in Fig. 1 we used data points recorded in the saturation regime but within 1000 h of stress time ($\approx 2 \cdot 10^{12}$ cycles) [2,5]. Additional data points recorded up to 7000 h of stress time ($> 10^{13}$ cycles) confirm the validity of the

power-law fit. The drift curve shown is Fig. 1 can be considered the worst-case for this technology because the devices were stressed to the maximum allowed gate voltage and temperature conditions mentioned in the datasheet.

A V_{th} drift evolution curve like the one presented in Fig. 1 can be further used to calculate the drift of other related electrical parameters such as the on-resistance (R_{DSON}). When the V_{th} increases, the R_{DSON} also increases because the channel overdrive ($V_{GS} - V_{th}$) is reduced. By using characterization data of unstressed devices, c.f. Fig. 2, the corresponding R_{DSON} drift (ΔR_{DSON}) can be extracted from the V_{th} drift data for any given temperature or overdrive condition assuming that any R_{DSON} variation is only due to changes in overdrive. We did not find any channel mobility degradation in our devices due to GSI.

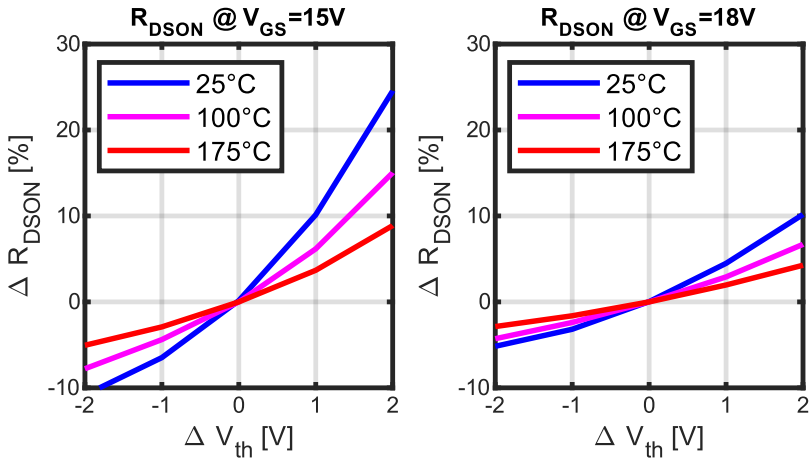

Fig. 2: Example of the dependence of R_{DSON} on stress-induced changes in overdrive ($V_{GS}-V_{th0}-\Delta V_{th}$). Curves are extracted from R_{DSON} characterization data measured at different overdrives and temperatures

Here, it is important to note that changes in V_{th} predominantly affect the channel resistance (R_{CH}) as a component of the total R_{DSON}:

$$R_{DSON} = R_{CH} + R_{JFET} + R_{Drift} + R_{Sub} \quad . \tag{1}$$

Other components of the total R_{DSON} are JFET (R_{JFET}), drift zone (R_{Drift}), and substrate (R_{Sub}) resistance. The relative contribution of R_{CH} to the total R_{DSON} decreases with increasing operating temperature, increasing gate voltage overdrive, and increasing drift zone resistance, therefore, the GSI induced R_{DSON} variations are naturally less pronounced for higher on-state gate voltages, higher operating temperatures, and for higher voltage class devices. This is shown in Fig. 3, where we converted the extrapolated V_{th} drift evolution curve shown in Fig. 1 into relative ΔR_{DSON} drift evolution curves using the characterization data shown in Fig. 2.

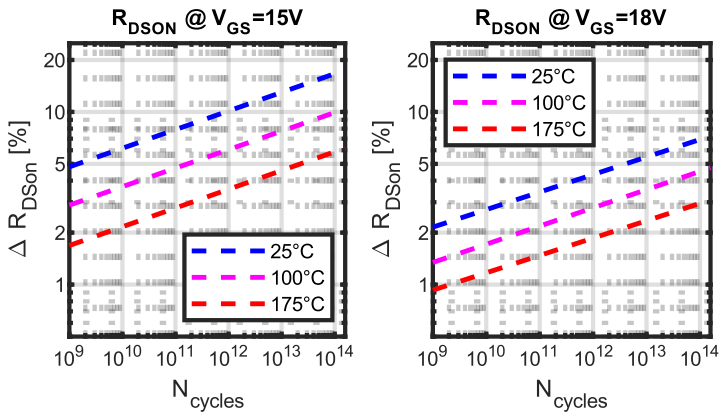

Fig. 3: Examples of worst-case relative R_{DSON} drift evolution curves derived from the V_{th} drift data shown in Fig. 1 and the characterization data shown in Fig. 2

Providing worst-case R_{DSON} drift curves, like the ones presented in Fig. 3, in technology application notes can help customers directly to extract the maximum drift that can be expected for a given technology in a specific application [12]. For the exemplary technology presented in this paper, one can infer, for instance, that at a gate voltage of 18 V and at an operation temperature of 100°C roughly 5% R_{DSON} drift can be expected in the worst case after 10^{14} switching cycles. Real-life operation conditions below maximum allowed data sheet values will lead to the same or even lower R_{DSON} drifts over a lifetime.

A Proposal for a Microscopic Model for GSI

Besides the ability to predict parameter variations due to GSI for specific applications, we also strived for a microscopic understanding of the degradation mechanism to explain the experimental observations.

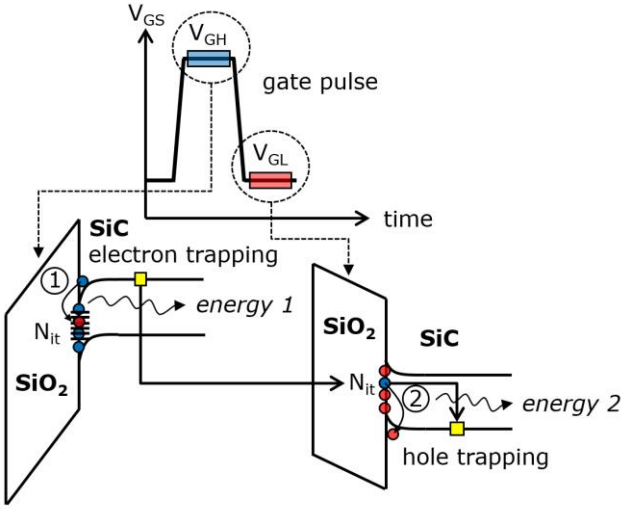

Fig. 4: An empiric model for GSI. (1) When switching fast from accumulation to deep inversion, previously captured holes (red) may temporary enhance the electric field (not shown). Shortly after, inversion electrons (blue) may recombine with captured holes, thereby releasing the first energy portion via radiation (e.g. emission of photons) and/or vibrational excitations (e.g. emission of phonons). (2) During turn-off, similar hole trapping processes take place. To sum, each full recombination event releases an energy equal to the SiC bandgap (3.3 eV) in every switching cycle. In SiC there may be 10^{11} cm^{-2} to 10^{12} cm^{-2} recombination events per switching cycle

While similar observations in silicon devices have been assigned to gate-sided hydrogen release [13], any model for GSI in SiC devices needs to consistently explain the main experimental observations reported by several independent groups [4-7]. These observations are:

- GSI is much less pronounced or even non-existent in Si MOSFETs
- GSI induced drifts are proportional to the number of switching events
- GSI kicks in only while pulsing the gate between deep accumulation ($V_{GL} < V_{FB}$) and deep inversion ($V_{GH} > V_{TH}$)
- GSI is stronger for steeper gate switching transients
- GSI does not (or only weakly) depend on the gate pulsing duty cycle

Our suggested model for GSI, shown in Fig. 4, is based on the charges trapped temporarily at the SiC/SiO_2 interface and on the release of excess energy due to trap-assisted recombination events at the SiC/SiO_2 interface that occur in every single switching cycle. After a fast switching of the gate bias between accumulation and inversion, previously trapped charge carriers in the defect states at the SiC/SiO_2 interface may locally enhance the electric field for a short duration before recombining with charge carriers from the valence, or the conduction band, respectively. We consider the local

enhancement of the electric field due to temporally trapped charge carriers as a minor or second order effect because our experiments show that voltage acceleration of GSI is relatively weak after exceeding deep accumulation during the low phase and deep inversion during the high phase of the gate pulse. We hypothesize that the major effect is due to the recombination at the interface. Each defect-assisted recombination process releases, in two steps, an energy equal to the SiC bandgap (3.3 eV) mostly through vibrational excitations and partly through radiation. The released thermal energy can act as a "phonon kick" to bring a defect to an excited vibrational state from which it can experience a reaction into a charged state. This process is well known as the recombination enhanced defect reaction [14-17]. It consistently explains the observed properties of GSI as mentioned above.

- Due to the higher number of recombination states at the SiC/SiO_2 interface and the larger bandgap of SiC, the number of recombination events and the energy released in every single recombination event is much less for Si MOSFETs compared to SiC MOSFETs
- The total recombination energy pumped into the system is naturally proportional to the number of switching events within a certain time, respective to the frequency
- Periodic trap-assisted recombination can only occur if there are holes present at the low level ($V_{GL} < V_{FB}$) and electrons present at the high level ($V_{GH} > V_{TH}$) of the gate voltage
- The faster the gate switches between accumulation and inversion, the wider is the active energy window of interface traps that may act as recombination centers [18]
- Electron and hole trapping into interface states is extremely fast, therefore, only very short time durations at V_{GH} and V_{GL} gate voltage levels are needed to recharge the interface

A more thorough discussion on the dependence of trap-assisted recombination on gate switching parameters such as biasing levels, frequency, rise/fall times, and temperature can be found in literature that focuses on charge pumping [18]. Charge pumping is an electrical measurement method for the characterization of interface states in MOSFETs. Many aspects of GSI that are consistent with trap-assisted recombination can be understood within the theoretical framework of charge pumping.

Spectroscopy of Interface Radiation to Reveal the Nature of Recombination Defects

While vibrational energy, after being generated due to interface recombination, dissipates rapidly and may thereby trigger degradation during GSS, the majority of generated photons can easily traverse the SiC crystal because their energy is below the bandgap of SiC. During GSS, these photons can be captured in-situ on the reverse side of a fully processed chip after etching parts of its backside metallization [8]. As the field effect confines the recombination strictly to the SiC/SiO_2 interface of the MOSFET, it is evident that the photons originate exclusively from that region. Their spectrum can be investigated using an optical spectrometer.

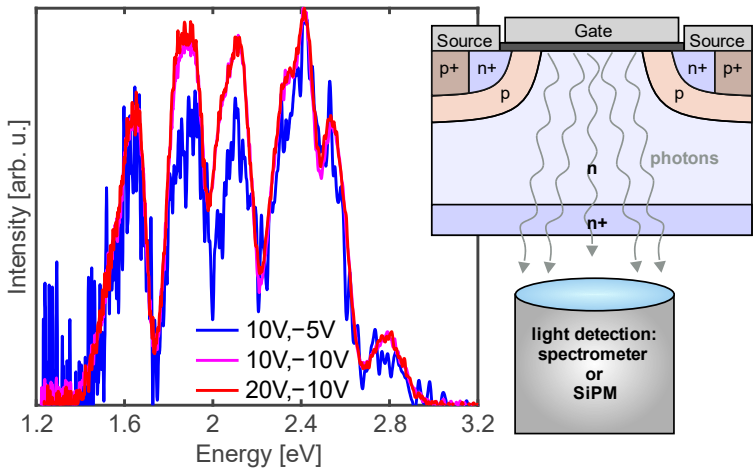

Fig. 5: The emission spectrum of photons created by defect-assisted recombination of charge carriers during GSS. Prior to their detection, the photons traversed the SiC crystal

The schematic experimental setup and an exemplary energy spectrum measured on a SiC DMOSFET device using different gate bias levels and a pulsing frequency of 1 MHz is shown in Fig. 5. This spectrum can be understood as a fingerprint of the radiative electronic interface transitions with distinct peak energies. The target of future research will be to further refine this optical methodology and to correlate the characteristic peaks in the spectrum to defect types suggested by theoretical calculations [9,10]. Also, correlating defect-specific emission peaks to findings of alternative methods that provide structural defect information such as electrically detected magnetic resonance [19,20] could lead to a deeper understanding of the nature of the involved defects.

Summary

We have developed a test procedure to assess worst-case parameter variations of SiC power MOSFETs in a switching operation. The results can be documented in application notes enabling customers to easily consider GSI in the safety margins of their system designs. A model for GSI-based on recombination enhanced defect reactions at the interface has also been suggested. The model is consistent with the main features of GSI reported in literature. Recent research has revealed that some recombination events at the interface also create photons. Their spectrum can be measured on a fully processed device. A comparison of characteristic peaks with theoretical predictions might help reveal the nature of the involved point defects.

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