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# Effect of Termination Region on Unclamped Inductive Switching Failure for 4H-SiC VDMOS

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**Keywords:** 4H-SiC, MOSFET, UIS, avalanche, breakdown.

**Abstract.** The effect of the termination structure on the unclamped inductive switching (UIS) failure is analyzed for two kinds of SiC MOSFET, where S-MOS and G-MOS termination structure are adopted. The MOSFETs are named as S-MOS and G-MOS according to the buses connecting with different electrodes in the termination region. The experimental results indicate that the avalanche energy G-MOS can withstand is 1.15 times larger than that of S-MOS. To understand what are the factors that lead to different UIS capabilities, further static measurements and hotpot mapping after UIS test are done, and technology computer aided design (TCAD) simulation also is done to further confirm the principle.

## Introduction

Silicon carbide (SiC) is an attractive candidate material for the next generation power electronics. The major upsides of SiC superior to those of silicon are generally considered as higher critical breakdown electric field, lower leakage current, and higher thermal conductivity [1, 2]. SiC MOSFETs, as the fastest advanced SiC device technology over these years, begin to substitute the silicon counterparts in some commercial applications [3]. However, the robustness and reliability of the SiC MOSFETs are issues before the complete replacement [4]. The unclamped inductive switching is one of the important robustness for SiC MOSFET [5].

An UIS event could happen when the MOSFET is employed in the power electronic systems containing inductive loads [6]. This operation is ordinarily encountered in automotive applications, like fuel injector coil circuits, anti-lock braking modules, etc. In the UIS test, the MOSFET is connected to an inductance without anti-parallel free-wheeling diode to commutate the loop current when switching off the device. The MOSFET has to bear the high avalanche current (Iav) and the drain-source avalanche breakdown voltage ($V_{(br)DSS}$) simultaneously during the avalanche process [7].

The failure mechanism of UIS is normally considered as the channel activation [8], parasitic bipolar junction transistor (BJT) turn-on [9] and melting of metal electrodes [10] caused by the junction temperature rise in a short time. The researches generally only focus on the failure in active region of MOSFETs. While, the termination region is also a significant part need to be considered in UIS failure for MOSFET. Soneda et al. [11] reported that the equivalence of the drain-source breakdown voltage for the active region and termination region can drive the avalanche failure point into the active region, and the optimal design for the $V_{(br)DSS}$ of the termination structure benefit avalanche energy improvement. However, the effect of the termination structure on the reliability is still not clear.

In this article, The experimental UIS test was carried out for SiC MSOFETs with two different kinds of termination structure. The failure point locations of devices are clarified by static

characteristic test results. The UIS behavior for SiC MOSFETs is analyzed by TCAD electro-thermal simulation. The simulation results demonstrate that the conduction current and the electric field distribution affected by the termination structure significantly determine the UIS capability of devices.

## Devices Structures and Experimental Method

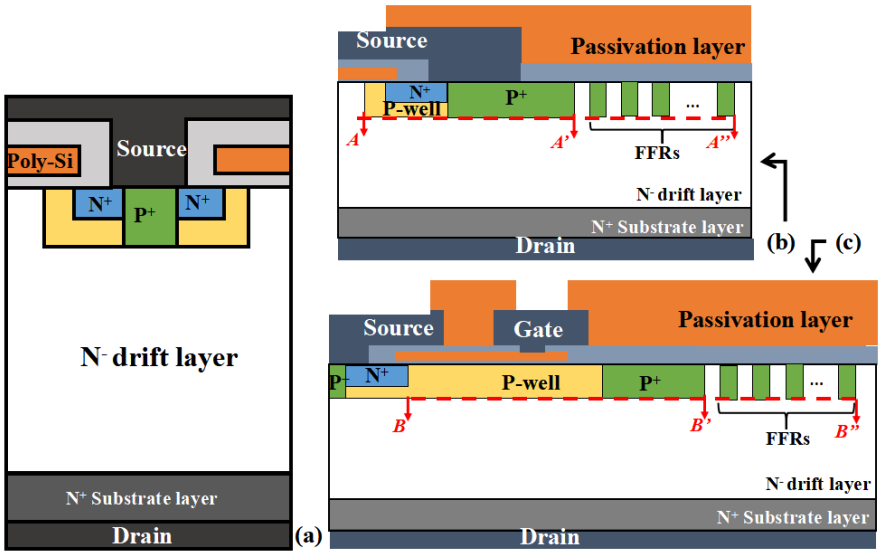


Fig. 1 Schematic cross-sections of (a) the active, termination regions of (b) S-MOS and (c) G-MOS for SiC MOSFETs.

SiC MOSFETs with two types of termination structures have been fabricated, as shown in Fig. 1 (a)-(b), respectively. The source bus is located in the termination structure for S-MOS. The other one has an extra gate bus and a long P- base doping region in the termination region, which is called as G-MOS. The MOSFETs were fabricated on a 4-inch 4H-SiC wafer with 13 μm n-type epitaxial layer and its doping concentration of $6\times10^{15}$ $cm^{-3}$. The die size is 0.024 $cm^2$, including 0.022 $cm^2$ for the active region and 0.002 $cm^2$ for the termination region.

The UIS measurements were carried out on ITC55X00C testers. To achieve an avalanche current of 1 A, the gate pulse duration is set to 61 μs with the load inductance of 3 mH and bus voltage of 50 V. This circuit is adopted in the mix-mode TCAD simulation, where the active region and termination region are connected in parallel. The purpose of this split design is to analyze the drain-source current of the two-part structure separately.

## Results and Discussion

In test, the avalanche current and bus voltage were fixed at 1 A and 50 V, respectively. The avalanche energy gradually rises by increasing the inductance until the critical avalanche breakdown was reached. The UIS experiments with 15 samples (6 of S-MOS and 9 of G-MOS) were carried out. The statistical experimental results are shown in Table. 1. The minimum, average and maximum of critical avalanche energy of G-MOS is 3 mJ, 4.035 mJ and 7.5 mJ, respectively. In contrast, the results of S-MOS are 2.5 mJ, 3.52 mJ and 5.5 mJ, respectively. These results indicate that the avalanche energy which G-MOS can withstand is 1.15 times than that of S-MOS.

Table I. The static results of the UIS test for S-MOS and G-MOS.

| | Sample Number | Avalanche Energy (mJ) | | |
|---|---|---|---|---|
| | | minimum | average | maximum |
| S-MOS | 6 | 2.5 | 3.52 | 5.5 |
| G-MOS | 9 | 3 | 4.035 | 7.5 |

As shown in Fig. 2, the typical UIS waveform and the failure waveform of two devices are different. Fig. 2 (a) indicates that the avalanche period lasts about 6 μs, after that, the current and voltage become zero. In contrast, when UIS failure happens for S-MOS, the drain-source voltage only reaches 500 V and oscillates to zero as the current reduces, which indicates that the device loses the voltage blocking capability. However, the drain-source voltage can reach 1400 V and directly decrease to zero later for G-MOS, while the avalanche current still keeps about 0.7 A. It indicates that there may be some problems with the gate control capability for G-MOS.

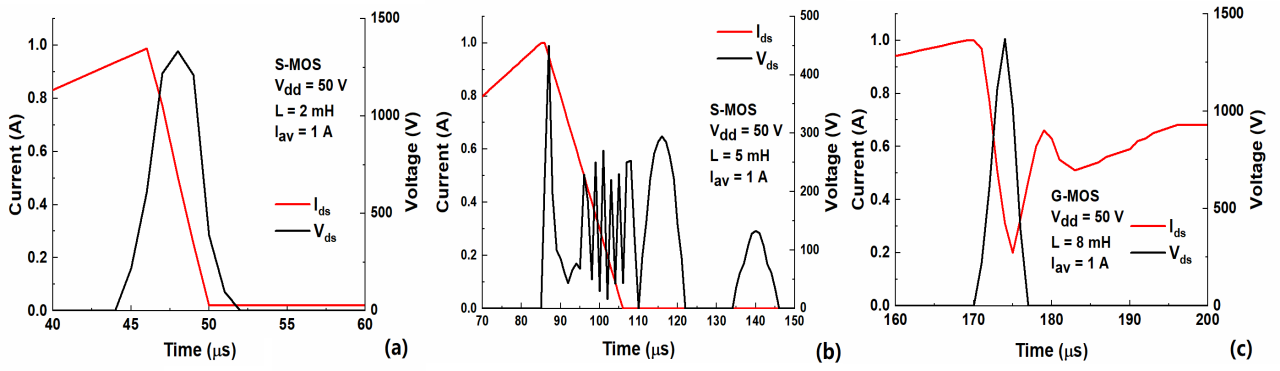


Fig. 2 Typical UIS failure waveform of (a) S-MOS and (b) G-MOS.

The static characteristics after UIS test is shown in Fig. 3. Different circumstances about transfer and breakdown characteristics happen after the UIS test. For the S-MOS, the transfer characteristic is still normal but the withstand capability of the blocking voltage loses at 100 μA. It indicates that the blocking capability loss but gate is not effected for S-MOS. The 3rd-quadrant behavior of S-MOS is shown in Fig. 3(c), in which the knee voltage is -3 V and -2 V at $V_{gs}$ = -5 V and 0 V, respectively. It means that the channel region is fine after the UIS test [12]. For G-MOS, the blocking voltage withstand capability is well but the gate leakage current is large in transfer curves. The 3$^{rd}$-quadrant characteristic of G-MOS is almost reclosing at $V_{gs}$ = 0 V, -5 V, which indicates that the gate loses the control capability. The blocking voltage withstand capability of the MOSFET is formed with the P-base/N-drift junction in the active region and the termination region, and the body diode structures exist only in the active region, which means that the possibility for the damage occurred in the active region is ruled out [13]. That is, the broken point happens in the termination region for S-MOS.

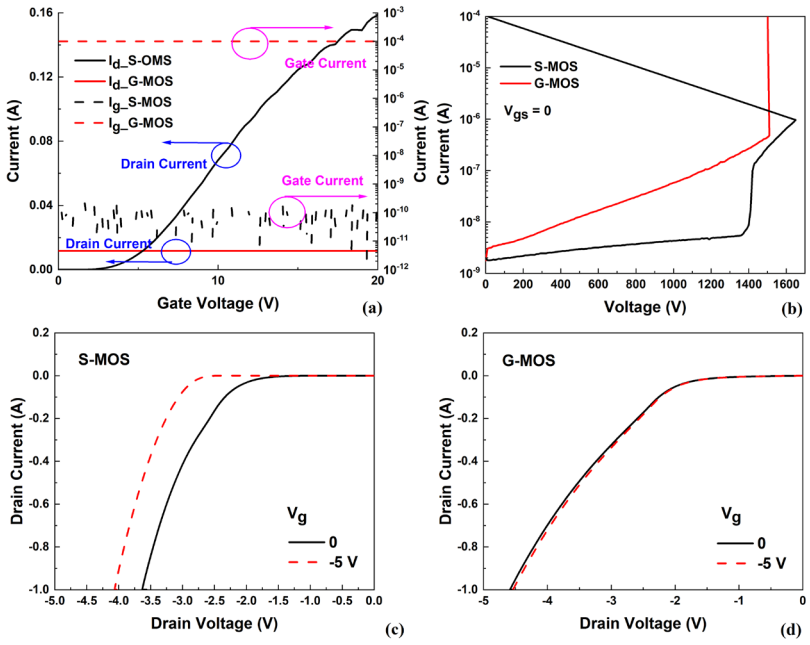


Fig. 3 Static characteristics for two kinds of MOSFET after UIS test.

The areas of active and the termination regions for TCAD simulation are defined as the same as the devices in reality. The drain current and voltage curves during UIS process are shown in Fig. 4. The avalanche process begins at 63 μs. $V_{(br)DSS}$ of both structures reach 2500 V, which are larger than the experimental results due to the ideal material set for simulation. The total drain current $I_d$ reaches 1 A, which includes the current through the active region ($I_{d\_ac}$) and termination region ($I_{d\_term}$). It is worth mentioning that the $I_{d\_term}$ of G-MOS is almost negligible, compared to the high $I_{d\_term}$ of S-MOS during the UIS process.

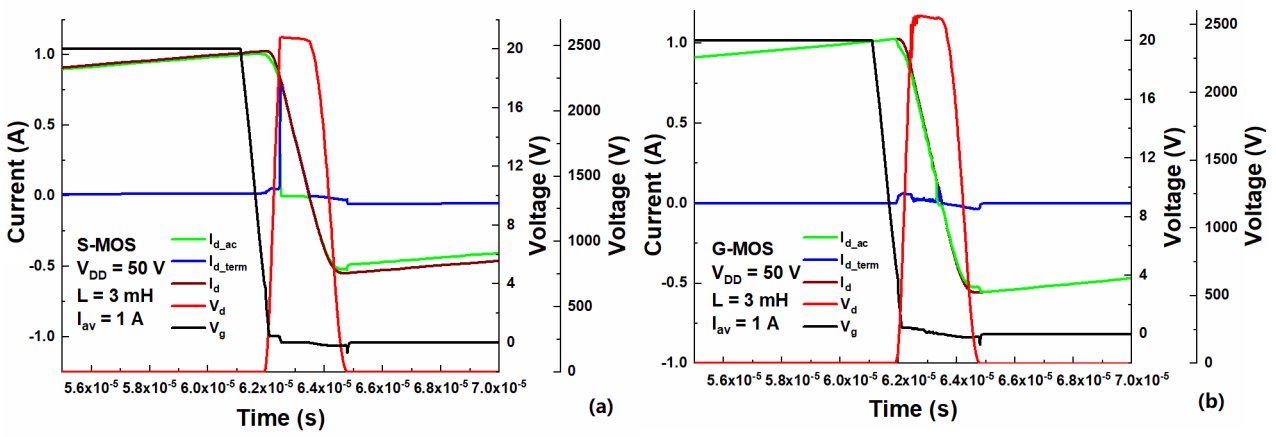


Fig. 4 UIS simulation results of (a) S-MOS; (b) G-MOS.

To better understand the avalanche processes of MOSFETs, the conduction current density distributions at 63μs are analyzed. The conduction current distributions are shown in Fig. 4. An obvious conduction current path exists in the termination region for S-MOS, which is up to $1.1\times10^{3}$ A•cm$^{-2}$. In contrast, the currents flowing through the active region and the termination region are extremely close for G-MOS, ranging from $3\times10^{-6}$ A•cm$^{-2}$ to $2.5\times10^{-4}$ A•cm$^{-2}$.

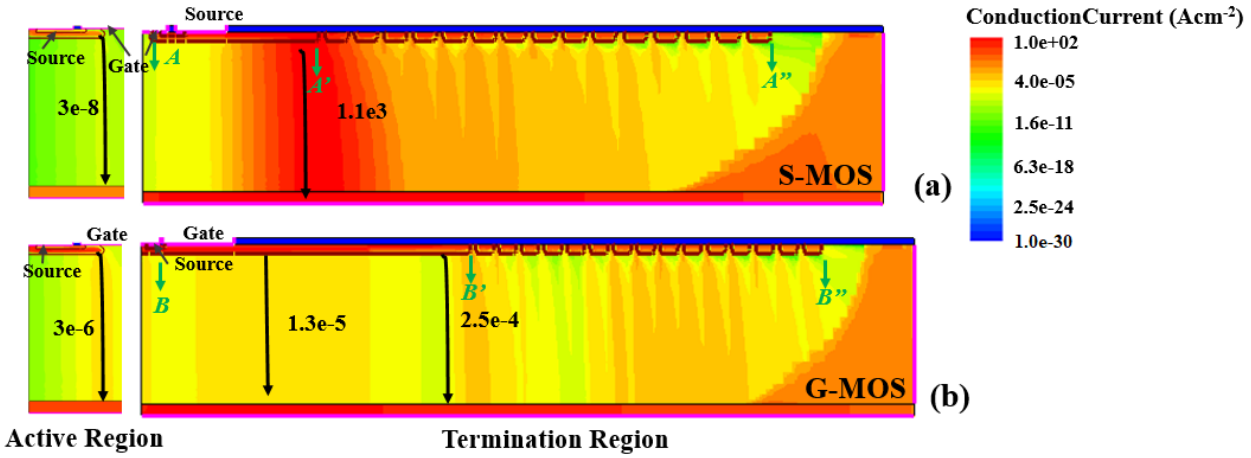


Fig. 5 Conduction current distribution for (a) S-MOS and (b) G-MOS on UIS condition.

The conduction current is extremely high at the main junction for S-MOS. The thermal failure is easy to happen in such a small area. In contrast, for G-MOS, the uniform electric field leads to a smooth current distribution. An additional electron drift current leakage path in the termination region makes the current distribution more uniform and avoids the heat concentration. To understand why the additional current path exists in G-MOS, the electric potential and band distribution for two devices are shown in Fig. 6. As Fig. 6(a) and (b) shown, impact ionization causes current generation at A' and B'. $I_{S\_3}$ flows to source pad directly for S-MOS. But $I_{G\_3}$ flows through N+/P-well/N-drift region, which cause the barrier lowing (shown in Fig. 6 (d)), the barrier low to 1.04 eV is much easier for electrons to transfer, which causes a high leakage current path.

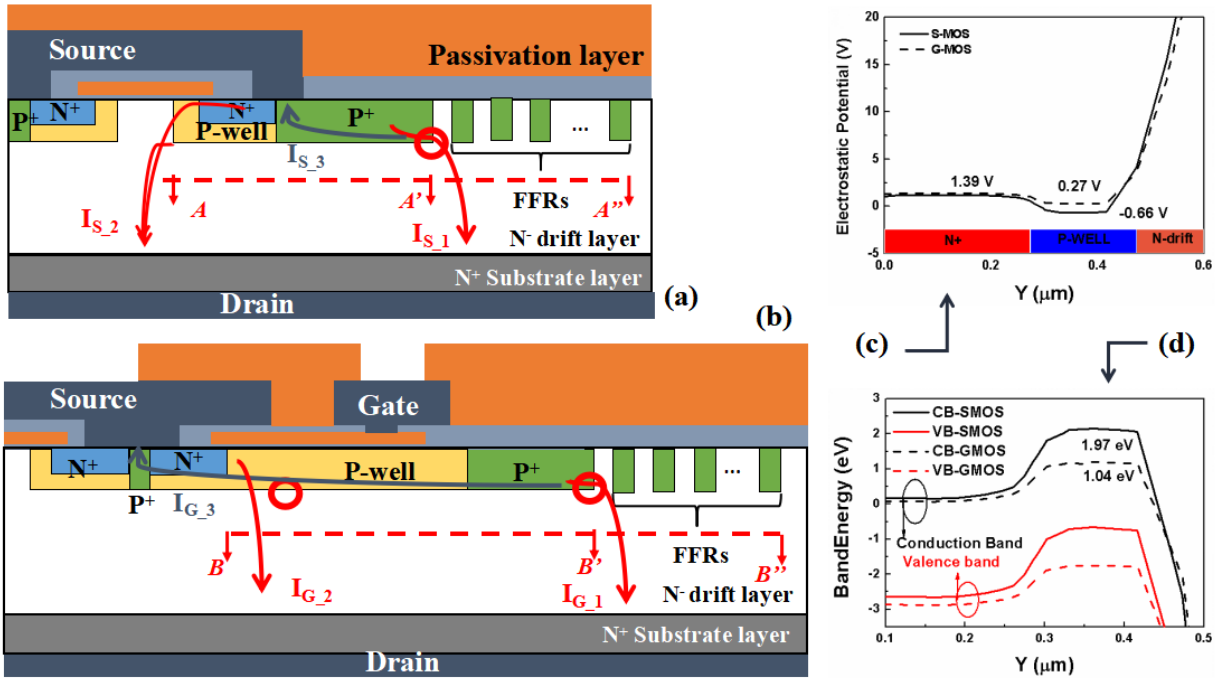


Fig. 6 Current distribution for (a)S-MOS and (b)G-MOS on UIS condition. (c)Potential and (d) energy band distributions on the Y direction at points A and B, respectively.


## Summary

The effect of the termination regions on the UIS condition for SiC MOSFETs is investigated by experimental and TCAD simulation tests. The statistical experimental results indicate that the G-MOS can withstand 1.15 times the avalanche energy of S-MOS at average. Static characteristics are measured for the devices after UIS test, which clarify that the failure points happen in the active region for G-MOS and termination region for S-MOS, respectively. The TCAD simulation and analysis for two device structures are also done. It is found that only one current path exists in the termination for S-MOS, while an extra current leakage path exists due to the barrier lowering in the termination for G-MOS. The extra current leakage path in the termination of G-MOS avoids the current concentrates in the termination region at the beginning of the UIS process. On the UIS condition, the maximum current density is $1.1\times10^{3}$ A•cm$^{-2}$ and $3\times10^{-8}$ A•cm$^{-2}$ in the termination region and the active region for S-MOS, respectively. While the current is $2.5\times10^{-4}$ A•cm$^{-2}$ to $3\times10^{-6}$ A•cm$^{-2}$ throughout those for G-MOS. That is, the G-MOS can maintain performance during the avalanche process, and the S-MOS is damaged by the avalanche breakdown in the termination region under the same condition. This work indicates that it is a convenient but not accurate method to judge the location of avalanche failure in the active and termination region by BV, and the essence of that method is the balance of current leakage capability of the two regions in the power devices.


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