*Key Engineering Materials*
*ISSN: 1662-9795, Vol. 948, pp 101-105*
*doi:10.4028/p-968y4h*

*Submitted: 2022-08-28*
*Revised: 2022-12-06*
*Accepted: 2022-12-06*
*Online: 2023-06-06*

# Investigations on 4H-SiC Low Voltage nMOSFETs with Thin Thermal $SiO_2$/Deposited Oxide Gate Dielectric

Kevin Kyuheon Cho, Brian Lee, Ki-Min Kim, Doojin Choi and K.S. Park

Onsemi, 55, Pyeongcheon-ro 850, Bucheon-si, Gyeonggi-do, Korea

[a]kevin.cho@onsemi.com, [b]brian.lee22@onsemi.com, [c]kimin.kim@onsemi.com, [d]doojin.choi@onsemi.com, [e]ks.park@onsemi.com

**Keywords:** 4H-SiC, low voltage nMOSFETs, channel mobility, interface state density, carbon cluster, charge pumping, deposited gate oxide, TLP

**Abstract.** The poor quality of $SiC/SiO_2$ interface significantly limits the channel mobility, especially in 4H-SiC MOSFETs. Several strategies have been addressed to overcome this issue. Nitridation by NO has been adopted widely by manufactures because nitrogen may replace carbon in some chemical bond at the $SiC/SiO_2$ interface. However, excessive nitridation is not desirable because of pronounced hole-trapping effects near the conduction band. As an alternative gate dielectric, thin $SiO_2$/deposited oxide stack has been investigated in 4H-SiC lateral nMOSFETs. Overall performances were reviewed in aspects of transfer/$g_m$/reverse characteristics, charge pumping method and TLP characteristics.

## Introduction

Silicon Carbide has become an important electronic material due to the potential of SiC power devices to provide efficient energy distribution and management for applications such as smart grid and electric vehicles. Despite continuing advances in fabrication and design, the channel mobility limits the performance which is caused mainly by structural imperfections of dielectric layer as well as in the interface. Interstitial carbon clusters, Si and C vacancies in the SiC surface and most probably a high strain of interface atomic layers are responsible for the creation of electrically active traps [1-2]. The alternative dielectric to improve the channel performance using 50Å thermal $SiO_2$/350Å deposited oxide has been analyzed through 4 terminals LV nMOSFETs and compared to nMOSFETs with 400Å thermal $SiO_2$. The reliability concerns of each dielectric have been evaluated by ESD performance using TLP characteristics for future vehicles in real applications.

## Results and Discussion

Fig. 1(a) shows the cross-section of 4 terminals 40V nMOSFETs fabricated on 4H-SiC epilayers on n-type substrate. The gate last process is used wherein gate dielectrics are formed by annealing SiC and followed by post oxidation annealing. Transfer characteristics, $g_m$ and reverse characteristics depending on channel lengths are shown in Fig. 1(b) and 1(c) according to different dielectrics. $V_{TH}$ roll-off starts to be shown from $L_{CH}$=3.0um in common, so we decided to proceed subsequent analysis focusing on $L_{CH}$=4.0um / W=300um nMOSFETs to get rid of mis-alignment or short channel effects.

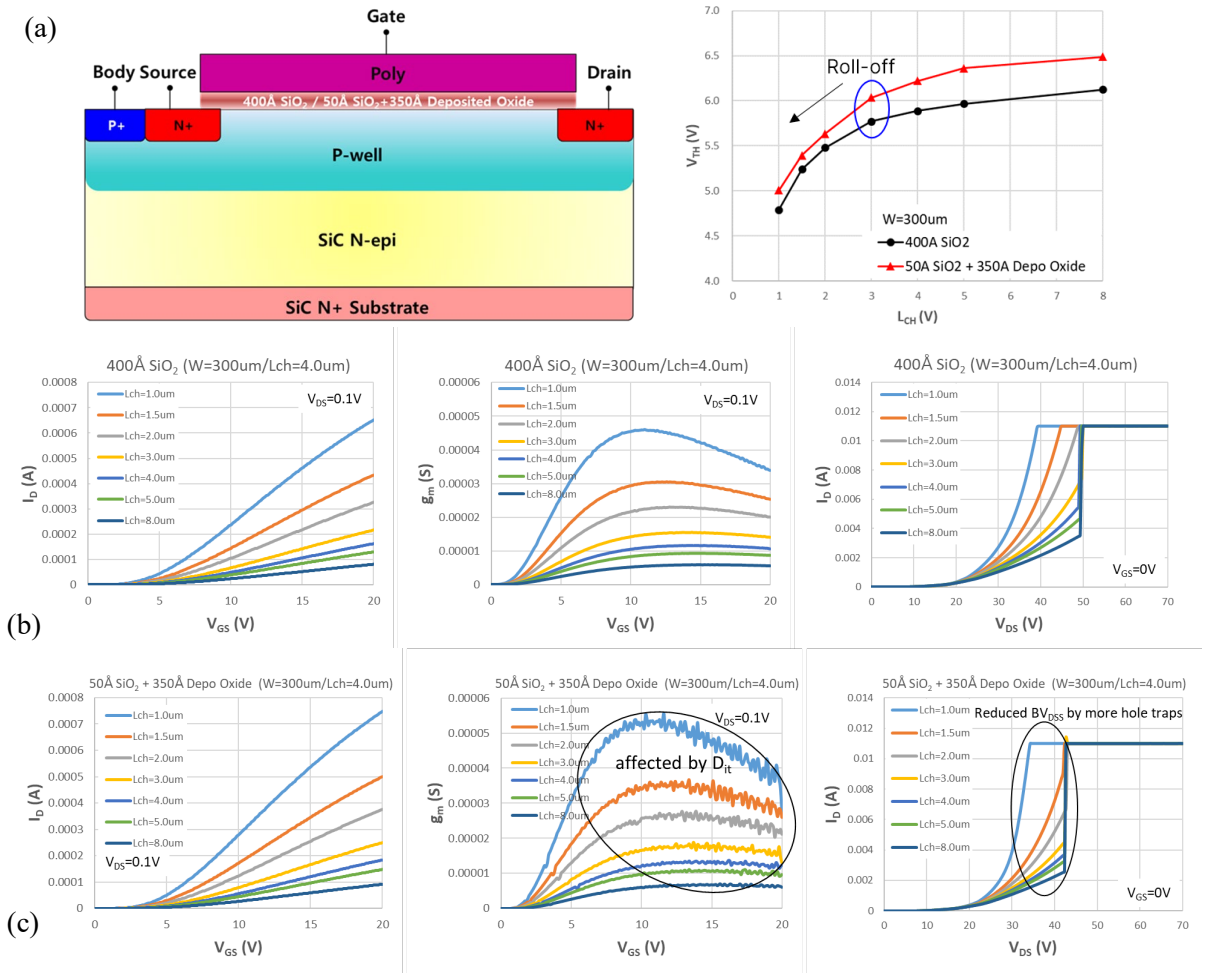


Fig. 1. (a) Cross-section of LV nMOSFETs, Transfer/$g_m$/Reverse characteristics of (b) 400Å thermal $SiO_2$ and (c) 50Å themal $SiO_2$/350Å deposited oxide gate dielectric

Fig. 2(a) shows the calculated $\mu_{FE}$ from $I_D$-$V_{GS}$ using the capacitance measured from MOS capacitors. $\mu_{FE}$ from 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric is increased by 10.6% compared to 400Å thermal $SiO_2$ at the high field (=4.5MV/cm) and this result would be caused by less carbon clusters and Si vacancies which are generated during short-time oxidation. $I_{D,Lin}$ and $I_{D,Sat}$ curves are measured respectively to confirm Drain-Induced Barrier Lowering (DIBL) depending on each gate dielectric and very stable DIBL effects are observed without any subthreshold leakage as shown in Fig. 2(b) and 2(c).

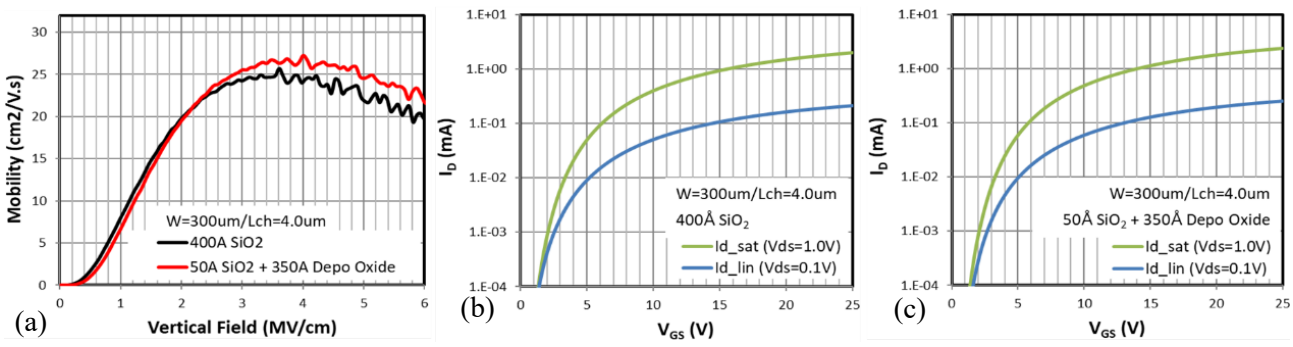


Fig. 2. (a) $\mu_{FE}$ comparison, Linear & Saturated $I_D$-$V_{GS}$ curves from (b) 400Å thermal $SiO_2$ and (c) 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric

Interface state densities at each gate dielectric were characterized using charge pumping measurements as shown in Fig. 3. 10V pulse amplitude has been employed for the base voltage sweep. Average $D_{it}$ can be extracted as a function of band-bending on the following equation; Avg. $D_{it}=I_{cp}/(qAf)$ where $I_{cp}$ is the charge pumping current, q is the electron charge, A is the channel area and f is the frequency. Approximately 50% higher $D_{it}$ level is shown in the 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric than 400Å thermal $SiO_2$ based on the result from charge pumping. $g_m$ in Fig. 1(c) also shows severe noises compared to Fig. 1(b) proving more $D_{it}$. Once you take a look at Fig. 3(b), the 2nd peak is introduced in charge pumping plot. Amount of captured holes by hot hole injection are recombined with channel electrons and lead to additional substrate current making the 2nd peak. The reason why higher $D_{it}$ level is observed in 50Å thermal $SiO_2$/350Å deposited oxide might be related to the insufficient oxidation time, so it would result in poor interface states than those of 400Å thermal $SiO_2$. Nevertheless, $\mu_{FE}$ from 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric shows better than 400Å thermal $SiO_2$ gate dielectric. When it comes to the channel mobility at least, surface roughness scattering that comes from carbon clusters generated during oxidation plays an important role than $D_{it}$ does, especially under high fields [3].

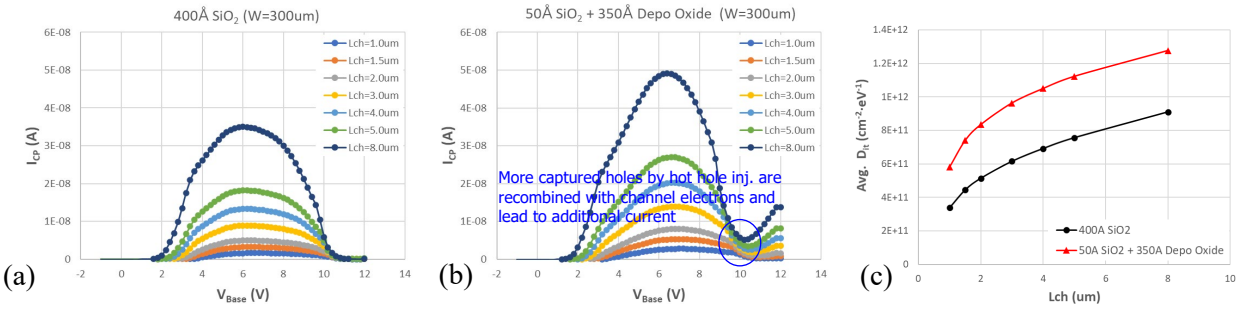


Fig. 3. Charge pumping measurement from (a) 400Å thermal $SiO_2$ and (b) 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric, (c) Comparison of average $D_{it}$ extracted from charge pumping measurement

Although SiC has been demonstrated with many superior properties like temperature tolerance, radiation hardness and thermal conductivity, the assessment of reliability regarding ESD performance could have a significant effect on the consideration of different gate dielectrics in nMOSFETs [5]. LV nMOSFETs operate properly showing on-state BV in Fig. 3(a) and 3(b) matches well with off-state BV in Fig. 1(b) and 1(c) respectively. However, 10V earlier dielectric damage on different $V_{GS}$ conditions tends to be shown at 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric. Therefore, the stacked gate dielectric needs to be revised by adopting more robust 50Å thermal $SiO_2$ process which interfaces with SiC surface to improve the gate oxide integrity. There are no concerns on parasitic bipolar triggering or unwanted latch-up when considering dielectric breakdown voltage and rated currents of nMOSFETs after evaluating the effect of gate biasing on TLP characteristics.

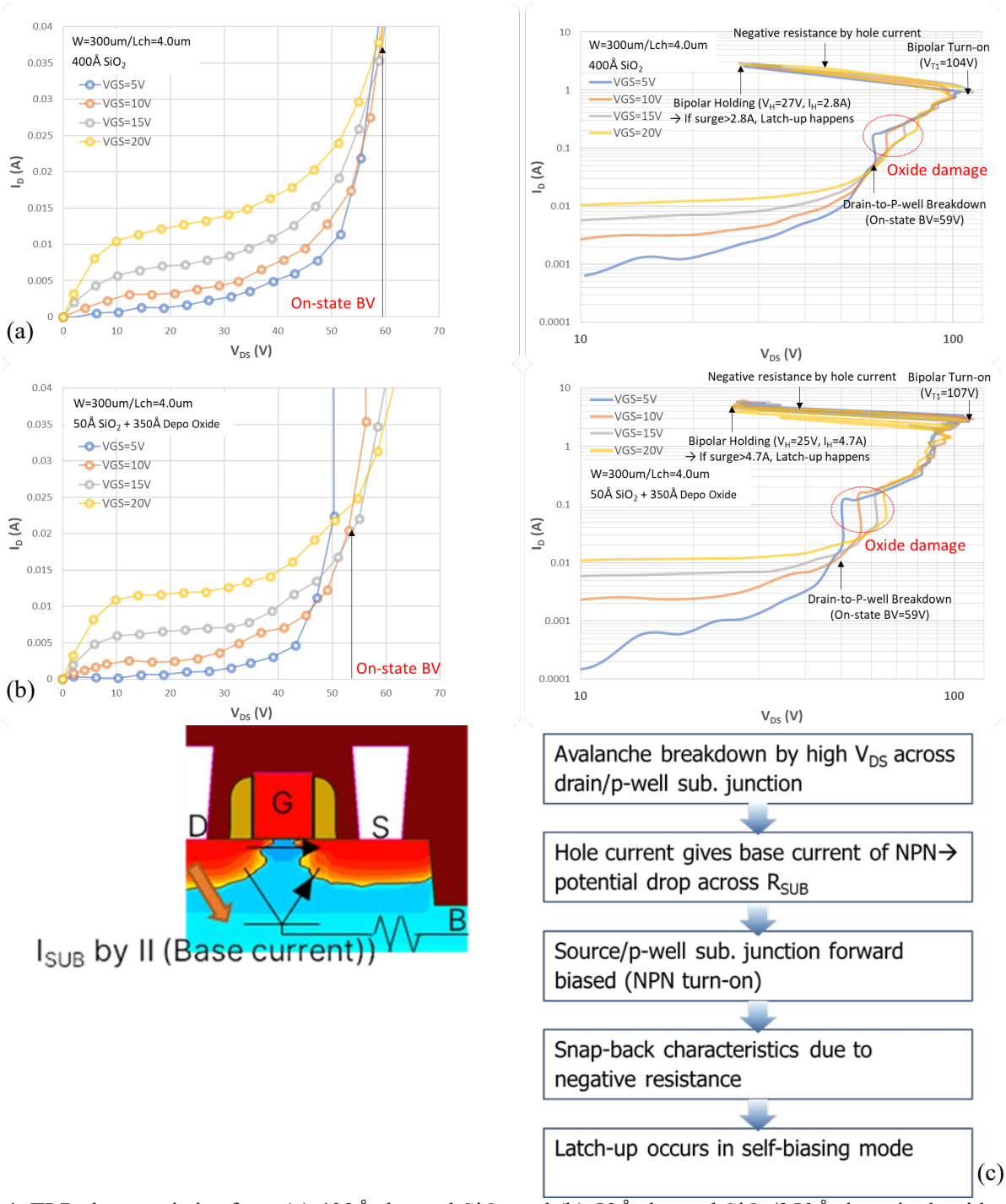


Fig. 4. TLP characteristics from (a) 400Å thermal $SiO_2$ and (b) 50Å thermal $SiO_2$/350Å deposited oxide gate dielectric, (c) LV nMOSFETs triggering mechanism

## Summary

The best way to reduce the channel resistance is to enhance the inversion carrier mobility by improving SiC/$SiO_2$ interface quality. Currently, the channel mobility limits the performance mainly caused by structural imperfections of dielectric layer such as carbon interstitials, oxygen vacancies and carbon clusters at the SiC surface. Nitridation by NO gives a better result than that by $N_2O$ because $N_2O$ molecules are more stable at high temperature. Number of interface traps can be qualitatively scaled down with the amount of interfacial nitrogens [4] however, excessive nitridation is not desirable because of pronounced hole-trapping effects near the conduction band. The balance between oxidation and passivation is a critical point to get SiC surface passivated nicely. The gate last process wherein gate dielectrics are formed by annealing SiC is accompanied by oxidation of SiC

surface inevitably and it leads to the degradation of interface properties through the introduction of carbon defects. The alternative gate dielectric by combining 50Å $SiO_2$/350Å deposited oxide for minimizing oxidation of SiC has been analyzed and compared to 400Å $SiO_2$ gate oxide in 4H-SiC LV nMOSFETs. 50% higher $D_{it}$ level is observed in the stacked gate dielectric compared to 400Å $SiO_2$ by using the charge pumping method, however $\mu_{FE}$ of the stacked gate dielectric is increased by 10.6% compared to that of 400Å $SiO_2$ at the high field (=4.5MV/cm) due to less carbon clusters generated during short time oxidation. This means $\mu_{SR}$ affected by carbon clusters plays an important role than $\mu_C$ under the high electric field. Based on TLP characteristics, there are no concerns on parasitic bipolar triggering or latch-up considering dielectric BV and rated current of 4H-SiC LV nMOSFETs with the stacked gate dielectric.

## References

[1] M. Cabello, V. Soler, G. Rius, J. Montserrat, J. Rebollo, and P. Godignon, Materials Science in Semiconductor Processing 78 (2018) 22-31.

[2] S. Wang, S. Dhar, S Wnag, A. Ahyi, A. Franceschetti, J. Williams, L. Feldman, and S. Pantelides, Phys. Rev, Lett. vol. 98, iss. 2-12, Jan. 2007.

[3] A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán, Microelectron. Eng.83 (2006) 440-445.

[4] J. Rozen, A. Ahyi, X. Zhu, J. Williams, and L. Feldman, IEEE Transactions on Electron Devices, vol. 58, no. 11, pp. 3808-3811, Nov. 2011.

[5] D. Thomas, S. Ahmed, T. Vrotsos, Z. Chen, and A. Mantooth, 2016 IEEE 4th WiPDA 236-241.