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Reduction of Forward Bias Degradation in 4H-SiC PiN Diodes Fabricated on 4H-SiC Bonded Substrates

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Abstract. The advantage in reducing forward bias degradation of bipolar 4H-SiC devices using a 4H-SiC bonded substrate is demonstrated. To evaluate the differences in forward bias degradation between a 4H-SiC bonded substrate and a commercially available 4H-SiC bulk substrate, a forward current stress test and subsequent photoluminescence (PL) imaging of PiN diodes fabricated on both the substrates were performed. Unlike the bulk substrate, the bonded substrate maintained a low ΔVf and the variation among the measured diodes was extremely small even after applying the highest current density of 1500 A/cm^2. The investigated number of bar-shaped SSFs within the electrically stressed diodes with more than 1000 A/cm^2 revealed the possibility that the BPDs existing at deep positions below the epilayer/substrate interface were drastically reduced in the 4H-SiC bonded substrate.

Introduction

4H-silicon carbide (4H-SiC) is a promising wide gap material for high power electrical devices owing to its high breakdown electric field and high thermal conductivity. Although such excellent material properties, its full-scale spreading to high power applications is limited. One of the key issues with 4H-SiC is difficulty in crystal growth. A several-hundred-micron-thick 4H-SiC monocrystalline boule must obtain single piece of 4H-SiC bulk substrate. However, in sublimation growth process, which is typically employed in 4H-SiC crystal growth, its growth rate is limited, that is, it is <500 μm/h to avoid the generation of undesirable crystal defects.

Recently, a novel 4H-SiC substrate using wafer bonding techniques (4H-SiC bonded substrate) has become commercially available. The 4H-SiC bonded substrate manufactured by SICOXS comprises an extremely thin (on the order of submicrons) monocrystalline 4H-SiC layer bonded on an n-type low resistivity polycrystalline 3C-SiC substrate by the surface activated bonding method. The 4H-SiC bonded substrate enables the reduction in the volume of 4H-SiC monocrystalline portion having low defect density for application in electrical devices. Furthermore, its unique hybrid structure is expected to bring some benefits that are not possible with a conventional 4H-SiC bulk substrate, such as reduction of on-state resistance in PiN diodes [1] and backside ohmic contact formation requiring no additional thermal annealing process [2].

In this study, we focus on forward bias degradation, which is widely observed in 4H-SiC bipolar devices. In this phenomenon, the on-state voltage increases with forward current stress, which is due to the growth of Shockley-type stacking faults (SSFs) starting from basal plane dislocations (BPDs) induced by electron-hole pair recombination [3]. To evaluate the differences in the forward bias degradation between novel 4H-SiC bonded substrates and conventional 4H-SiC bulk substrates, electrical and optical observations of PiN diodes fabricated on both the substrates were performed.

Experimental

Fig. 1 shows a cross-sectional schematic illustration of the PiN structure employed here. The heavily nitrogen (N)-doped buffer layer and lightly N-doped drift layer were formed homoepitaxially on both 4H-SiC bulk and bonded substrate. The dopant concentration and thickness of the buffer and drift layer are 4×10^{17} /cm^3, 1×10^{16} /cm^3 and 0.1 µm, 10 µm, respectively.
A p+ anode region with a dopant concentration of 3×10^{20} /cm^3 was fabricated using aluminum (Al) implantation at 500 °C followed by the activation annealing at 1620 °C. Finally, anodes and cathodes were formed on both sides of the substrate to obtain the PiN diodes. An active area of which is 0.038 cm^2.

A forward current stress test was performed on these PiN diodes. The forward current stress is applied in four steps (the forward current density of 100, 500, 1000 and 1500 A/cm^2) at 175 °C. The forward current–voltage (I–V) characteristics are measured at an initial step and each step after applying the forward current stress. The amount of forward bias degradation is quantitatively defined as the forward voltage shift (ΔVf) at a forward current of 60 A between the initial and electrically stressed diode (Fig. 2).
To investigate the evolution of SSFs within the electrically stressed diodes, photoluminescence (PL) imaging with a 420-nm band-pass filter was performed after removal of the electrodes of the diodes.

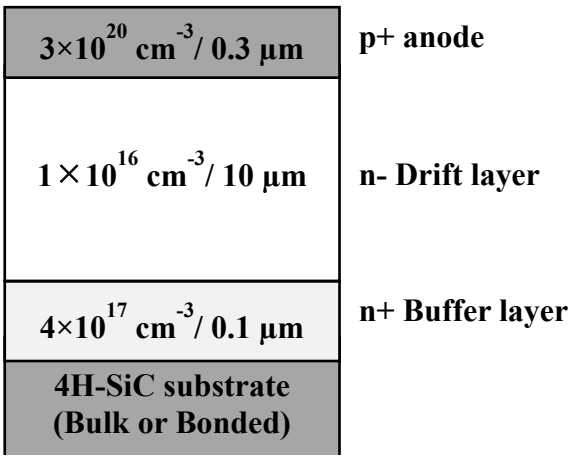

Fig. 1: Schematic image of PiN structure in this study

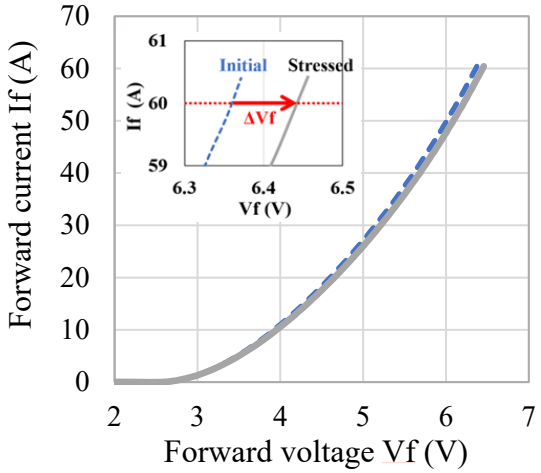

Fig. 2: Forward I–V characteristics of initial and stressed PiN diode

Results and Discussion

1. Forward current stress tests and PL imaging measurements

Fig. 3 shows the changes in the ΔVf caused by the forward current stress for both the substrates. In the case of the 4H-SiC bulk substrate, the ΔVf were obtained over the wide range of 50 mV to 400 mV depending on the applied forward current stress. In particular, the ΔVf abruptly increased at the forward current density of 1000 A/cm^2 or more. Unlike the bulk substrate, the ΔVf for the 4H-SiC bonded substrate remained low and the variation among the measured diodes was extremely small even after applying the highest current density of 1500 A/cm^2.

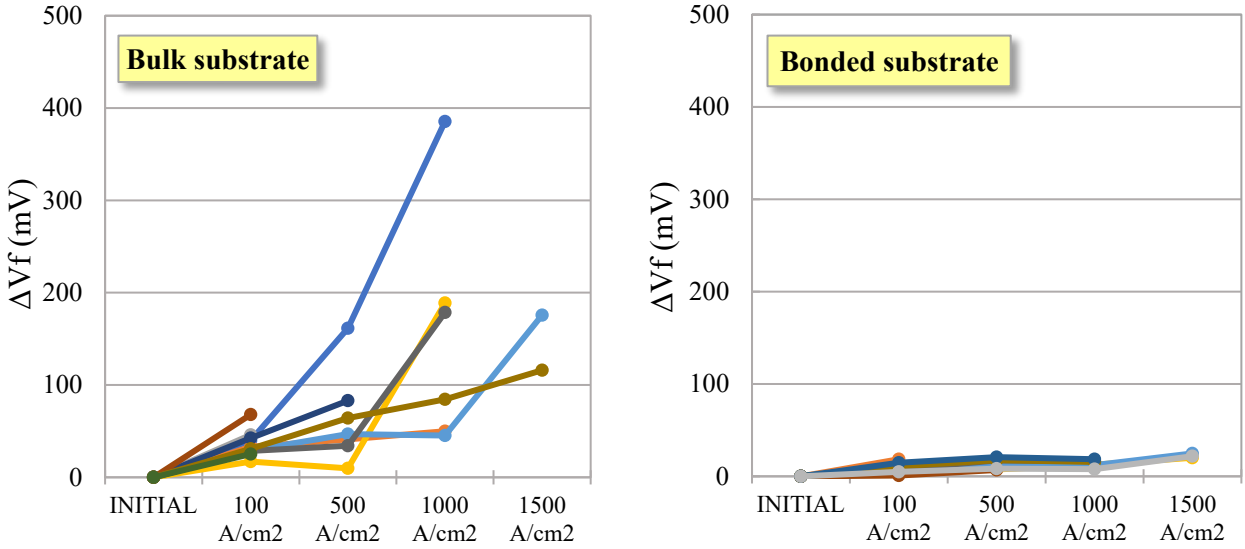

Fig. 3: Changes in the ΔVf caused by forward current stress for the PiN diodes fabricated on both the substrates (Number of the measured diodes = 10)

Fig. 4 shows the plot of the correlation between the total area of SSFs and the ΔVf. PL images of the diodes with the specific ΔV of (a)83 mV, (b)178.6 mV, and (c)20.1 mV are shown together. For the 4H-SiC bulk substrate, the ΔVf showed nearly linear relationship with the total area of SSFs. Many triangular SSFs were observed at around 100 mV (Fig. 4 (a)). In addition, not only typical triangular but also large bar-shaped SSFs [4] emerged at around 200 mV (Fig. 4 (b)). In contrast, the 4H-SiC bonded substrate maintained the small ΔVf, which were less than 40 mV, for all diodes and few SSFs were observed within them (Fig. 4 (c)).

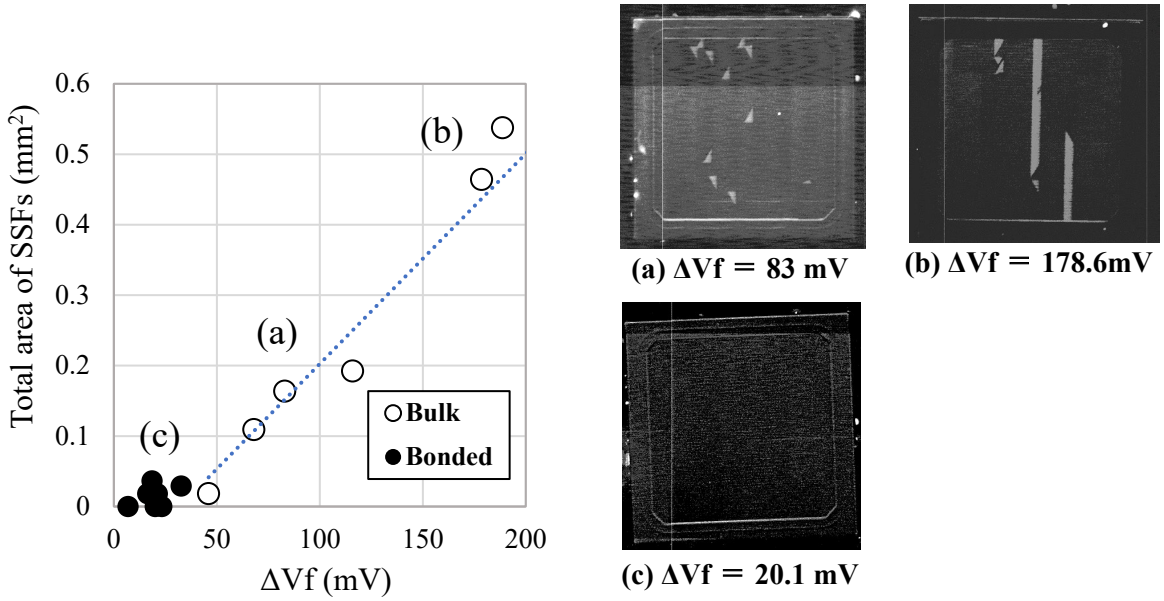

Fig. 4: Plot of correlation between total area of SSFs and ΔVf
(Right side) PL images of the diodes with the specific ΔV of (a)83 mV, (b)178.6 mV, and (c)20.1 mV

These results indicate that the ΔVf in Fig. 3 reflects the total area of the expanded SSFs depending on the forward current stress. The distinct difference between the bulk substrate and the bonded substrate in Fig. 3 is the number and size of the expanded SSFs induced by forward current stress.

As for the bulk substrate, a prior study using transmission electron microscopy analysis confirmed that the origin of SSF expansion under a forward current density of more than 500 A/cm^2 was a BPD that converted into a threading edge dislocation (TED) existing below the epilayer/substrate interface [5]. It's also reported that the depth of a BPD–TED conversion point, which was the starting point of SSF expansion, became deeper with an increase in applied forward current density, such as 550 nm (for 1000 A/cm^2), 698 nm (for 1250 A/cm^2) and 825 nm (for 1500 A/cm^2). Additionally, it is thought to be due to TED glide that a BPD–TED conversion point could move below the epilayer/substrate interface.

Fig. 5 shows a schematic drawing of TED glide. TED glide is a phenomenon in which the TED moves in opposite direction of [11$\bar{2}$0] due to continuous BPD-TED conversion to reduce the total length of dislocations during epitaxial growth [6] or high temperature annealing [7]. As the TED moves, its conversion point also can move downward with a depth more than several hundred nanometers.

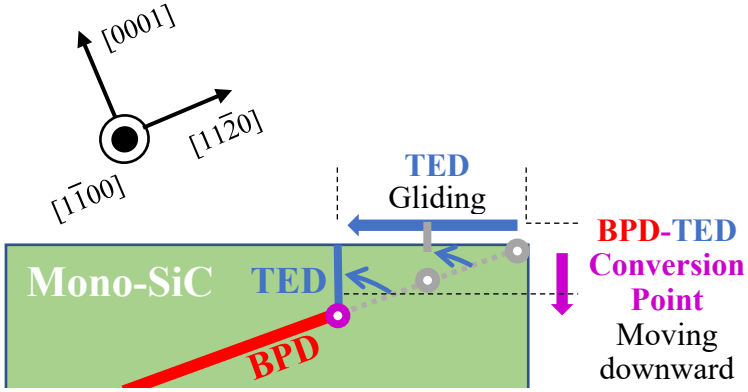

Fig. 5: Schematic drawing of TED glide

2. Investigation of the number of bar-shaped SSFs expanded within the electrically stressed diodes with high forward current density

The main origin of the SSF expansion under relatively high forward current stress is the BPDs converted into TEDs below the epilayer/substrate interface, which is mainly converted into bar-shaped SSFs [8]. This means that the number of bar-shaped SSFs within the electrically stressed diodes with high-forward current density gives the information on the BPDs existing in deep positions below the epilayer/substrate interface. To clarify the difference in such BPDs for both the substrates, the number of bar-shaped SSFs within the electrically stressed diodes was investigated.

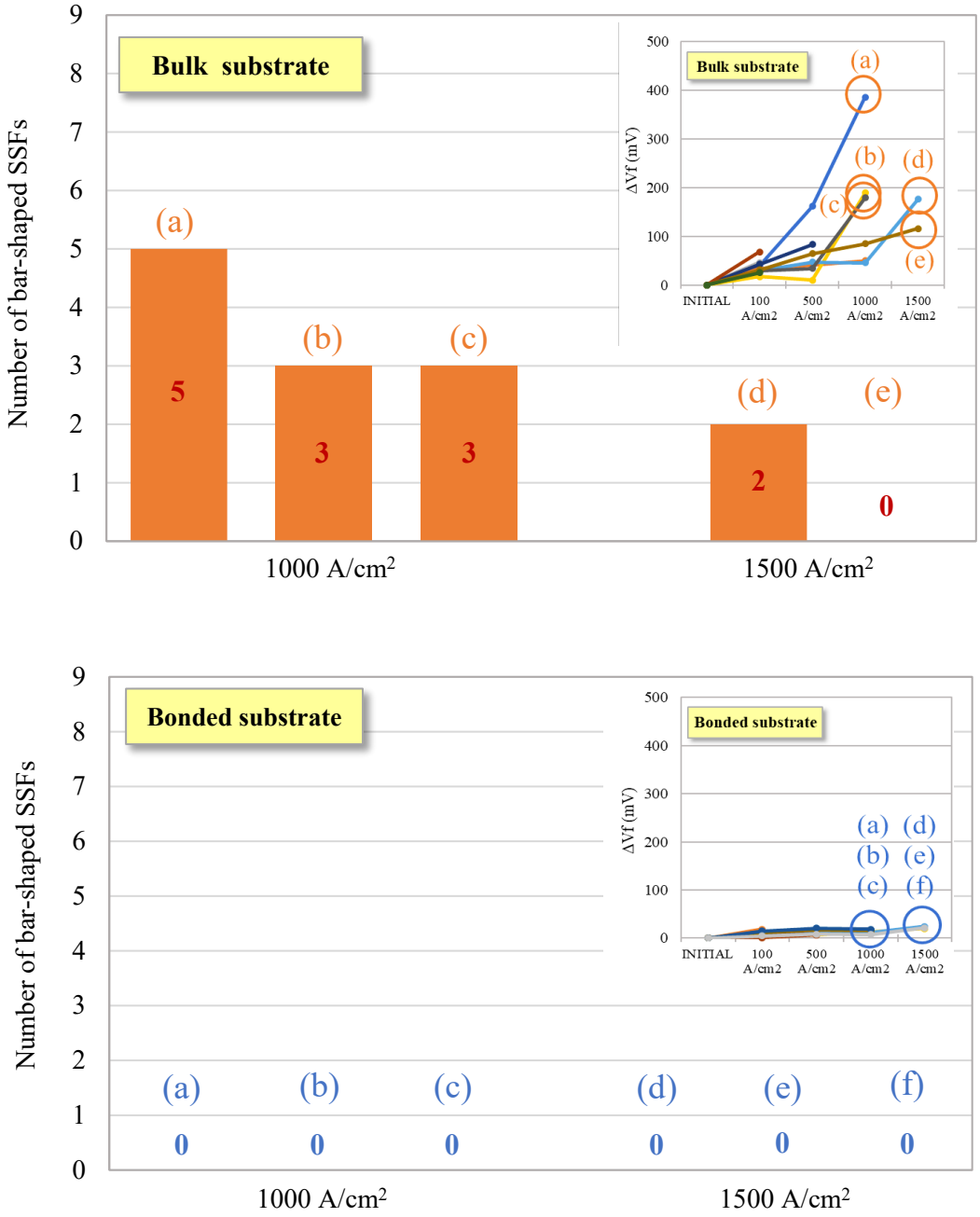

Fig. 6: Difference in the number of bar-shaped SSFs expanded within the electrically stressed diodes with 1000 and 1500 A/cm^2 for both the substrates

Fig. 6 shows the difference in the number of bar-shaped SSFs expanded within the electrically stressed diodes with 1000 and 1500 A/cm^2 for both the substrates.

In the bulk substrate, some bar-shaped SSFs were observed in almost all the investigated diodes electrically stressed at 1000 A/cm^2 or more. These results are consistent with the previous study [5] and therefore suggest that some BPDs at the submicron depth below the epilayer/substrate interface contributed to SSF expansion in the bulk substrate.

In contrast, no bar-shaped SSFs were found from all the investigated diodes in the bonded substrate. This result can be interpreted as that the BPDs located at deep positions below the epilayer/substrate interface were drastically reduced in the bonded substrate.

3. Prediction of the BPD reduction associated with TED glide in the 4H-SiC bonded substrate

The bonded substrate may have a much smaller number of BPDs existing at deep positions below the epilayer/substrate interface than the bulk substrate. One prediction to explain such diffrences in the BPDs for both the substrates is described as follows (Fig. 7).

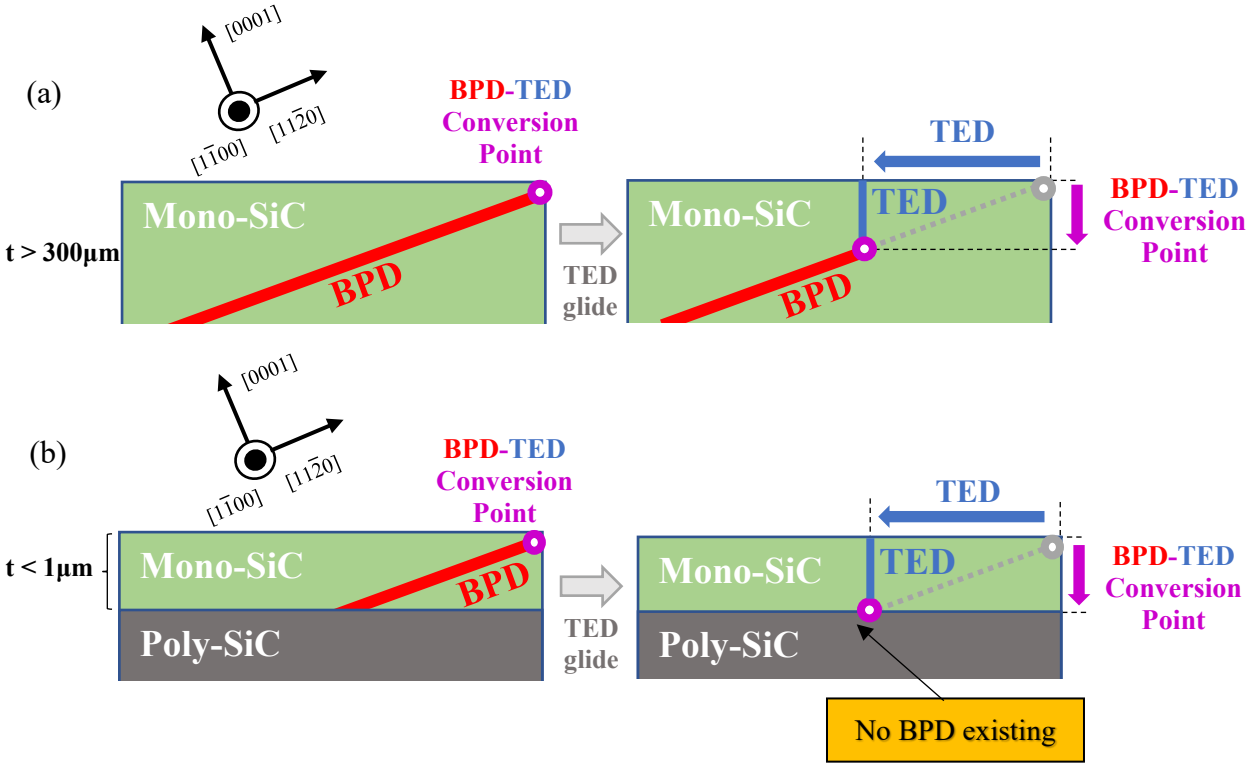

Fig. 7: Schematic drawings of the predicted BPD reduction associated with TED glide in (a) 4H-SiC bulk substrate and (b) 4H-SiC bonded substrate

A BPD–TED conversion mainly starts at the substrate surface in the early stage of the epitaxial growth. Such BPD–TED conversion occurs continuously to minimize the total length of dislocations, which leads to a TED glide and moves its conversion point downward of the substrate. For the bulk substrate, the BPD always exists below the conversion point due to its thick (more than 300-μm thickness) monocrystalline portion (Fig. 7 (a)), which causes SSF expansion under high-forward current stress. The 4H-SiC bonded substrate, on the other hand, has an extremely thin (on the order of submicrons) monocrystalline 4H-SiC layer compared to the bulk substrate. As all BPDs terminate within the monocrystalline layer, no BPD exists below the conversion point if the moving depth of the BPD–TED conversion point reaches the thickness of the monocrystalline layer (Fig. 7 (b)).

This prediction gives an expectation that the 4H-SiC bonded substrate can be greatly advantageous in reducing forward bias degradation in 4H-SiC bipolar devices, particularly, under the high-forward current stress.

Summary

To evaluate the differences in forward bias degradation between a 4H-SiC bonded substrate and a commercially available 4H-SiC bulk substrate, a forward current stress test and subsequent PL imaging of PiN diodes fabricated on both the substrates were performed. Unlike the bulk substrate, the bonded substrate maintained a low ΔVf and the variation among the measured diodes was extremely small even after applying the highest current density of 1500 A/cm^2. The investigated number of bar-shaped SSFs within the electrically stressed diodes with more than 1000 A/cm^2 revealed the possibility that the BPDs existing at deep positions below the epilayer/substrate interface were drastically reduced in the 4H-SiC bonded substrate.

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