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Early Burn-In Parasitic Conduction in 500 °C Durable SiC JFET ICs

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Abstract. All prior reports of long-term 500 °C operation of SiC JFET-R ICs have noted the existence of an initial "burn-in" period of changes in measured electrical characteristics for the first few hundred hours oven-testing. This work reports measurements of "burn-in parasitic MOSFET conduction" that can substantially impact the performance of some circuits during initial heat-up of JFET ICs, but then subsequently disappears after a few hours of operation at 500 °C. The behavior appears generally consistent with the known MOS phenomenon of bias-temperature driven redistribution of mobile ionic contamination. Approaches for further mitigating this initial burn-in conduction mechanism are discussed.

Introduction

Substantial expansion of the practical environmental envelope for integrated circuit (IC) operation offers important benefits to a variety of automotive, aerospace, deep-well drilling, and manufacturing applications [1]. Prior NASA Glenn work has reported fabrication, packaging, and testing of SiC Junction Field Effect Transistor – Resistor (JFET-R) ICs with two levels of interconnect that have uniquely achieved operation in extreme environments including over a year at temperature (T) of 500 °C [2,3]. These reports have noted that the largest observed changes in SiC JFET-R IC electrical properties (prior to eventual passivation cracking induced failure) occur during the initial few hundred hours of high temperature electrical testing. While this circuit behavior in early-testing has been classified as an "initial burn-in" phenomena, the physical mechanisms behind the observed burn-in remain to be investigated. It is important to gain improved understanding of all parameter-drift effects towards achieving mitigation as well as increased technology confidence for infusion. This report describes recent studies of the behavior of one previously identified early burn-in mechanism that we refer to as "burn-in parasitic MOSFET conduction" [4].

Background

In our prior work [4], we observed large imbalance of resistor conduction in a SiC JFET-R differential amplifier circuit fabricated in the prototype run we denoted as IC Gen. 8 (Fig. 1) that we attributed to parasitic Metal Oxide Semiconductor Field Effect Transistor (MOSFET) conduction. During initial heating above 200 °C under intended amplifier biasing, the n-SiC mesa resistor running beneath the positive power supply V_{DD} interconnect trace (denoted by the lighter green dashed line in Fig. 1) exhibited substantially increased current compared to its nearby twin mesa resistor (purple dashed line). The resulting resistance imbalance was fatally detrimental to the operation the during initial heating of the differential amplifier circuit. It was surmised that the +30 V biased V_{DD} trace was helping to create a parasitic inversion n-channel MOSFET enabling an additional current path denoted by red arrows between the two adjacent legs of the green-dashed resistor in Fig. 1. In other words,

the V_{DD} trace functioned as the gate terminal of an inversion channel n-MOSFET formed between the two n-mesas functioning as n-doped source and drain. It was also observed that the resistor current imbalance could be eliminated by applying negative voltage to the V_{DD} trace for two hours at 300 °C [4].

The observed reversible bias-temperature-time stress behavior appears consistent with mobile positive-charge ion contamination phenomenon well-known to be detrimental to MOS devices [5]. Positive ions in the oxide become mobile at elevated T and are repelled by positive V_{DD} bias to migrate closer to the SiC-oxide interface beneath the V_{DD} metal, which in turn reduces the turn-on threshold voltage V_T of the parasitic n-MOSFET. Negative V_{DD} terminal bias high-T attracts positive ions back towards the gate, increasing threshold voltage to turn off the parasitic MOSFET conduction.

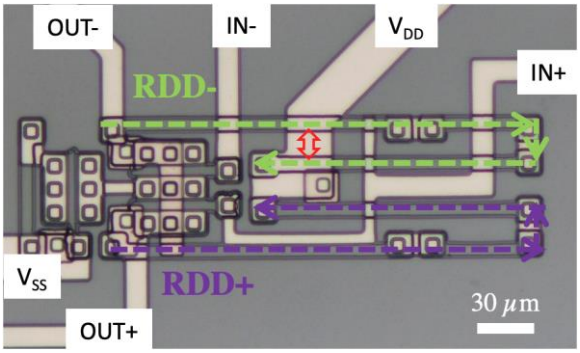

Fig. 1. Annotated optical image of the IC Gen. 8 differential amplifier that exhibited severe resistance imbalance arising from parasitic MOSFET conduction that formed in the p-type SiC beneath the positively biased V_{DD} trace [4].

After surface analysis confirmed the presence of a mobile ion contaminant (sodium) on IC Gen. 8 SiC JFET-R chips, a concerted effort to eliminate sources of mobile ion contamination in the NASA fabrication laboratory was undertaken, including replacement of chemical and wafer handling hardware. Some contamination mitigation practices of the silicon IC industry were also incorporated into the SiC JFET-R IC process (starting with IC Gen. 9), including the introduction of stoichiometric Low-Pressure Chemical Vapor Deposited (LPCVD) Si_3N_4 passivation layers as well as p-type "field stop" (also known as "channel-stop") ion implants into regions between n-mesas. Subsequent mask layouts also avoided V_{DD}-biased first-layer interconnect (Metal 1) traces spanning/bridging separated n-mesas, especially for the case of analog differential amplifier circuits [6].

Experimental

Fig. 2 illustrates the primary test device employed in IC Gen. 10 to study the parasitic MOSFET conduction behavior, wherein the drawing on the left depicts the cross section along the black dashed arrow on the right top view photo (see [2,3] for SEM cross-section of JFET and interconnects from IC 10.1 wafer). This "Field FET" is effectively an inversion channel SiC MOSFET wherein $TaSi_2$ Metal 1 interconnect functions as a 6 µm long by 48 µm wide gate terminal between adjacent n-mesas that function as source and drain terminals. Aluminum was implanted at room temperature into the SiC surface field regions between mesas (self-aligned prior to stripping the mesa etch masks) as the field stop implant towards suppressing conduction between separate n-mesas in the IC. Shallow (~ 0.1 µm) profiles, doping density near 7 x 10^{16} cm^{-3} (5 x 10^{11} cm^{-2} @ 70 keV + 1.8 x 10^{11} @ 35 keV) for Wafer 10.1 and 2 x 10^{17} cm^{-3} (1.4 x 10^{12} cm^{-2} @ 70 keV + 5.0 x 10^{11} cm^{-2} @ 35 keV) for

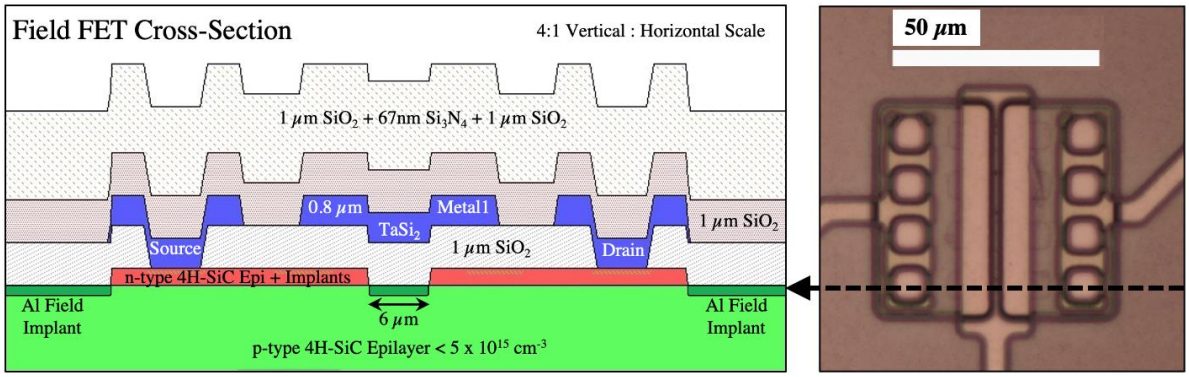

Fig. 2. Cross-sectional schematic drawing (left) and top view optical microscope image (right) illustrating the "Field FET" device structure fabricated on NASA Glenn SiC JFET-R IC Gen. 10 wafers towards characterizing the behavior of parasitic MOSFET conduction mechanism.

Wafer 10.2 were activated along with the n-type SiC JFET-R process implants using SiO_2 capped anneals in nitrogen tube furnace for 100 hours at 1360 °C [2]. Field FET current vs. voltage (I-V) properties were characterized on high-T packaged devices inside air-ambient ovens with gold wires running outside the oven to a terminal strip and connected to computer-controlled DC source measure units (SMU's) that were swept at rates below 1 V/sec. It is worth noting that the high-T packaging process subjects diced chips to 2.5 hours of heat treatment at 600 °C to attach the chip backside to Pt pad patterned on the high temperature co-fired ceramic alumina package with gold thick-film materials [7].

Theory

Simplistically, an inversion-channel n-MOSFET turns on when the applied gate voltage V_G exceeds its threshold voltage V_T. If V_T of the parasitic MOSFET is always larger than $2xV_{DD}$, parasitic MOSFET conduction in SiC JFET-R ICs would be suppressed for even the worst case of a V_{DD} biased Metal 1 trace (+ 25 V) passing overhead of separated n-mesas biased near V_{SS} (-25 V). Since the shortest n-mesa to n-mesa spacing rule of IC Gen. 10 was 6 µm, the long-channel approximation applies for theoretically estimating V_T of the parasitic MOSFET [5]:

$$V_T = V_{FB} + 2\emptyset_F + \frac{\epsilon_S t_{ox}}{\epsilon_{ox}}\sqrt{\frac{4qN_A}{\epsilon_S}\emptyset_F} \qquad (1)$$

where t_{ox} is the SiO_2 thickness (1 µm for Metal 1 gate, or 2 µm for Metal 2 [2,3]), ϵ_s and ϵ_{ox} are the 4H-SiC and SiO_2 dielectric constants (8.6 x 10^{-13} F/cm and 3.4 x 10^{-13} F/cm) and N_A is the p-type aluminum doping density in the 4H-SiC MOSFET channel region. The $\emptyset_F$ term is the bulk semiconductor bulk Fermi potential governed by N_A, T, 4H-SiC intrinsic carrier concentration n_i (itself a function of T) and reverse substrate bias V_S applied relative to the grounded MOSFET source:

$$\emptyset_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) + V_S \qquad (2)$$

where k and q are the Boltzmann and electron charge physical constants. The flat band voltage V_{FB} is governed by:

$$V_{FB} = \emptyset_{MS} - \frac{Q_F}{C_{ox}} - \frac{Q_M\gamma_M}{C_{ox}} - \frac{Q_{IT}}{C_{ox}}. \qquad (3)$$

The $\emptyset_{MS}$ term is the gate metal-semiconductor work function difference and C_{ox} (i.e., ϵ_{ox}/t_{ox}) is the area-normalized oxide capacitance (3.4 x 10^{-9} F/cm^2 for 1 µm thick SiO_2). The charge densities in the insulator are fixed oxide charge Q_F, charge due to mobile ions in the oxide Q_M, and interface trap charge Q_{IT} in Coulombs/cm^2. As discussed in [5], the unitless term γ_M accounts for the integral average depth position of the mobile charge distributed throughout the oxide thickness: γ_M = 1 implies the mobile ion charge resides entirely at the oxide-semiconductor interface (where mobile ions have the largest impact on V_{FB} and V_T), whereas γ_M = 0.5 for a uniform mobile ion distribution throughout the oxide thickness. At sufficiently high-T that enables ion migration, γ_M will increase as positive gate bias repels positive mobile ions closer to the SiC/SiO_2 interface, or oppositely γ_M will decrease under negative gate bias as the mobile ions are attracted towards the gate.

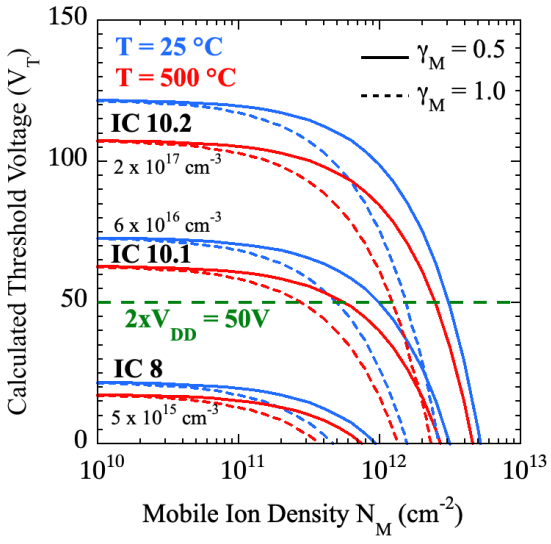

Fig. 3. Plots of theoretical V_T for turn-on of parasitic MOSFETs as a function of mobile positive ion charge density calculated for three different prototype SiC JFET-R IC processes (see text).

Fig. 3 plots a comparison of theoretical V_T calculated at 25 °C and 500 °C using Eqs. (1-3) as a function of the areal density of mobile ions in the oxide N_M (i.e., Q_M/q in units of #/cm^2) for IC Gen. 8 ($N_A \leq 5 \times 10^{15}$ cm^{-3}), 10.1 ($N_A = 6 \times 10^{16}$ cm^{-3}) and 10.2 ($N_A = 2 \times 10^{17}$ cm^{-3}). Bookend values of T and γ_M are compared: $\gamma_M = 0.5$ representing a presumed "initial" state of uniform positive ion distribution prior to bias-temperature stressing and "worst case" $\gamma_M = 1.0$ wherein all positive ions have (repelled by positive gate bias) piled up at the SiC/SiO_2 interface. As the three IC generations were fabricated using the same metal ($TaSi_2$) and insulator processing, it is reasonable to surmise minimal differences in ϕ_{MS}, C_{ox}, Q_F, and Q_{IT} terms in Eq. 3 amongst the three devices. T-independent values falling within literature spreads for $\emptyset_{MS} = 1$ V, $Q_F = -1 \times 10^{12}$ cm^{-2} and $Q_{IT} = 1 \times 10^{12}$ cm^{-2} were assumed for the Fig. 3 calculation, with the understanding that more realistic T-dependent values specific to the SiC JFET-R process remain to be ascertained by future work.

Increasing T from 25 °C to 500 °C has far less impact on Fig. 3 plotted V_T than 4H-SiC doping N_A. The typically employed SiC JFET-R $2xV_{DD}$ of 50 V is marked by the green dashed line in the plot. For IC Gen. 8 that did not employ a field-stop p-type implant, V_T is well below $2xV_{DD} = 50$ V regardless of N_M indicating susceptibility to parasitic MOSFET channel formation. The p-type field-stop implants employed in IC Gen. 10 devices desirably push V_T above 50 V for N_M below 2 x 10^{11} cm^{-2}. However, Fig. 3 indicates that burn-in parasitic MOSFET channel formation remains a risk in IC Gen. 10.2 as ion contamination density N_M exceeds 10^{12} cm^{-2}.

Measurements and Results

Data shown in Figs. 4-7 illustrate examples of the main temperature-bias-time dependent electronic behaviors observed in the IC Gen. 10 Field FET measurements. The packaged Field FET exhibits insignificant conduction until the initial heat-up of the Field FET exceeds 150 °C. With further T increase, parasitic conduction arises under positive Metal 1 gate bias that peaks around 300 °C. Fig. 4 plots a drain current I_D vs. drain voltage V_D characteristic measured with the device at 300 °C during initial heating up to 500 °C roughly corresponding to conditions that largest Field FET currents were observed. It is important to note that V_G bias was applied for 60 seconds prior to the start of each V_D sweep for intended purpose of promoting parasitic conduction. The I_D vs. V_D characteristic does not saturate in a manner consistent with $V_T < 10$ V indicated by initial turn-on at $V_G \leq 10$ V, which suggests that electrically significant ion migration is occurring over the several-minute duration of the SMU I-V measurement.

Fig. 5 illustrates the SMU measured Field FET drain current I_D vs. gate voltage V_G behavior of the Fig. 4 device measured at constant $V_D = 20$ V drain bias for 0 hours, 2 hours, and 10 hours of electrically biased testing time (t) from initially reaching 500 °C. At 0 hours, the I_D-V_G characteristic near $V_G = 0$V exhibits exponentially increasing current consistent with MOSFET sub-threshold conduction but then saturates and declines following device turn-on. Most importantly, the Field FET current effectively vanished by 10 hours to nA levels consistent with the leakage current floor of the 500 °C packages.

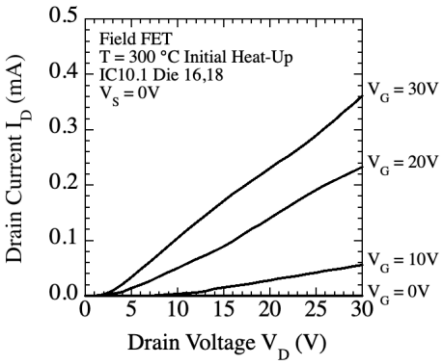

Fig. 4. Measured Field FET I-V characteristics demonstrating increasing parasitic MOSFET conduction with positive gate bias as the device is initially heated to 300 °C (during ramp to 500 °C). No parasitic MOSFET turn-on is observed prior to heating.

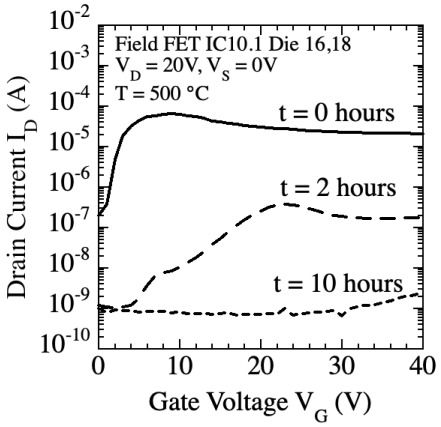

Fig. 5. Measured Field FET I_D vs. V_G plots demonstrating extinction of parasitic MOSFET conduction within 10 hours of biased testing at 500 °C.

It is worth noting that drain current peaks in Fig. 5 at different V_G. Given this observed behavior, the term I_{DMax} is defined to be the peak drain current observed during I_D vs. V_G sweeps measured at under fixed positive drain bias. Fig. 6 plots a comparison between IC10.1 and 10.2 peak Field FET current I_{DMax} measured during I_D vs V_G sweeps under identical initial T ramps to 500 °C. The behavior is similar, but the IC 10.2 Field FET exhibits lower I_{DMax} peak than the IC 10.1 device.

Fig. 7 displays the behavior of I_{DMax} for the IC 10.2 device over two thermal ramps to 500 °C. Between the thermal ramps, the device was burned in at 500 °C for 141 hours and cooled to 25 °C. The 40 V open-circuit package leakage measured between adjacent pads is also plotted. The large parasitic MOSFET conduction observed for the first ramp completely vanishes during the 500 °C burn-in and does not return during subsequent thermal ramping.

X-ray Photoelectron Spectroscopy (XPS) surface analysis conducted following electrical testing observed K (0.6-0.8 at%), Fe (0.4-0.6 at%), and Na (0.3-0.4 at%). The Na was removed after a 1-minute (~ 100 Å) in-situ sputter, but trace amounts of K and Fe remained. The Pt conductive traces showed Ga (6 at%), Fe (3 at%), and Na (2 at%) contaminants on their surfaces. Again, Na was removed after sputtering, but smaller amounts of Ga and Fe remained. The white Al_2O_3 field regions of the packages showed Mg (4-5 at%), Na (1-2 at%), and Ca (0.5-0.9 at%). The die attach material was found to be pure gold after C and O surface contamination was removed by sputtering. Other than a trace amount of S on one of the samples, no other trace elements were detected on the die attach material.

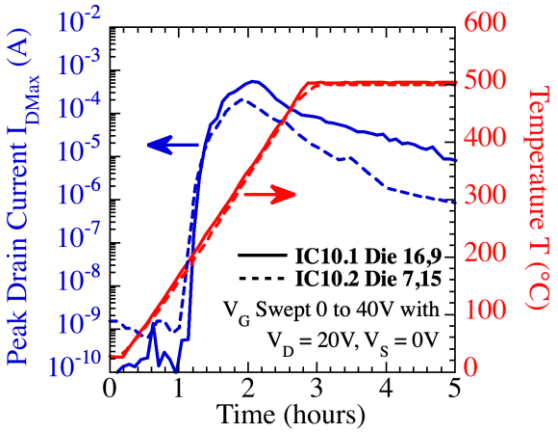

Fig. 6. Comparison of IC10.1 and 10.2 peak Field FET drain current I_{DMax} observed during identical initial T ramps to 500 °C.

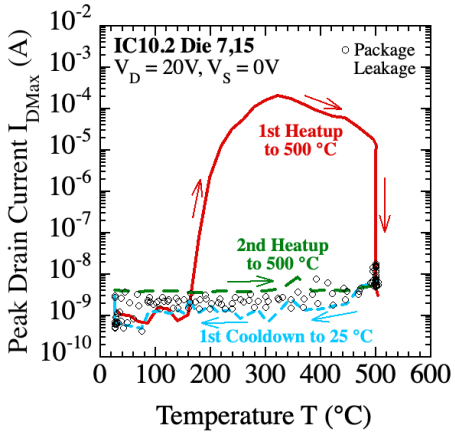

Fig. 7. Plot of IC10.2 peak parasitic MOSFET current I_{DMax} vs. T recorded during 1st heatup and 141 hour bake at 500 °C (red), cooldown (blue), and 2nd heatup to 500 °C (green). The measured package leakage current is also plotted.

Discussion

Despite processing revisions implemented since IC Gen. 8, the results of this study indicate that parasitic MOSFET formation remains as an issue for design and deployment of SiC JFET-R ICs. Given the experimental evidence gathered to date, O_2:N_2 (simulated air) annealing of the wafers prior to dicing should be attempted to ascertain if effective burn-in after heating in oxygen might be accomplished prior to dicing and packaging. Additionally, alternative packaging and ovens should be investigated towards minimizing mobile ion contamination. Presently, the wafer processing is done in reducing environments such as Ar:H or N:H forming gas with dielectrics deposited using tetraethyl orthosilicate (TEOS), ammonia, and dichlorosilane precursors. These chemistries could conceivably leave non-fully reacted ions at the SiC/SiO_2 interface. Additional impurities (including Fe) in the $TaSi_2$ sputtering and/or reactive ion etching could be left at the metal interconnect surfaces. All these possible sources of mobile ions might be passivated or migrate out of the sensitive MOSFET channel region under electrically biased high-T air annealing. The observed permanent extinction of parasitic MOSFET conduction upon exposure to 500 °C suggests that mobile ion source is finite in nature. If the mobile ions were supplied by the ceramic packaging materials, such an impurity source would be expected to sustain parasitic conduction for far longer duration (as a nearly indefinite supply of impurities) inconsistent with the observed short-term burn-in electrical behavior.

Engineering tradeoffs remain to be investigated for accomplishing further reduction of burn-in parasitic MOSFET conduction, complete suppression of which would improve technology capability and infusion. For example, Metal 1 traces tied to -V_{SS} bias can be routed to interrupt parasitic channel MOSFET conduction between mesas/devices residing beneath Metal 2 V_{DD} power. Greatly increased field-stop implant doping can also shift the parasitic MOSFET V_T towards withstanding higher contamination levels, but this could also require significantly higher implant and/or activation temperatures. If completely successful, the higher field-stop implant dose approach would remove metal routing restrictions to achieve higher circuit packing density while perhaps also supporting lower-purity packaging materials and operational environments.

Conclusion

Further electrical studies of parasitic MOSFET conduction that can adversely impact SiC JFET-R IC operation during the first hours of high temperature operation have been described. While burn-in and layout strategies exist for effective mitigation of this short-duration burn-in effect, it is hoped that future work will lead to complete elimination of this phenomenon.

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