Key Engineering Materials
ISSN: 1662-9795, Vol. 948, pp 83-88
doi:10.4028/p-86f73x

Submitted: 2022-09-03
Revised: 2022-12-02
Accepted: 2022-12-04
Online: 2023-06-06

Optimization of $TaSi_2$ Processing For 500 °C Durable SiC JFET-R Integrated Circuits

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Keywords: $TaSi_2$, Tantalum Silicide, Sputter Deposition, Film Stress, IC fabrication

Abstract. Experiments are described towards optimizing tantalum silicide ($TaSi_2$) interconnect metal film sputter-deposition and annealing in a manner compatible with the NASA Glenn two-layer interconnect silicon carbide (SiC) JFET-R IC process flow. Films deposited on 100 mm diameter wafers were investigated over a range of film thickness, sputter deposition, and post-deposition anneal conditions. An optimized process that achieved $TaSi_2$ films free of cracking and morphological defects while nearly halving post-anneal stress was developed and will be used for completing the interconnect fabrication of prototype IC Gen. 12 SiC JFET-R ICs.

Introduction

Early prototypes of 500 °C durable electronics were fabricated on 50 mm 6H-SiC wafers with only one layer of interconnect metal [1]. The first report of the NASA Glenn 4H-SiC JFET-R process on 75 mm diameter wafers using $TaSi_2$ as a two-layer interconnect for 500 °C durable integrated circuit (IC) electronics was in 2015 [2]. With successive improvements in design and fabrication of SiC JFET-R ICs, the transistor count has increased to over 1000 per chip. The JFET-R process has demonstrated operation over 1000 °C temperature (T) span without significant change to output and input signals, radiation hardness $\geq$ 7 Mrad(Si) total ionizing dose and Au heavy ion strikes, and operation for over a year at 500 °C and 60 days in Venus surface conditions[3]. The current in-process JFET-R circuits (designated IC Gen. 12) employ larger die size (5 mm x 5 mm) and larger SiC wafer size (100 mm). These changes will only exacerbate the $TaSi_2$ cracking previously reported at ICSCRM 2019 as a crucial technology limitation requiring further improvement [4]. This ICSCRM 2022 contribution describes more recent experiments aimed at optimizing $TaSi_2$ interconnect metal film deposition and annealing in a manner that is compatible with the two-layer interconnect SiC JFET-R IC process flow.

Experimental

During dielectric depositions employed to realize the SiC JFET-R IC two-level interconnect stack, patterned $TaSi_2$ interconnect features get subjected to at least 720 °C process temperatures for tens of hours. *Therefore, the driving hypothesis is that the minimization of $TaSi_2$ film stress after tens of hours at 720 °C of thermal processing is far more important than minimizing stress of as-deposited films.* For expediency, the experiments were broken into three major sub-studies accomplished in parallel. The first experimental sub-study employed a standard RF magnetron CMS-18 deposition tool (one not used for IC interconnects) [5] that nevertheless guided understanding to down-select $TaSi_2$ film deposition parameters. $TaSi_2$ films deposited in this CMS-18 tool with a fixed target to substrate distance >180 mm was also employed for the second sub-study, that investigated changes to $TaSi_2$ film properties as a function of post deposition anneal conditions. The third experimental sub-study was carried out using the same close-proximity $TaSi_2$ pulsed-DC sputter system (that we refer to as the "YZT" sputter system) used for the fabrication of recent-generation IC interconnects.

This close-proximity YZT sputter system features target to substrate distance adjustable from 18 mm to 118 mm is custom-designed for realizing more conformal films in thickness and density compared to the CMS-18 system necessary for the 1-2 µm topological features that arise during the SiC JFET-R fabrication process. The improved film properties are achieved via much closer-proximity and time-programmed lateral movements of the wafer relative to the target not possible with the CMS-18 system. Additional capabilities of the YZT system not available in the CMS-18 include in-situ wafer heating up to 720 °C and in-situ localized wafer curvature measurement system [6].

For all three study phases, $TaSi_2$ films were initially deposited onto 100 mm diameter silicon (Si) wafers purchased with a 1 µm thick thermal SiO_2. The most crucial Si-wafer experiments were subsequently re-run on 100 mm 4H-SiC wafers with a 1 µm-thick SiO_2 films deposited by low-pressure chemical vapor deposition (LPCVD) using tetraethyl orthosilicate (TEOS) precursor (the same process as that used during actual the SiC JFET-R IC fabrication). A TOHO FLX 2320-S film stress analyzer [7] was used to measure/map the wafer bow before deposition, after deposition, and after post-deposition anneal (PDA), to determine stress measurements as a function of temperature up to 350 °C. The first two studies with films deposited in the CMS-18 measured stress linearly along two lines parallel and perpendicular to the major flat. The stress measurements for the third study with films deposited in the YZT system used a 3D map of stress across the wafer generated by multiple scans of the wafer in the stress analyzer. Only film stresses that were maximum at the center of the wafer and exhibited smooth uniform stress profiles were considered ideal. For example, a film stress map that represented a sombrero hat, saddle, or torus would not be ideal and was excluded. A PhenomXL [8] Scanning Electron Microscope (SEM) with Energy-Dispersive Spectroscopy, KLA stylus profilometer, and Polytech [9] optical profilometer were used to measure film thickness, characterize film morphological structure, and critically ascertain if there was any cracking in the films that would nullify quantitative stress comparisons.

Using the "optimal" deposition process ascertained via the above experiments, $TaSi_2$ films were blanket deposited in the YZT onto two 4H-SiC test wafers with ~ 1 µm deep trench patterns already dry-etched into their TEOS SiO_2 layers for the purpose of simulating deposition surface topography encountered during actual SiC JFET IC fabrication. One test wafer had oxide trenches with vertical (90°) sidewalls etched using C_4F_8 Reactive Ion Etching (RIE) [50 W, 5 sccm C_4F_8, and 35 sccm Ar at 50 mTorr] in a parallel plate system, while oxide trenches on the other test wafer were etched using SF_6 RIE [50 W, 5 sccm SF_6, and 35 sccm Ar at 15 mTorr] that produced 60° trench sidewall slope angle. The as-deposited $TaSi_2$ film was then RIE patterned [50 W, 5 smm SF_6, and 35 sccm Ar at 15 mTorr] using a photoresist mask into a variety of metal conductivity test devices including narrow (6 µm, IC Gen. 12 minimum metal trace width) and wide (45 µm, IC Gen. 12 power bus width) test traces, with some patterned $TaSi_2$ traces crossing dozens of oxide trench features while others resided entirely on regions of flat oxide. All devices on each test wafer were electrically mapped using a computer-controlled automated probing station with DC source-measure units documenting the current vs. voltage (I-V) and resistance of each metal trace device at 25 °C prior to annealing, and after each in a series of increasing temperature 1-hour anneals in nitrogen.

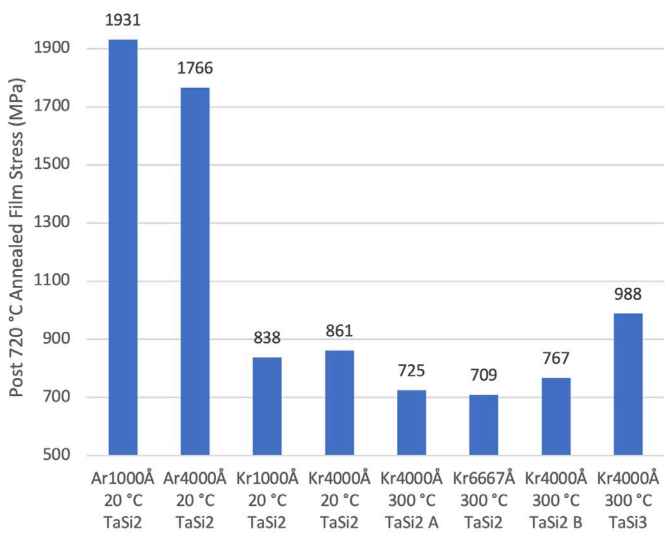

Fig. 1. Measured maximum stress of 720 °C annealed conventional-sputtered $TaSi_2$ films across various process conditions (see text).

Results

Conventional Sputtering (CMS-18). Fig. 1 summarizes the maximum measured stress for $TaSi_2$ films sputtered onto Si-SiO_2 wafers under various deposition processes in the conventional sputtering system (i.e., CMS-18) after 720 °C nitrogen PDA in a tube furnace. For all the entries on the Fig. 1 chart the sputter deposition pressure was 6 mTorr, the gun power was 90 W, and the PDA stresses were tensile. 1000 Å and 4000 Å thick films were studied as they were below the critical film thickness with stable microstructures. The relevant process trends indicated in Fig. 1 are: (a) Kr carrier gas produced lower PDA $TaSi_2$ stress than films sputtered with Ar carrier gas, (b) $TaSi_2$ sputter target produced marginally lower PDA stress than $TaSi_3$ sputter target, (c) Wafer temperature of 300 °C produced lower PDA stress than wafer temperature of 25 °C during deposition, (d) PDA $TaSi_2$ stress increased somewhat with target age (5^{th} bar from left vs. 7^{th} bar from left of Fig. 1), but the difference is small compared to the impact of carrier gas. With respect to carrier gas composition, the efficiency of material ejection from the target is believed to be the major factor instead of trapped gas since the effect remains following PDA and there is also no difference in optimal deposition pressure. A consistent trend of PDA stress as a function of $TaSi_2$ film thickness was not observed.

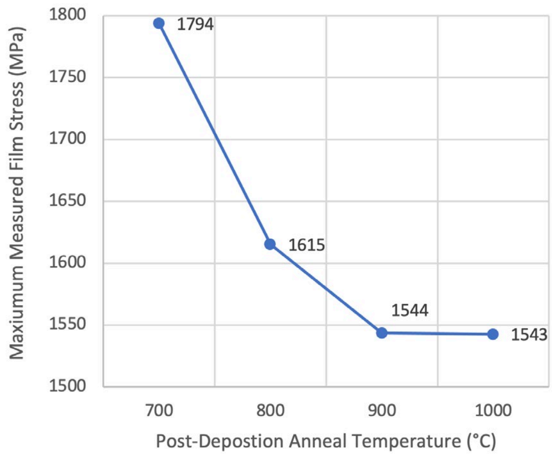

Fig. 2. $TaSi_2$ PDA film stress as a function of anneal temperature (CMS-18 with Kr).

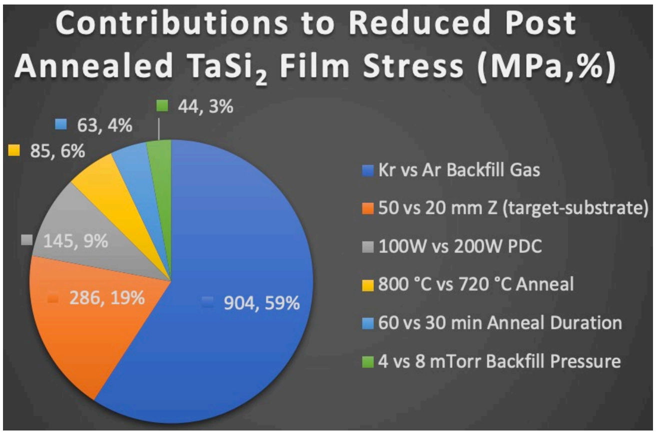

Fig. 3. Pie chart illustrating deposition and annealing process variable contributions to the reduction in $TaSi_2$ achieved in the YZT close-proximity sputter deposition system.

Post Deposition Anneal (PDA). Fig. 2 data indicates that the maximum stress measured in conventional (CMS-18) sputtered $TaSi_2$ films decreased with increasing PDA temperature up to 900 °C. While not shown, it is worth noting that PDA $TaSi_2$ film stress exhibited minimal change as anneal duration was increased from 30 minutes to 2 hours. Similarly, decreasing PDA from 30 minutes to 15 minutes resulted in minimal change.

Close-Proximity Sputtering (YZT). The results obtained from $TaSi_2$ films deposited in the close-proximity YZT sputter system generally followed trends seen in the conventional sputtering system experiments. However, additional YZT capabilities facilitated important relevant understandings. The optimal process target to substrate distance was found to be 50 mm, more than twice the 20 mm distance employed for the fabrication of prior SiC JFET-R IC generations [1-3]. The changed sputter

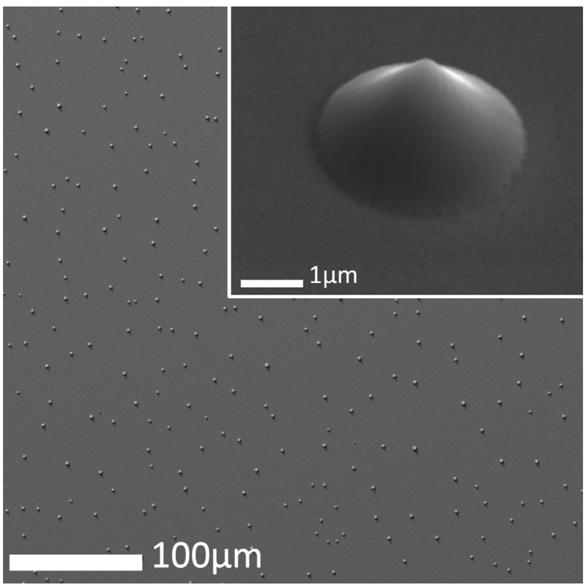

Fig. 4. SEM images of Si-rich $TaSi_2$ droplets that formed during PDA on films deposited at substrate T above 300 °C.

distance as well as wafer size increase from 75 mm to 100 mm necessitated revision of the YZT stage motion program to attain sufficiently uniform film thickness across the wafer. The optimized sputter process also halved sputter gun power (decreased from 200 W to 100 W) and the carrier gas was changed from Ar to Kr based on results from the earlier CMS-18 experiments. Ne carrier gas sputtering was also attempted, but deposition rates obtained were impractically small. Increasing the standard PDA to 800 °C and 1 hour duration were smaller contributions to reducing stress compared to the changes mentioned above. The pie chart of Fig. 3 summarizes relative contributions of various process changes to the stress reduction achieved in these experiments relative to the baseline for that variable employed in the IC Gen. 11 $TaSi_2$ YZT sputter deposition process. It is important to note that it is assume that not all deposition parameters are orthogonal and total stress reduction should not be linearly summed. The optimized films were also characterized in the TOHO film stress analyzer system as a function of temperature up to 350 °C and exhibited a high degree of linearity of film stress vs. T behavior very similar to the work of Townsend [10].

It is important to note that PDA film morphology properties played a vital role in the $TaSi_2$ film deposition process optimization. Indeed, Fig. 4 shows an SEM of the PDA surface of what otherwise would have been the lowest-PDA-stress $TaSi_2$ film obtained during these YZT system experiments accomplished at wafer deposition T = 300 °C. The silicon rich $TaSi_2$ droplets are uniformly distributed across the wafer and were not detectable by SEM inspection prior to PDA. The remedy for the silicon rich $TaSi_2$ droplets was to drop the depositions temperature to 70-80 °C following a 1 hour 300 °C dehydration bakeout in the deposition chamber. $TaSi_2$ films that exhibited PDA droplets or cracked surface under SEM inspection were ruled out from both the stress results presented in this paper as well as from consideration as an optimum IC interconnect. All $TaSi_2$ films deposited at wafer $T \geq 400$ °C exhibited cracked morphology in as-deposited state (i.e., prior to any PDA). Some of the higher temperature deposition cracks were visible with an optical microscope, however many wafers exhibited cracks that were only visible with the SEM and localized to confined regions of the wafer surface.

The localized wafer curvature measurement apparatus on the YZT system also revealed “potato chip” deformation of 100 mm wafers (both Si and SiC) taking place while the substrate heater was powered, which was attributed to non-uniformities in the YZT system substrate heater. Since wafers in the YZT system are sputtered on “face down” towards the vacuum chamber floor (facing the sputter gun located below), we took advantage of gravity to place a 2.5 mm thick x 100 mm diameter silicon wafer (polished side down) directly onto the SiC wafer’s backside to better distribute heat from the substrate heater.

Electrical Testing. A substantial percentage of measurements collected on the “as deposited” state exhibited filament-like I-V turn-on behavior (i.e., sharp non-linear current increases) suggesting the presence of thin native oxide that interfered with probe tips making nominal electrical contact with device metal until higher voltages broke down the thin insulator. For the subsequent (PDA) measurements, a “burn-in” I-V sweep to 25 V was inserted immediately before collecting actual wafer data. The probe resistance (Probe R in Table 1) was mapped/measured using adjacent short-circuited probe pad features to provide indication of parasitic series resistance encountered when connecting to the test devices. Metal trace length added by topography (e.g., trench sidewalls) was relatively small and not included in sheet resistance calculations.

Table 1. Summary of "optimized process" 6 μm wide $TaSi_2$ trace wafer map measurements during a sequence of increasing temperature anneals.

Test Wafer	Electrical Measurement	Device Topography	720°C Anneal	800°C Anneal	900°C Anneal	1000°C Anneal	1100°C Anneal
C	Avg. Probe R	Flat	102 Ω	110 Ω	124 Ω	55 Ω	909 Ω
C	% Yield	Flat	94%	96%	96%	93%	55%
C	Avg. RSheet	Flat	3.2 Ω/sq.	2.5 Ω/sq.	2.5 Ω/sq.	2.4 Ω/sq.	5.8 Ω/sq.
C	*% Yield*	*90° Trench*	*80%*	*85%*	*88%*	*91%*	*34%*
C	*Avg. RSheet*	*90° Trench*	*4.2 Ω/sq.*	*3.5 Ω/sq.*	*3.1 Ω/sq.*	*2.6 Ω/sq.*	*6.0 Ω/sq.*
S	Avg. Probe R	Flat	156 Ω	164 Ω	126 Ω	108 Ω	954 Ω
S	% Yield	Flat	93%	98%	95%	94%	44%
S	Avg. RSheet	Flat	3.5 Ω/sq.	2.8 Ω/sq.	2.7 Ω/sq.	2.6 Ω/sq.	5.3 Ω/sq.
S	*% Yield*	*60° Trench*	*76%*	*90%*	*93%*	*97%*	*12%*
S	*Avg. RSheet*	*60° Trench*	*4.7 Ω/sq.*	*3.5 Ω/sq.*	*2.9 Ω/sq.*	*2.5 Ω/sq.*	*7.2 Ω/sq.*

The results shown in Table 1 for 6 μm wide test devices measured after each of the successive PDA's are mostly consistent with wafer mapping results obtained on wider trace widths. Despite the reduction in $TaSi_2$ film thickness (from 0.80 μm to 0.68 μm) from prior IC generations, all PDA average sheet resistances shown in Table 1 fall below the 5 Ω/square model specified in the IC Gen. 12 layout guide [11]. However, 10 Ω/square was selected as the sheet resistance metric for % yield calculations, as SPICE simulations conducted during IC Gen. 12 circuit design have indicated acceptable circuit operation at even higher sheet resistances. The measured sheet resistance and % yield both improved with each anneal below 1100 °C. In most cases, % yields were slightly higher for flat traces compared to traces running through trench topography, while measured sheet resistances exhibited only minor disparities. The performance differences between devices running across 90° sidewall trenches vs. 60° sidewall trenches also appears to be minor.

$TaSi_2$ Deposition Process for IC Gen. 12

As a result of the experimental work outlined above, the following process is planned to be employed for $TaSi_2$ Metal 1 and Metal 2 interconnect metal depositions during fabrication of IC Gen. 12:

(1) Load: 100 mm diameter SiC wafer with 2.5 mm thick silicon wafer heat-spreading puck resting on backside into YZT sputter deposition system and achieve vacuum < 10^{-7} Torr.

(2) Bakeout: Lower substrate heater into position and initiate 10 °C/minute ramp from 25 °C to 300 °C, bake at 300 °C for 1 hour, then turn off heater and cool for additional hour down to 70-80 °C deposition start temperature.

(3) Starting Position: Wafer at 50 mm distance from sputter gun with $TaSi_2$ target and initiate wafer stage rotation.

(4) Deposition Start: Establish 30 sccm Kr gas flow and 4 mTorr chamber pressure before initiating 100 W $TaSi_2$ pulsed DC sputter deposition and starting wafer lateral motion program.

(5) Deposit for 30 minutes: 10 cycles of 3-minute lateral motion program used to achieve uniform film thickness in close-proximity deposition conditions. Nominal average thickness of $TaSi_2$ film thickness is 0.68 μm.

Conclusion

Experiments and understanding leading to the development of an improved $TaSi_2$ metal interconnect deposition process for extreme environment SiC JFET-R IC fabrication have been described. The new close-proximity sputter deposition process more than halves the maximum $TaSi_2$ film stress across 100 mm diameter SiC wafers without significant penalty to conductivity and conformal step coverage performance. Future investigation for further improvements could focus on exploring other deposition methods and adding a third element to the film to improve the conductivity. However, the immediate goal is to apply this revised deposition process in the upcoming fabrication of NASA Glenn IC Gen. 12 interconnect stack towards realizing substantially upscaled 500 °C durable SiC JFET-R chip capability exceeding 2500 transistors per chip.

Acknowledgements

This work was conducted by NASA Glenn Research Center in Cleveland, Ohio USA with funding from the NASA Science Mission Directorate under the High Operating Temperature Technology (HOTTech) and Long-Lived In-Situ Solar System Explorer (LLISSE) projects. The authors are grateful to D. Lukco, K. Moses, M. Mrdenovich, A. Miller, R. Buttler, A. Trunek, M. Lienhard, G. Hunter, G. Beheim, R. Okojie, D. Centeno-Gomez, and T. Kremic for their support.

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