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650V Vertical SiC MOSFETs and Diodes with Improved Terrestrial-Neutron Single-Event Burnout

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Abstract. Silicon carbide (SiC) power devices such as Schottky diodes and metal-oxide semiconductor field-effect transistors (MOSFETs) are susceptible to failure by terrestrial neutron single-event burnout (SEB) while in the high-voltage blocking state. In this study the effects of the drift layer design of 650V SiC vertical power diodes and MOSFETs have been studied. TCAD simulations of different device designs have been performed, and fabricated device single-event burnout (SEB) properties are compared between the devices fabricated. We find that the standard 650V devices have a low area-scaled failure-in-time (FIT/cm^2) such that essentially no failures (0.01 FIT/cm^2) are expected at 400V drain-source bias (V_{DS}) operation and below. An improved design allows the SEB failure rate curve to be shifted downward in failure rate, such that at for a given V_{DS} operation condition, the FIT/cm^2 can be decreased by 10 - 100 times, depending on the V_{DS} value. This allows operation at about 75V higher V_{DS} value with a similar SEB failure rate, allowing these devices to be used in a wider range of applications.

Introduction

Silicon carbide (SiC) power devices such as Schottky diodes and metal-oxide semiconductor field-effect transistors (MOSFETs) are susceptible to failure by terrestrial neutron single-event burnout (SEB) while in the high-voltage blocking state and above a V_{DS} threshold for that device. This is true for silicon-based power devices [1,2] as well as for SiC devices [3-5]. It has been shown that SiC power device failure rates can be described well by a 'universal' relationship between the area-scaled failure-in-time (FIT/cm^2) and the effective field, described by the ratio of V_{DS} and the avalanche breakdown voltage (V_{aval}), or V_{DS}/V_{aval} [4-6]. It has also been shown that SiC MOSFET and diode failures and failure rates are similar, such that typical MOSFET SEB failure is not dominated by gate-related failure or degradation.

In Si devices, it has been shown that the drift design is very important for the SEB performance [7]. In this study the effects of the drift layer design of 650V SiC vertical power diodes and MOSFETs have been studied. SEB testing has been performed at Los Alamos National Laboratory (LANL) using the spallation neutron source [4]. TCAD simulations of the different device designs have also been performed to compare the expected breakdown characteristics of the two device types. The measured SEB characteristics are compared between the devices described here: standard devices (referred to as 'Std' device in the figures), versus the radiation hard 'RadHard' devices.

Experimental

For this study, 650V 15mohm SiC MOSFETs and similarly sized power diodes were fabricated with a standard 'Std' Wolfspeed Gen3 MOSFET design, and other devices (with the same active area) were fabricated with a new radiation hard 'RadHard' design. The design goal is to achieve similar device properties such as the on-resistance and the blocking voltage, while achieving better SEB performance. The device types being compared here were fabricated on multiples wafers for each device type, with thousands of devices fabricated in total for each design compared.

Neutron-induced failure rates were measured as a function of device drain bias (V_{DS}) at 25°C for Wolfspeed SiC MOSFETs and diodes at the Los Alamos Neutron Science Center (LANSCE) utilizing their spallation neutron source, which has a beam energy distribution matching closely to that of terrestrial neutrons produced by cosmic ray interactions with the atmosphere. Devices under test are mounted perpendicular to the neutron beam (for maximum irradiated area), with up to 12 devices irradiated per V_{DS} test condition. The devices are connected in parallel, each with a current limiting resistor and voltage divider circuit such that drain bias across the device can be monitored, and the circuit does not short when a device fails. The neutron fluence and device drain bias are continuously monitored, so that neutron fluence (n/cm^2) at device failure can be recorded for each device. Beam spreading is accounted for when mounting devices at different distances from the neutron detector, as the neutron beam spreads with distance from the neutron point-source. After most or all the devices fail (dependent on V_{DS} and the failure rate at that voltage), a fresh group of devices are mounted, a different V_{DS} is applied, and they are run until devices fail. This is repeated to obtain a complete failure in time (FIT, fails per billion device hours; or FIT/cm^2 of active area) versus V_{DS} data set for the devices under test. Mounting fresh devices ensures that any potential cumulative effects of high-energy neutron bombardment, although not expected, do not affect the outcome.

Device failure by SEB is noted when devices suddenly and catastrophically fail to block, characterized by sudden changes in I_D across the device. This SEB failure is characterized by a large 'crater' formed in the device active area, as shown for the de-capped 650V 15mohm packaged MOSFET in Fig. 1. Devices that do not fail, even after hours of neutron beam exposure at high drain bias, typically do not show device degradation (thus the breakdown is a 'single-event' effect). The failure signature is similar for all device voltage ratings our group has measured (650V to 6.5kV), such that failure due to neutron SEB can easily be verified by de-capping packaged devices and performing visual inspection, as performed here.

The calculation of FIT rate from the neutron fluence to failure follows the approach presented in the JEDEC terrestrial cosmic ray induced effects document, JEP151A [8]. From the devices tested at a given V_{DS} condition, one FIT rate value is obtained for that group of failures. Using the device active area, a FIT/cm^2 value is obtained. The sea level reference flux value for neutrons with $E > 1$ MeV is taken to be 0.005 n/cm^2/sec as used in our previous publications [4-6].

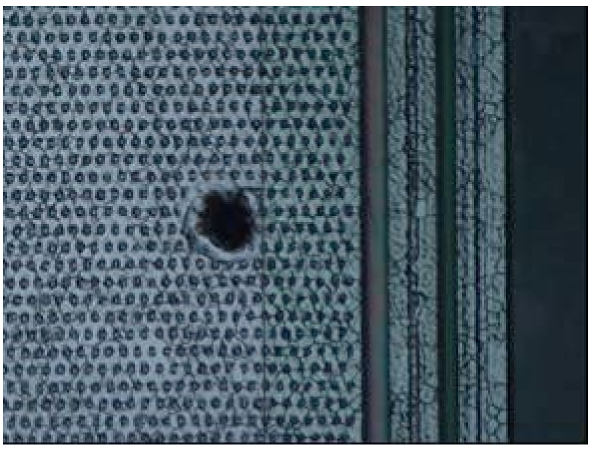

Fig. 1. Single-event burnout failure signature for a de-capped 650V SiC MOSFET. Failure occurs in the active area as expected for an SEB failure.

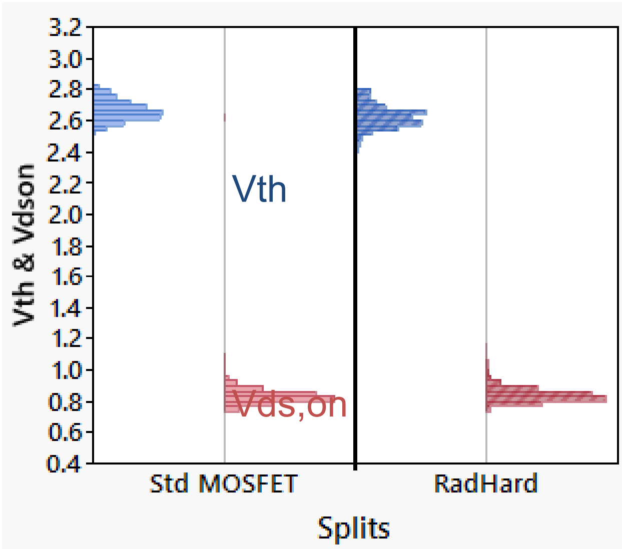

Fig. 2. Comparison of threshold voltage (Vth) and on-state voltage (Vds,on) of >2000 MOSFET devices with standard and RadHard designs.

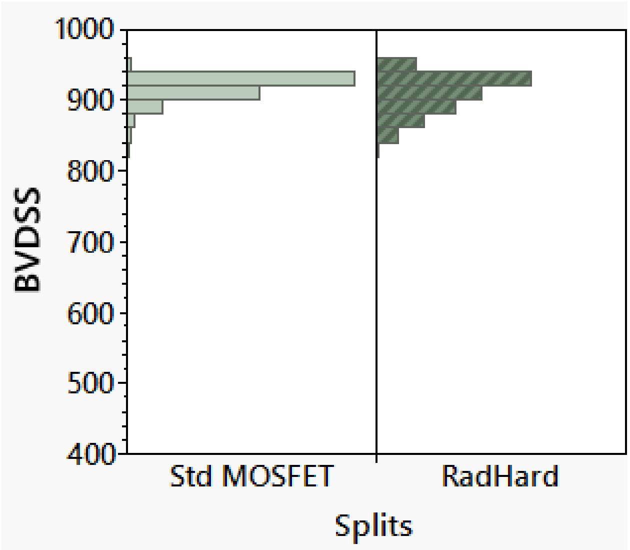

Fig. 3. Comparison of avalanche voltage of >2000 MOSFET devices with standard and RadHard designs.

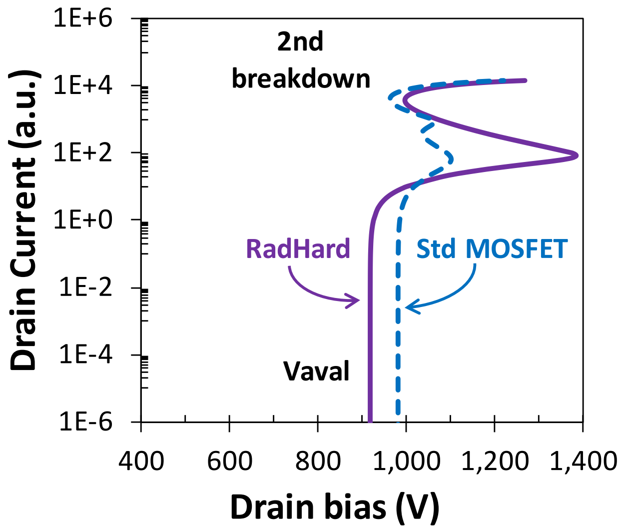

Fig. 4. TCAD simulation of I_D versus V_{DS} showing that the RadHard drift (solid line) is expected to have a lower avalanche breakdown than the standard design (dotted line).

Results and Discussion

Devices for terrestrial neutron SEB testing were taken from a larger population of parts that were fabricated to compare standard and RadHard parts. Figures 2 and 3 show a comparison of the device properties for the designs evaluated, which includes about 2000 parts from each population. Figure 2 shows that the threshold voltage (Vth) and the on-state voltage (Vds,on) are unaffected by the design change. Note that the avalanche breakdown voltage is slightly lower for the RadHard design as shown in Fig. 3, but this agrees with the expectation from TCAD simulations, shown in Fig. 4. The observed spread in device breakdown voltage will tighten as this device enters a production phase, as this variation is not representative of the device itself.

The SEB failure in time scaled by active area (FIT/cm^2) for the MOSFETs and diodes are shown in Figs. 5 and 6, respectively. The points represent the measured FIT/cm^2 rates from 12 devices tested at each V_{DS} value, calculated using the JEP151A approach [8]. The line connecting the data follows a model equation presented by Kaminski [9]. Comparing Figs. 5 and 6, the MOSFET and diode failure rates are practically identical, as previously shown for 1200V SiC MOSFETs and diodes [4]. The Std design MOSFETs and diodes follow the 'universal' behavior we showed previously for SiC vertical devices [4,5]; such that on a plot of FIT/cm^2 versus V_{DS}/V_{aval} this data overlaps with similar data for 900V, 1200V, 1700V, and 3.3kV devices. These results also show that the Std devices have an extremely low failure rate of 0.01 FIT/cm^2 at a V_{DS} of 400V. Thus the standard Gen3 650V MOSFETs and corresponding diodes are expected to operate in a 400V application without experiencing SEB failure. The SEB failure rate increases rapidly as the V_{DS} is increased beyond this, as is typical for SEB failure.

The RadHard designed MOSFETs and diodes have a FIT/cm^2 rate more than an order of magnitude lower than the standard designs, at any given drain voltage. The RadHard designs have failure rates that fall significantly below the universal behavior we published previously [4,5]; or put differently, the FIT rate curve is shifted right to higher drain voltages even with a similar or lower avalanche voltage. Therefore a substantial improvement is achieved using the RadHard design, that is not simply a device over-design of the avalanche voltage. These RadHard devices can thus operate with the same FIT rate at about 75V higher in V_{DS} than the standard devices, thus allowing for a wider range of applications for these RadHard 650V devices.

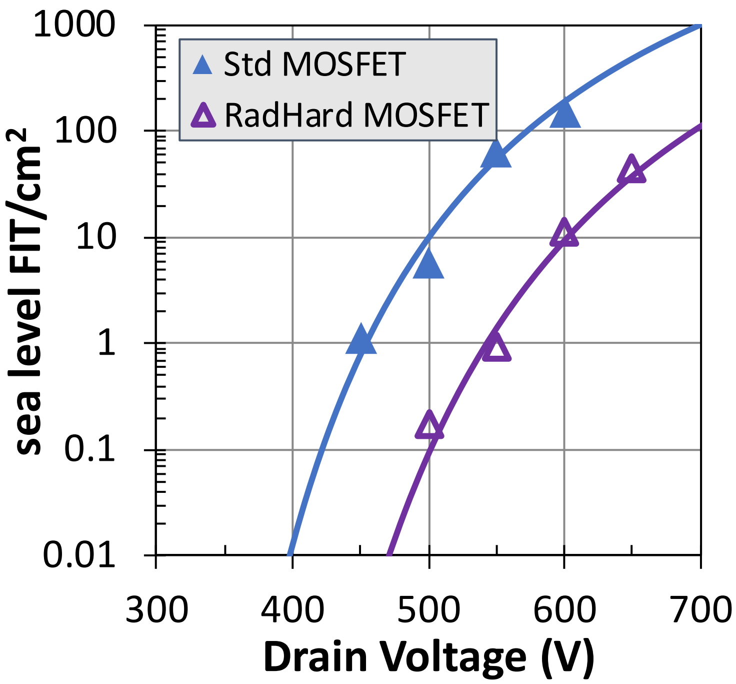

Fig. 5. SEB burnout results showing lower failure rate for the RadHard MOSFET design.

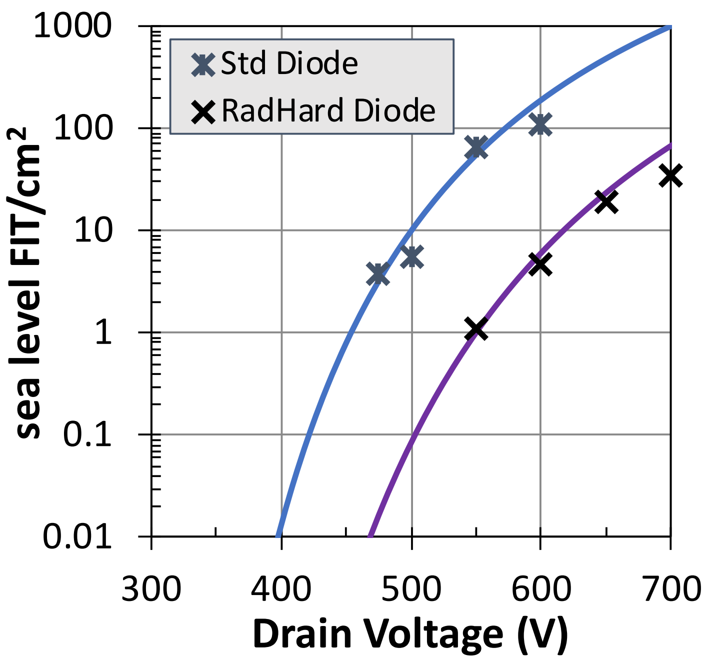

Fig. 6. SEB burnout results showing lower failure rate for the RadHard diode design.

Summary

Terrestrial neutron SEB characteristics have been measured for Wolfspeed Gen3 650V 15mohm MOSFETs, and similarly rated diodes. The standard ‘Std’ devices have a failure rate as low as 0.01 FIT/cm^2 at 400V, making them an excellent device choice for 400V applications. Moreover, devices designed to be more radiation hard have a failure rate ≥10 times lower, such that the failure rate remains below 0.01 FIT/cm^2 up to 470V. Thus the radiation hard devices can be safely operated in higher voltage applications. These ‘RadHard’ devices have failure rates lower than our previously published ‘universal’ behavior for SiC vertical power devices.

References

[1] E. Normand, D. L. Oberg, J. L. Wert, J. D. Ness, P. P. Majewski, S. Wender, and A. Gavron, IEEE Trans. Nucl. Sci. 41(6), 2203 (1994).

[2] H. R. Zeller, Sol. State Electron. 38(12), 2041 (1995).

[3] H. Asai, K. Sugimoto, I. Nashiyama, Y. Iide, K. Shiba, M. Matsuda, and Y. Miyazaki, IEEE Trans. Nucl. Sci. 59(4), 880 (2012).

[4] D.J. Lichtenwalner, A. Akturk, J. McGarrity, J. Richmond, T. Barbieri, B. Hull, D. Grider, S. Allen, and J.W. Palmour, Mat. Sci. Forum Vol. 924 pp. 559-562 (2018).

[5] D.J. Lichtenwalner, B. Hull, E. Van Brunt, S. Sabri, D.A. Gajewski, D. Grider, S. Allen, and J.W. Palmour, A. Akturk and J. McGarrity, IEEE IRPS, pp. 2B.2.1–2B.2.6 (2018).

[6] D.J. Lichtenwalner, D.A. Gajewski, S-H Ryu, B. Hull, S. Allen, and J.W. Palmour, ECSCRM2021, Mat. Sci. Forum, to be published.

[7] S. Liu, J. L. Titus, and M. Boden, IEEE Trans. Nucl. Sci. 54(6), 2554 (2007).

[8] JEP151A, *Test Procedure for the Measurement of Terrestrial Cosmic Ray Induced Destructive Effects in Power Semiconductor Devices*, JEDEC solid state technology association (2020).

[9] N. Kaminski, A. Kopta, Failure rates of HiPak modules due to cosmic rays, Application Note 5SYA 2042-04 (2013).