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Design of Monolithically Integrated Temperature Sensors in 4H-SiC JFETs

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Abstract. In this paper we study and compare two designs of a temperature sensor monolithically integrated to a vertical SiC JFET. One sensor utilizes the standard JFET P+ aluminum gate implantation scheme. The advantage of this sensor is that the integration with a JFET process flow can be achieved with no additional process steps or mask layers. The other sensor uses a combination P-body and a low energy P+ implantation scheme, typically seen in MOSFETs. Both sensors exploit the variation of resistance with temperature of Al doped SiC. Drift-Diffusion simulations of both designs are carried out at fixed temperatures, exhibiting an excellent ~53% relative reduction in sensor resistance from 300 to 450K. However, neither design shows linear behavior with temperature, beginning to saturate at 450K. Electrothermal simulations are also deployed to verify the sensor robustness as the sensor is locate relatively far from the JFET junction. Due to the high thermal conductivity of SiC, the sensor average temperature follows closely the junction temperature. Current crowding (or 2D effects) close to the contact edges is observed in both sensors. We also deploy a simple analytical model to calculate the resistance as a function of the temperature for both sensors. The model agrees with the drift-diffusion calculations, however due to the 2D nature of current flow, a maximum 19.6% relative error is obtained. In general, both sensors deployed similar relative sensitivity, however the P-body sensor resistance changes in a range of 10.6kΩ to 4.95kΩ compared to 700Ω to 330Ω for the P+ sensor.

Introduction

Sensors and electrical control systems are desired for harsh environment operation, in applications such as natural resource extraction, automotive, aerospace and energy production. Silicon based electronics are typically limited to a maximum operating temperature of 200°C due high leakage currents [1]. Due to Silicon Carbides (SiC) larger bandgap of 3.26eV, leakage current is significantly improved, and thus is more suited to high temperature power electronics. Furthermore, the excellent thermal stability of SiC and radiation hardness enables operation in extreme environments such as nuclear systems or space exploration [2]. Typically, temperature sensors are located outside the device packaging away from the device surface. Package temperature is expected to be vastly different to internal device temperature due to the typically poor thermal conductivity of the passivation layers alongside packaging materials. As a result, monolithic integration of a temperature sensor would provide valuable real-time information on the junction temperature (T_j) of the device.

A common approach to developing such a sensor is to monitor a temperature sensitive parameter, such as forward current (I_f) in an Schottky Barrier Diode [3]. Another such design is to use a region uniformly doped with dopants that sit deep in the SiC bandgap. Due to large activation energies, the dopants are significantly affected by incomplete ionization [4]. This results in a varying in the conductivity of the doped region with temperature. In this case, using aluminum, a common P-type dopant which as an ionization energy of 265meV is suitable [5].

Owing to SiC's wider bandgap and excellent thermal conductivity, in theory SiC devices can operate at higher temperatures than silicon devices. In practice, due to thermal limits of aluminum

wire bonds, and silicon gel used in encapsulation, devices are limited to under 200°C. Furthermore, SiC MOSFETs gate oxide utilizes the SiC/SiO_2 interface. This interface typically has an order of magnitude higher density of interface traps (D_{it}) than the Si/SiO_2 interface, which hampers SiC MOSFETs reliability and thus also its ability to operate at extreme temperatures. The SiC gate oxide interface has been an active area of research for the past 15 years and is still being improved to this day [6], [7].

JFETs do not feature a gate oxide, and as such have great potential in high temperature, high reliability applications. In this work, we propose a lateral P+ temperature sensor which utilizes the same implantation schedule as a standard JFET P-type gate implant. This enables the integration of such a sensor into a JFET fabrication process without additional mask layers, or process steps. The second proposed design utilizes a traditional MOSFET P-body and shallow P+ implant schedule, as seen in [4]. This would require an additional mask layer, and further adaption of the JFET process flow. In the following sections, we evaluate the sensors capabilities using a Drift-Diffusion model.[8] This allowed assessment of the sensitivity and linearity of both designs over a temperature range of 300-450K. A simple model has been developed to illustrate the main physical phenomena the sensor experiences with temperature variation, namely increase in dopant ionization and mobility degradation. Electrothermal simulations are also completed to ensure that the sensor temperature will accurately reflect the junction temperature of the device.

Device and Simulation Methodology

In SiC, the impurity level for aluminum sits relatively deep compared to the thermal energy k_BT (265meV). Due to the deep level of the aluminum dopant, it is expected that not all the dopants present in the lattice are ionized in the 300-450K temperature range. The quadratic equation to find the density of ionized dopants or the free hole concentration (p) as a function of N_A (acceptor concentration), E_A (activation energy of the dopant) and N_V (effective density of states of the valence band) is given by.[9]

$$p(N_a, T) = \frac{N_A}{1 + g_A \frac{p}{N_V} \exp\left(\frac{E_A}{k_B T}\right)} \tag{1}$$

Where k_B is Boltzmann's constant, and g_A is the degeneracy factor for acceptor impurities, equal to 4 in SiC. As stated in the introduction, the aluminum energy level considered for this model is 265meV [5]. Fig. 1 shows Eq.1 plotted as a function of T for multiple values of N_a.

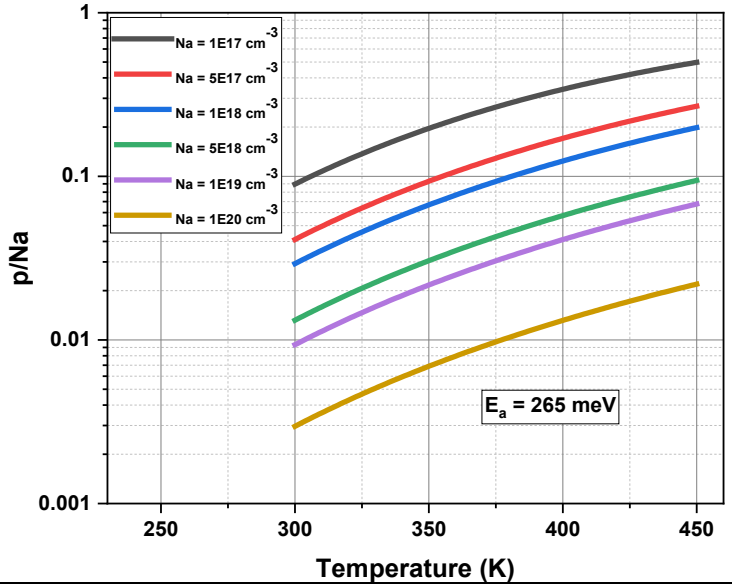

Fig.1. Calculated ratio of active carriers to aluminum impurities in P-type SiC, plotted against temperature. Different aluminum concentrations ranging from 1E17 cm^{-3} to 1E20 cm^{-3} have been considered.

As is clearly shown above in Fig.1, as N_A increases the ratio of p to N_A drastically reduces at all temperatures. Therefore, at higher values of N_A, the effect of incomplete ionization is considerably larger, resulting in ~10% activation for N_A = 1E19 cm^{-3} at 500K, compared to 65% for N_A = 1E17 cm^{-3} at the same temperature. The carrier mobility degradation due to dopants and phonons is parametrized by using Eq. 2. [9]. The 4H-SiC values for the parameters μ_{max}, μ_{min}, N_{ref}, γ and α are shown below in Table 1. [10]

$$\mu_h(T, N_a) = \left(\mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{p(N_a, T)}{N_{ref}} \right)^{\gamma}} \right) \times \left(\frac{T}{300} \right)^{\alpha} \quad (2)$$

Table 1. Material dependent coefficients for 4H-SiC to be used in the mobility model presented in Equation 2. [10].

Symbol	Value	Unit
μ_{max}	125	[cm^2/Vs]
μ_{min}	15.9	[cm^2/Vs]
N_{ref}	1.7×10^{19}	[cm^{-3}]
γ	0.34	1
α	2.15	1

The doping profile of the proposed monolithic sensor, alongside active JFET channels is shown in Fig 2. The drift doping N_D was set to 4E15 cm^{-3}, with a layer thickness of 10µm. Additionally, a standard 350µm substrate thickness with a doping of 1E19 cm^{-3} was used.

The JFET P+ implant has a target concentration of 1E20 cm^{-3}, whilst the MOSFET P-body and P+ ohmic implants have target concentrations of 5E17 cm^{-3} and 1E20 cm^{-3}, respectively. These doping profiles are shown in Fig 3.1. and Fig 3.2. The JFET P+ and P-body implant have been modelled as box profiles with a depth of 1µm. The implants were simulated using kinetic Monte Carlo simulations.[11] To achieve the 1µm box profile, a total of 5 individual implant shots were used, with energies ranging from 40-680keV. Further explanation of Monte Carlo calculation in Synopsys can be found in [12]. The distance between sensor contact pads is modelled as 40µm and contacts are 2µm wide, giving a total sensor length of 44µm. The sensor extends 100µm in the Z-direction.

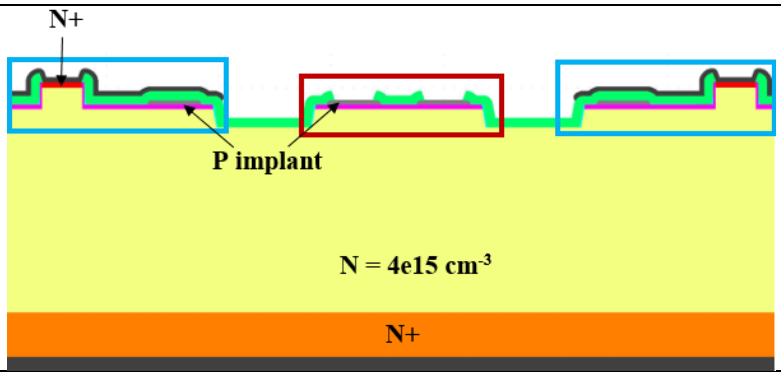

Fig. 2. Doping profile of the proposed design of a monolithically integrated temperature sensor in a vertical JFET. The sensor is highlighted in red, and JFET active cells are highlighted in blue.

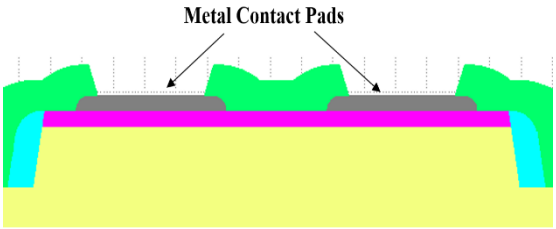

Fig. 3.1. Doping profile of the sensor using the JFET P+ gate implant.

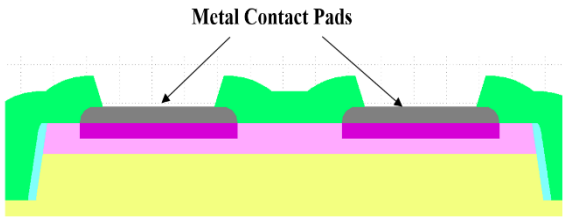

Fig. 3.2. Doping profile of the sensor using a P-body implant. The P+ implant is only located below the metal contacts to enable ohmic behavior.

The calculation of current-voltage characteristics utlises the drift-diffusion approach combined with the Poisson equation. Fermi-Dirac statistics are used to high carrier concentrations (>10^{19} cm^{-3}) being present in the both the P+ regions and the active area of the JFET cells.[13] Bandgap narrowing is also considered. Carrier recombination is captured by both Shockley-Read-Hall (SRH) and Auger models at high concentrations.[14] The doping dependance of the carrier mobility due to lattice (phonon), coulomb and impurity scattering is active. [10] Additionally, the effect of the anisotropic 4H-SiC lattice is also considered. [10] All parameters used for the incomplete ionization model are shown in Table 1. For electrothermal simulations, to solve the heat equation, thermal resistances are used on the top and bottom of the device, and Neumann boundary conditions for the lateral (left/ right) boundary.

Results and Discussion

An electrothermal simulation was firstly completed to verify the main localized sources of power dissipation in the JFET active cells, and furthermore how this translated to the sensor. Fig. 4.1 Shows the 2D temperature profile of the P+ sensor at V_{ds} = 15V, V_{gs} = 0V. The temperature is highest in the JFET channels, which is the highest resistance region of the device. This is reflected in the electron joule heat profile of the device, shown in Fig. 4.2.

It is also observed that the blanket deposited dielectric on the topside of the device, intended to imitate passivation layers on a practical device, experiences a large temperature gradient compared to the rest of the structure. This is due to the poor thermal conductivity of dielectrics, in this case SiO_2.

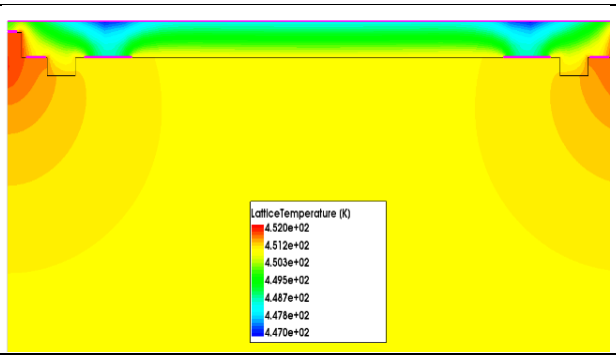

Fig. 4.1 2D temperature profile of the integrated P+ sensor at V_{ds} = 15V, V_{gs} = 0V.

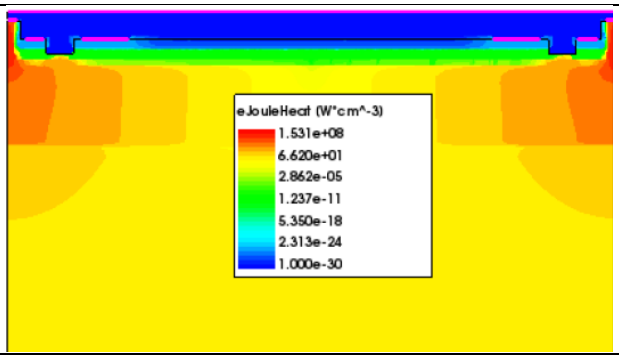

Fig. 4.2 Electron joule heat of the integrated P+ sensor at V_{ds} = 15V, V_{gs} = 0V.

Output characteristics at V_{gs} = 0V for both electrothermal and fixed temperature values of 300K and 450K are shown below in Fig. 5. The electrothermal curve closely resembles the 300K at low V_{ds}, due to the small power dissipation, and thus T_j stays close to 300K. As V_{ds} increases, the power dissipation of the device vastly increases, resulting in T_j to increase significantly. For the JFET active cells, as T_j increases the electron mobility degrades significantly due to elevated levels of phonon

scattering. Thus, the conductivity and therefore I_{ds} reduces in the JFET active cells as T_j increases. As V_{ds} approaches 15V, the electrothermal curve closely resembles the fixed 450K curve. This agrees with Fig. 4.1, which shows T_j is close to 450K at V_{ds} = 15V.

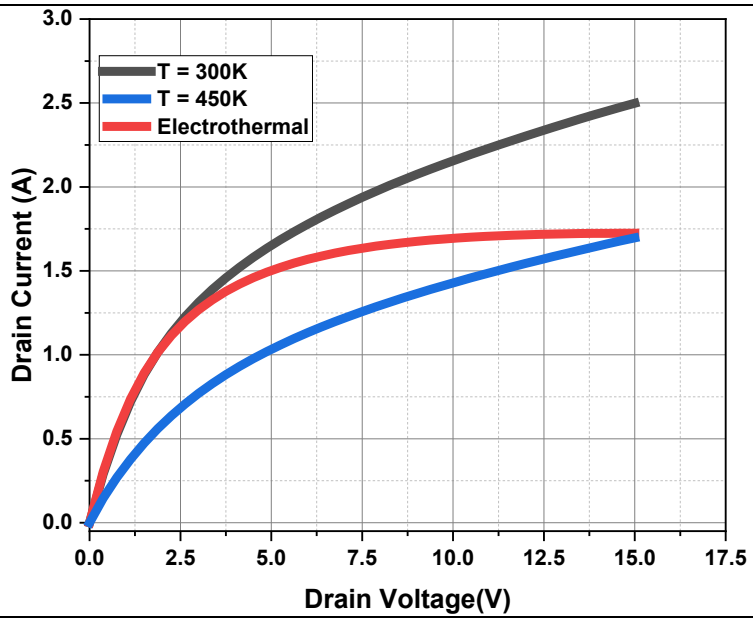

Fig. 5. JFET output characteristics at Vgs = 0V for fixed temperatures of 300K and 450K, compared to the output characteristic from an electrothermal simulation.

When one of the sensor contacts is biased a nominal amount whilst the other is grounded, current flow between the sensor contacts occurs. Current crowding effects are observed at the contact edges in both designs. This is shown below in Fig. 6.1 and Fig. 6.2 for the P+ and P-body sensor, respectively. Due to the higher resistance path of travelling through the P-body region below the contact instead of travelling through the P+ region, a greater degree of current crowding in the P-body design is observed. This may induce contact degradation in practice. Conversely, as the P+ sensor possesses uniform P+ doping throughout the whole sensor region, thus current crowding is reduced. This current crowding is a 2D effect, as the current flow is two dimensional.

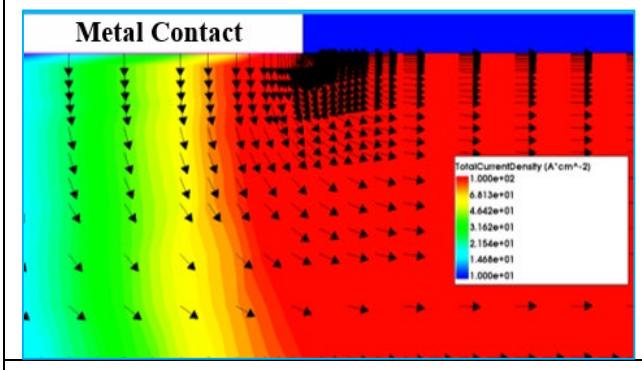

Fig. 6.1. 2D total current density plot displaying current vectors for the P+ sensor.

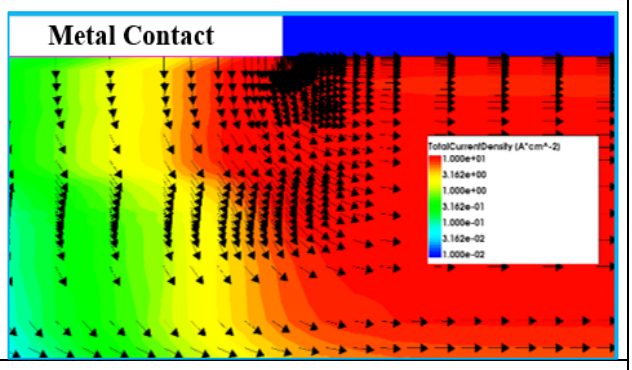

Fig. 6.2. 2D total current density plot displaying current vectors for the P-body.

Sensor resistance (R_{sens}) was tested at fixed temperatures in the range of 300-450K for both designs. R_{sens} as a function of temperature is shown below in Fig. 7. The P+ design has a far lower resistance of 700Ω at 300K, compared to 10.6kΩ for the P-body design. This is expected, as the conductivity of the P+ sensor should be considerably higher, due to N_A being 100 times higher than the P-body. Both designs exhibit an excellent ~53% relative reduction in resistance at 450K compared to 300K to 330Ω and 4.95kΩ, respectively. This is 40% higher than the sensitivity observed in [15] over the same temperature range.

However, it is recognized that R_{sens} does not behave linearly with temperature and is approaching saturation at 450K. Between 400K and 450K, the P+ sensor experiences an 8% reduction in R_{sens}, compared to 29% between 300K and 350K. The P-body sensor is more severely affected – with a 11% and 35% reduction over the same temperature ranges. Primarily, this is due to the diminishing impact of incomplete ionization around 450K, whilst simultaneously μ_h continuously degrades as temperature increases. Thus, incomplete ionization and μ_h partially compensate for each other at 400-450K temperatures, result in resistivity saturating.

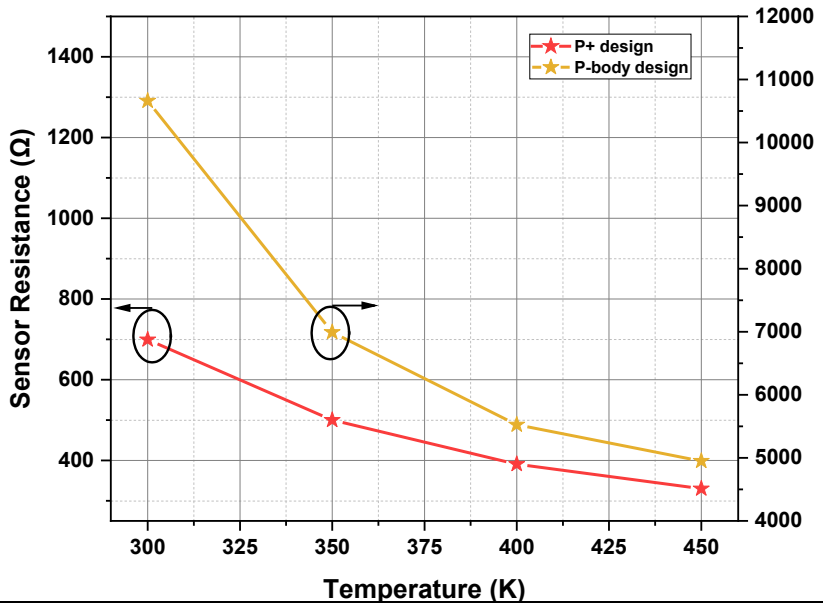

Fig. 7. Resistance of both sensor designs plotted as a function of temperature (V_{sens} = 0.1V).

The behavior of the R_{sens} for both designs' shown in Fig. 7 can be explained by a simple model that combines Eq. 1 and Eq. 2 to calculate sensor resistance. This model considers the sensor as a uniform section of doped 4H-SiC in which the current flow is assumed homogeneous, with contacts located at each end. This is a crude representation of the sensors depicted in Fig 3.1/3.2. For this model, both an area A and a length L must be defined to calculate R_{sens} from the resistivity. Although the total length of the sensor is 44µm, due to the current crowding effects shown in Fig. 6.1 and Fig. 6.2, the total length of the sensor is reduced to 41µm. The width in the Z-direction at 100µm as previously stated. For the depth of sensor, it is assumed that there is minimal vertical current crowding in the bulk of the sensor. Therefore, the depth of the sensor is set to the maximum implantation depth of 1µm.

The analytical model closely agrees with the simulated R_{sens} values for both designs, at all temperatures modelled, as shown below in Fig. 8. At 300K, the model predicts a R_{sens} value of 815Ω for the P+ sensor, 115Ω higher than the drift-diffusion simulation. At 450K, the model predicts R_{sens} = 306Ω, compared to the simulated 330Ω – a 7.2% difference. The P-body design is also predicted accurately at room temperature, with a predicted R_{sens} = 10556Ω compared to 10660Ω – a <1% absolute error. At high temperature, the analytical model diverges slightly for the P-body sensor, predicting to be 16.7 % lower than simulated at Rsens = 4137Ω in contrast to 4950 Ω. In general, the model has a minimum 19.6% accuracy over this temperature range. This is to be expected due as the model assumes uniform current flow through the sensor, which our simulation demonstrated is not the case.

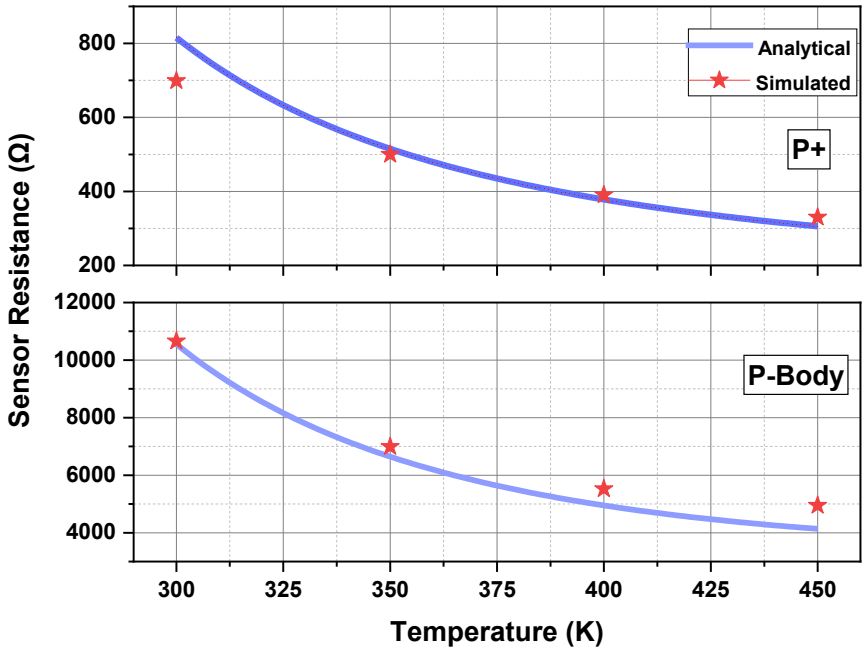

Fig. 8. Comparison of simulated sensor resistance to analytical model over the 300-450K temperature range.

Summary

We have carried out drift-diffusion/electrothermal simulations of a vertical 4H-SiC JFET with a monolithically integrated temperature sensor. The sensor is based in the incomplete ionization of Aluminum dopants in SiC. Two sensor designs have been studied. One design utilizes deep P+ doping and thus is more suitable for integration into a JFET fabrication process. The other follows the standard MOSFET P-body profile. The resistance calculated by the drift-diffusion method agreed within a 17 % error, with a simple analytical model that consider the sensor as a p-doped 4H-SiC region. The deviation between the model and simulation is expected to be associated to two dimensional crowding effects of the current flow close to the metal contacts. The P-body design experienced a larger current crowding effect at the corner of the sensor contacts, which in practice could affect the reliability of the device. The effect of incomplete ionization on the hole concentration induces larger changes in resistance between 300-350K compared to 400-450K, where sensor resistance begins to saturate. The 2D thermal profiles from electrothermal simulation show that sensor temperature follows close the JFET junction temperature in the range of temperatures studied. Neither sensor exhibits linear behavior in the range of temperature studied. From the fabrication point of view, implementing the P-body design into a JFET process would result in a further mask layer being required, unlike the P+ design. Further work will include fabricating the P+ integrated sensor design to verify the simulation work.

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