Ultrafast Pulsed *I-V* and Charge Pumping Interface Characterization of Low-Voltage n-Channel SiC MOSFETs

Mattias Ekström[1,a*], B. Gunnar Malm[1,b], and Carl-Mikael Zetterling[1,c]

[1]KTH Royal Institute of Technology, School of Electrical Engineering and Computer Science, Sweden

[a]mekstr@kth.se, [b]gunta@kth.se, [c]bellman@kth.se

Abstract. Control of defects at or near the MOS interface is paramount for device performance optimization. The SiC MOS system is known to exhibit two types of MOS-defects, defects at the SiO_2/SiC interface and defects inside of the gate oxide that can trap channel charge carriers. Differentiating these two types can be challenging. In this work, we use several electrical measurement techniques to extract and separate these two types of defects. The charge pumping method and the ultrafast pulsed *I-V* method are given focus, as they are independent methods for extracting the defects inside the gate oxide. Defects are extracted from low voltage n-channel MOSFETs with differently processed gate oxides: steam-treatment, dry oxidation and nitridation. Ultrafast pulsed *I-V* and charge pumping gives comparable results. The presented analysis of the electrical characterization methods is of use for SiC MOSFET process development.

Introduction

Defects at the channel interface or near-interface (inside gate oxide) degrade the performance of MOS-FETs. MOSFETs fabricated in silicon carbide (SiC) technology currently suffers from high density of both kind of defects [1, 2]. Typical extracted interface state densities can be in the order of 10^{11}–10^{12} cm^{-2} eV^{-1} [2, 3, 4, 5]. The defects reduce the number of mobile charge carriers and the channel mobility by Coulomb scattering, and they increase noise and subthreshold slope leakage current. Reduction of these defects would improve SiC MOSFETs for power applications and for use in integrated circuits.

In our previous work, we reported lateral low-voltage recessed channel transistors intended for high-temperature integrated circuits [6, 7]. In this work, we present the results of the pulsed characterization of the interface and near-interface defects found in these transistors.

Charge pumping estimates the amount of recombination centers at the gate oxide interface to the channel by pulsing the gate of a gated diode (either reverse biased or clamped at 0 V) from accumulation to inversion and measuring the generation-recombination current. The theoretical basis for charge pumping has been extensively discussed in the literature [8, 9, 10]. The simplest pulsing, a two-level trapezoidal voltage pulse-train, probes the near-interface traps inside of the gate oxide when frequency changes while keeping rise- and fall-times constant [9, 10]. A two-level triangular pulse-train probes both interface recombination centers and near-interface traps when frequency changes [7, 8]. Charge pumping has previously been used to investigate SiC transistors [3, 4, 5, 11].

Ultrafast pulsed measurements measures current at a higher sampling rate (1 sample per 100 ns - 100 μs) than ordinary source-measurement units (1 sample per 100 ms - 1 s). This allows the extraction of dynamic transistor behavior. Ultrafast pulsed measurements can resolve charge trapping with μs resolution. Charge trapping is due to near-interface defects that capture channel carriers. It increases the threshold voltage with increasing time, which causes a decrease in both overdrive voltage and on-state current. By measuring the decrease in on-state current immediately after the rising flank of a voltage pulse, it is possible to estimate the amount of defects inside of the gate oxide. A similar study
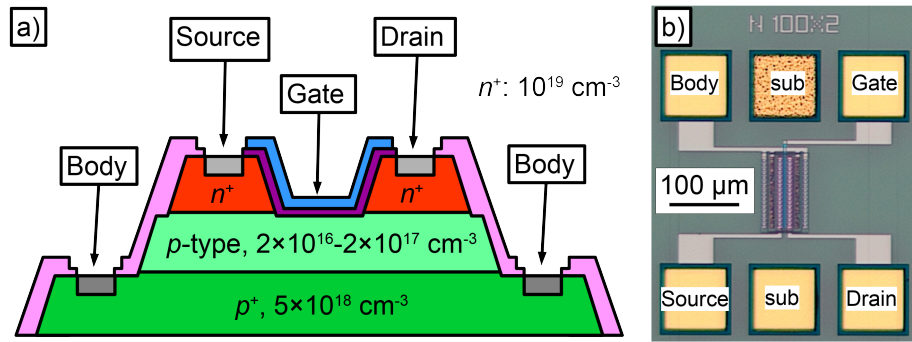
Fig. 1: Lateral low-voltage recessed channel transistor. a) Cross-section of a lateral recessed channel transistor. b) Photograph of a transistor, 100 μm channel width and 2 μm length. This figure is based on Fig. 1 in [6] (CC-BY 3.0).

Table 1: Gate oxide processes. ALD-SiO_2 was deposited prior to treatment. The wafers were first oxidized (either dry oxygen or in N_2O), followed by annealing in nitrogen gas. Only the steam-treated wafer was re-oxidized in pyrogenic steam. All process steps were performed immediately after each other in the same oxidation furnace.

Wafer	Step 1: Oxidation	Step 2: Anneal	Step 3: Re-oxidation
Steam-treated	O_2 / 1050 °C / 10 min	N_2 / 1050 °C / 60 min	H_2O / 950 °C / 10 min
Dry oxidation	O_2 / 1050 °C / 10 min	N_2 / 1050 °C / 60 min	-
Nitrided	N_2O / 1050 °C / 10 min	N_2 / 1050 °C / 60 min	-

was taken by Lelis et al. [12], who found a linear-with-log-stress-time response of threshold voltage in time for commercial SiC power MOSFETs.

Experimental Methods

Three 100 mm 4H-SiC wafers with epitaxy grown by Norstel [13] were processed to give lateral low-voltage MOSFETs, shown in Fig. 1. The gate oxide (SiO_2) was deposited by atomic layer deposition (ALD) to achieve a conformal gate oxide with well controlled thickness. The deposition was performed at 350 °C by using a commercial precursor (Air product AP-LTO-330) and ozone as oxidant. 300 cycle deposition was used, giving a nominal 33 nm thick gate oxide. Following the deposition, the three wafers were differently treated, as given by table 1. One wafer was steam-treated, one wafer by dry oxidation and the last wafer by nitridation in N_2O. Dry oxidation was expected to give the worst performance, although there are claims of good performance by growing a thin oxide at 1050 °C [14]. Steam-treatment has been shown to produce PMOS transistors with high mobility ($\sim$15 cm^2/Vs) [15] and is of interest for SiC CMOS, although the channel electron mobility can be single digit low ($\sim$1 cm^2/Vs) [16]. Nitridation by nitrous oxide (N_2O) or by nitric oxide (NO) is a common method to achieve high-performance NMOS transistors (mobilities around 25–35 cm^2/Vs) [1, 17]. The low temperature and short times were motivated by reducing excessive oxidation on the exposed a-faces present in the recessed channel design [6, 7]. In-situ doped polysilicon (n-type) was used as gate electrode. All three processes gave a capacitance equivalent thickness (CET) of $\sim$34 nm, estimated by split C-V method on large channel area transistors (100 μm $\times$ 100 μm), and using the maximum inversion capacitance as a measure of gate oxide capacitance (C_{ox}) [6, 7]. Details on the other process steps can be found in [6, 7].

   N-channel transistors of 100 μm width and 2 μm channel length were electrically characterized at 200 °C to investigate their use for high-temperature applications using a Keithley 4200-SCS con-

nected to a semi-automatic Cascade 12000 probestation. A large number of transistors (>30) were measured from each wafer to generate statistical data. The electrical methods include extracting sub-threshold slope (SS), threshold voltage (V_t), charge pumping to extract interface state density ($\bar{D}_{IT}$) and near-interface state density ($\bar{N}_{NIT}$), and ultrafast pulsed *I-V* to extract transconductance (g_m) and near-interface state density. Threshold voltage was estimated by constant drain current method [21, Sec. 4.8.3], with the threshold current arbitrarily set to 50 nA for a transistor with 100/2 aspect-ratio at a drain voltage of 1 V. The presented subthreshold slope was sampled from the maximum transconductance ($\partial \log_{10}(I_d)/\partial V_{gs}$, where I_d is the drain current and V_{gs} is the gate voltage) in subthreshold region at a drain voltage of 1 V and a gate voltage step of 0.1 V.

Charge pumping measurements were performed with both triangular and trapezoidal pulse-trains in order to separate near-interface state defects and interface state defects. The pulse amplitude was 20 V, and the base was swept. The maximum current was sampled as the charge pumping current, I_{cp}. The source and drain of the transistors were short-circuited and biased at 0.1 V and the body was biased at 0 V in order to reverse-bias the gated diode. Transistors with large aspect ratios (100/2) and relatively long pulses with rise- and fall times (>1 μs) were used to reduce the influence of the geometric factor [8, 3, 5]. A high-low approach (100 Hz and 100 kHz) was used to automatically extract the amount of recombination centers. At least five transistors from each wafer were carefully measured manually with a fine frequency step to determine the accuracy of the rough automatic high-low approach.

Charge trapping was measured by ultrafast pulsed *I-V* measurement, where the sampling rate was 1 sample/μs. 100 pulses were measured and averaged to reduce noise. The drain voltage was set to 1 V and the gate voltage was pulsed from -15 V (accumulation) to +15 V (inversion). The body and source were connected to the common ground. The transconductance was estimated from the average of the rising-flank and falling-flank maximum transconductance, which in all cases occured at +15 V. Due to lack of software support, the ultrafast pulsing was only performed manually on at least five transistors from every wafer.

Results

Fig. 2a) shows the subthreshold characteristics of the transistors. The nitrided transistors show a sharp transition from off-state to on-state, as compared to the more gradual behavior of the steam-treated and dry oxidized transistors. The median subthreshold slope is the lowest for the nitrided transistors (260 mV/dec) and the highest for the steam-treated transistors (720 mV/dec). The dry oxidation transistors show the most nonlinear subthreshold slope, but exhibit a higher maximum subthreshold transconductance than the steam-treated transistors at low current (~ 1 pA). Both the nitrided and steam-treated transistors show tight distribution of values, as seen in Fig. 2b), wheras the dry oxidized transistors show a large distribution. The nitrided transistors have the lowest threshold voltage, whereas the steam-treated and dry oxidized transistors show similar median values, as see in Fig. 2c).

Examples of charge pumping characteristics are shown in Fig. 4. The base voltage sweep in Fig. 4a) shows an inverted 'U'-curve, which is characteristic of charge pumping. Large pulse amplitudes are needed to observe the charge pumping current, as seen in Fig. 4b). Near-interface traps are extracted from trapezoidal pulses from Eq. 1 [9, 10, 7],

$$\bar{N}_{NIT} = -2\kappa\frac{\partial N_{cp,Tra}}{\partial \ln(f)} \; [\mathsf{L}^{-3}], \tag{1}$$

where $N_{cp,Tra}$ is the recombined charge ($= I_{cp}/qfA_{ch}$, where q is the elementary charge, f is the frequency and A_{ch} is the channel area), $\bar{N}_{NIT}$ is the average number density of near-interface traps and κ is the attenuation coefficient given by Wentzel-Kramers-Brillouin (WKB) approximation of quantum mechanical tunneling,

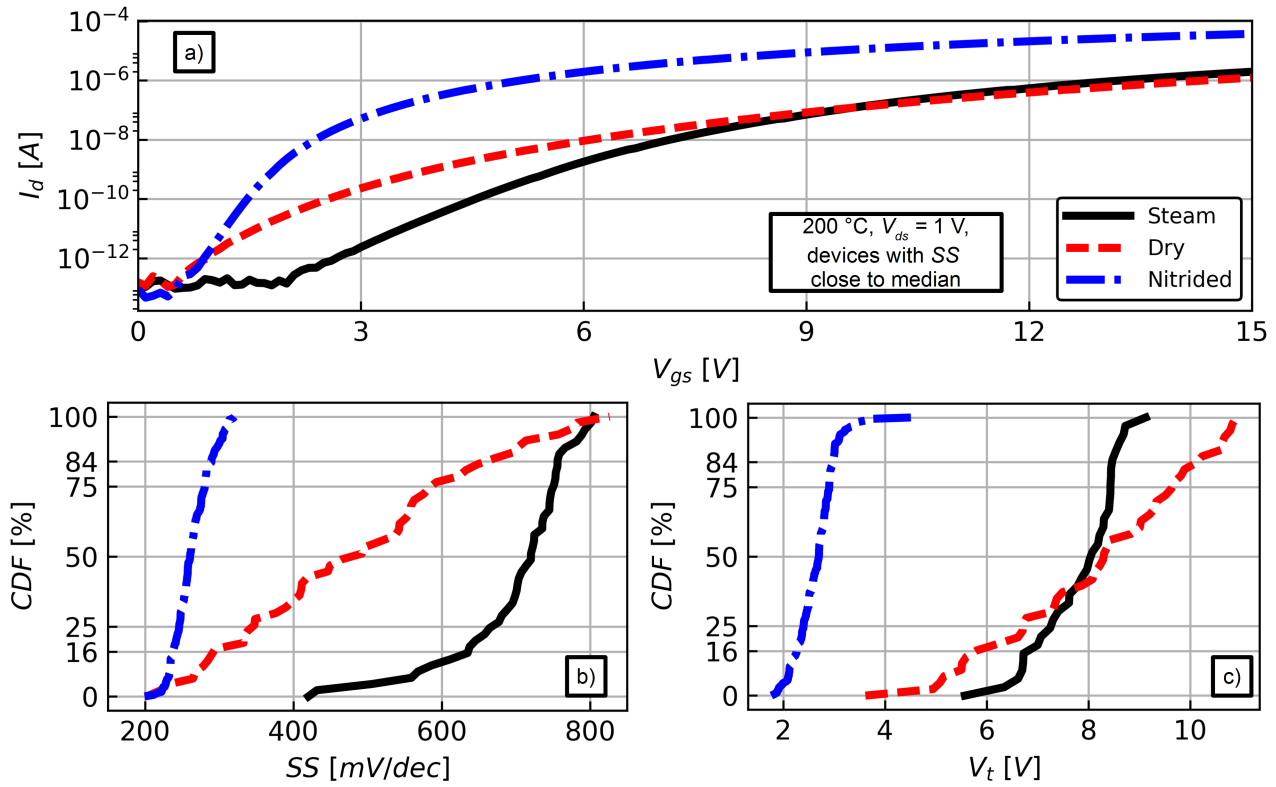$$\kappa(\Delta E) = \frac{\sqrt{2m_{ox}(\phi + \Delta E)}}{\hbar} \; [\mathsf{L}^{-1}], \tag{2}$$

Fig. 2: Subthreshold characteristics of 100 μm width, 2 μm channel length transistors at 200 °C. Steam is solid, dry is dashed and nitrided is dash-dotted. a) Subthreshold current of transistors, exhibiting SS close to median. b) Cumulative distribution function of subthreshold slope. c) Cumulative distribution function of threshold voltage values.

where m_{ox} is the electron tunneling mass in SiO$_2$ (estimated as $0.42m_0$, where m_0 is the vacuum electron mass [18]), ϕ is the electron potential barrier height across the SiO$_2$/4H-SiC (0001) interface (estimated by Afanas'ev et al. as 2.7 eV [19]), ΔE is the energy difference between electrons and the 4H-SiC (0001) conduction band edge, and $\bar{h}$ is the reduced Planck constant. The coupled Poisson-Schrödinger equation must be solved to determine the quantized eigenenergies in the triangular quantum well formed by the SiO$_2$/SiC interface. A 1D p-type MOS-capacitor, with doping, gate oxide and interface trap densities similar to the transistors, was simulated in Synopsys Sentaurus to estimate the eigenenergies and the attenuation coefficients. The result is shown in Fig. 3. The attenuation coefficients are weakly decreasing with gate voltage because the eigenenergies increase with increasing overdrive voltage. For the remainder of this paper, the attenuation coefficient will be assumed to be $\sim 5.5 \times 10^9$ m^{-1} with an uncertainty of 10 %. This uncertainty propagates to the estimation of N_{NIT}, which is assumed to have an uncertainty of 10 % from κ alone.

Eq. 1 reduces to Eq. 3 for the high-low case,

$$\bar{N}_{NIT} = -2\kappa \frac{N_{100k,Tra} - N_{100,Tra}}{\ln(f_{100k}/f_{100})} \; [\mathsf{L}^{-3}],$$ (3)

where the subscripts refer to the 100 Hz case and the 100 kHz case. Density of interface traps can be estimated from both trapezoidal and triangular pulses, or triangular pulses alone in the absence of near-interface traps, from Eq. 4 [7, 8],

$$\bar{D}_{IT} = \frac{1}{2k_B T} \cdot \left(\frac{\partial N_{cp,Tri}}{\partial \ln(f)} + \frac{\bar{N}_{NIT}}{2\kappa} \right) [\mathsf{M}^{-1}\mathsf{L}^{-4}\mathsf{T}^2],$$ (4)

where k_B is the Boltzmann constant and T is the absolute temperature (473 K). Eq. 4 reduces to Eq. 5 for the high-low case,
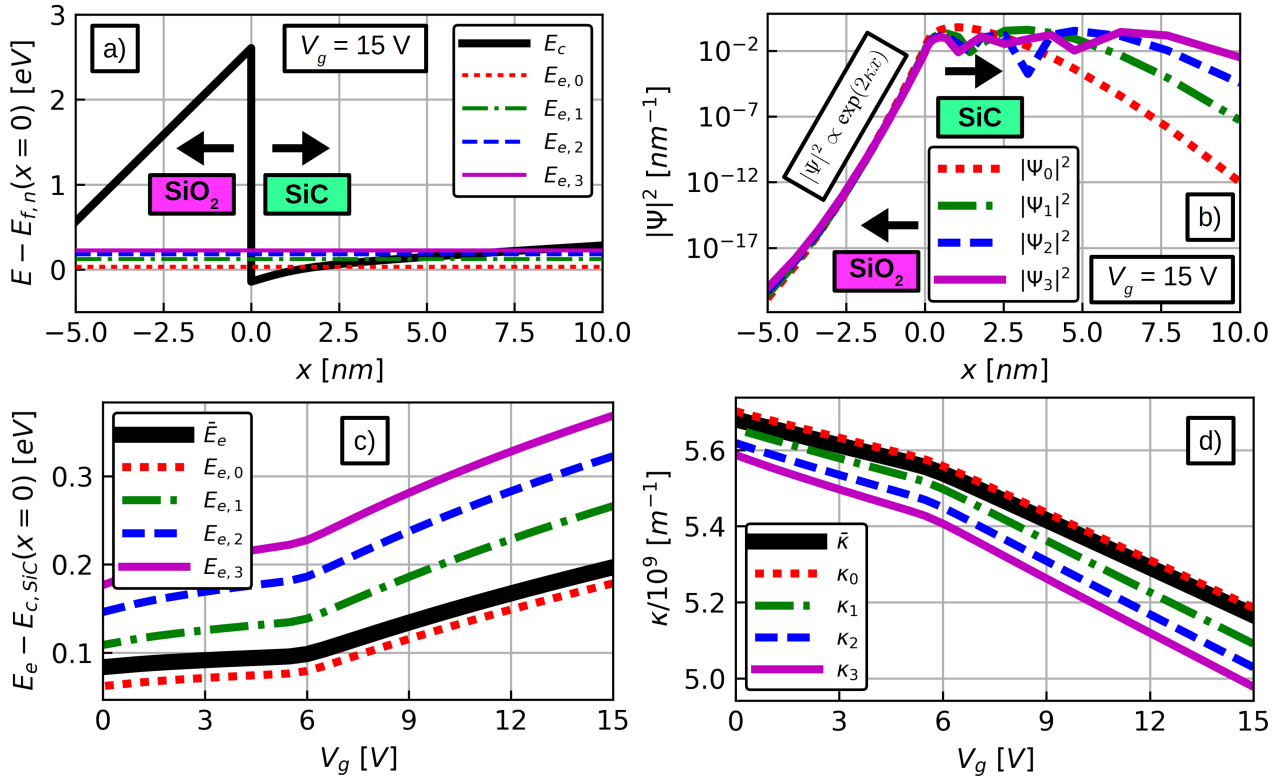
Fig. 3: Simulated quantum mechanical system. Most material properties are software default values - the potential barrier was set to ∼2.7 eV, by setting the electron affinity of SiO_2 to 0.95 eV and 4H-SiC to 3.65 eV, based on the result of Afanas'ev et al. [19]. a) Potential well and the first four eigenenergies. b) Probability density $|\Psi|^2$ vs. x. c) Eigenenergy E_e vs. applied gate voltage V_g. The threshold voltage of the system is approximately 6 V. The thick solid line is the occupation-averaged energy (weight-function is Fermi-Dirac distribution). d) Attenuation coefficient κ vs. gate voltage. The thick solid line is the occupation-averaged coefficient (weight-function is Fermi-Dirac distribution).

$$\bar{D}_{IT} = \frac{(N_{100k,Tri} - N_{100,Tri}) - (N_{100k,Tra} - N_{100,Tra})}{2k_B T \ln(f_{100k}/f_{100})} \ [\mathsf{M}^{-1}\mathsf{L}^{-4}\mathsf{T}^2] \tag{5}$$

A similar approach was presented by Matsuya et al. at ICSCRM 2019, where three-level charge pumping was used to subtract the near-interface trap contribution to extract the interface trap contribution [20].

The estimated density of interface traps and density of near-interface traps are shown in Fig. 4c) and 4d), respectively. All treatments give $\bar{D}_{IT}$ on the order of 10^{12} cm^{-2} eV^{-1}. The densities are high, as could be expected for non-optimized gate oxide processes, and other charge pumping studies give comparable results [3, 4, 5]. The nitrided transistors have the lowest amount of interface traps, although the distribution shows a considerable tail of high density values. The steam-treated transistors have the highest median density of interface traps. This is in positive correlation with the subthreshold slope, which shows the same pattern. The subthreshold slope is theoretically proportional to the capacitance division between the gate oxide capacitance and the interface state density [21, Sec. 6.3.5], and should therefore show a positive correlation. Charge pumping extracts very similar near-interface trap densities for all three treatments, as seen in Fig. 4d), and as such it is possible that the interface treatment did not significantly alter the ALD-SiO_2 film itself.

The rough measurements were complemented by careful measurements of at least five transistors from each wafer, shown in Fig. 5. The curves are fairly linear with frequency, with no unusual characteristics.
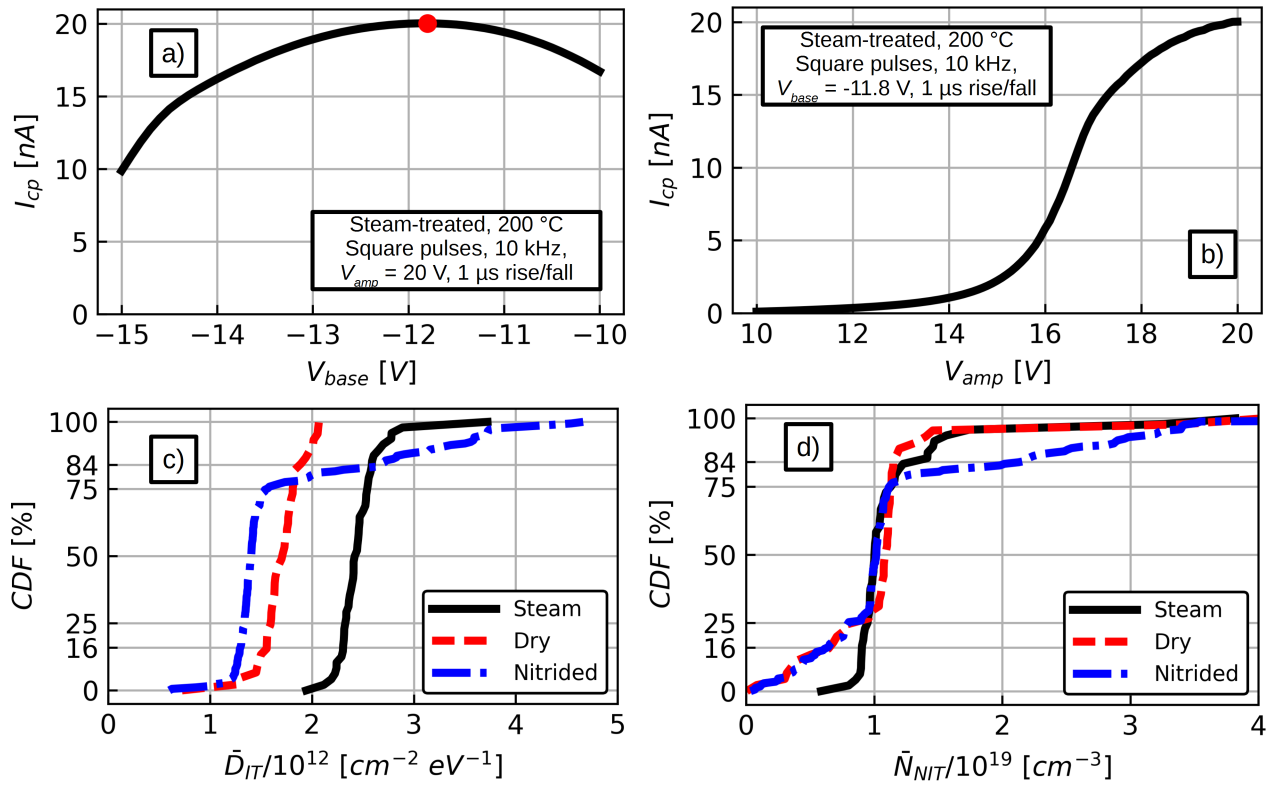
Fig. 4: Charge pumping characteristics at 200 °C. a) Example of a base voltage sweep. b) The amplitude voltage sweep corresponding to the base voltage sweep in a). c) Cumulative distribution function of density of interface traps. d) Cumulative distribution function of density of near-interface traps.

Charge pumping is primarily a quantitative method and other methods, such as spin-dependent or electrically detected magnetic resonance charge pumping [22, 23], would have to be used to determine the chemical nature of the defects. That said, charge pumping can estimate the geometric average capture cross section $\sigma_{n,p}$ from the frequency-intercept of triangular pulses in the absence of near-interface traps [8]. The extraction is highly inaccurate because of the exponential sensitivity to errors in I_{cp} and N_{cp}. The estimated geometric average capture cross section and surface recombination velocity s_r ($= \sigma_{n,p} v_{th} k_B T \bar{D}_{IT}$, where v_{th} is thermal electron velocity) are presented in table 2. It can be seen that the steam-treated capture cross section is unusually large, and suggest a Coloumb attractive trap. The dry oxidation treated interface shows an average cross section, and may be a neutral trap. The nitrided interface shows the smallest capture cross section, and may correspond to a Coloumb repulsive trap. The surface recombination velocity is smallest for the nitrided interface, not because the interface state density is low but because the capture cross section is small. A consequence of this result is that the low surface recombination velocity of nitrided interfaces give the best PN-junction passivation (lowest generation-recombination leakage current) [24], which may be found in bipolar junction transistors, PIN-diodes and MOSFETs (drain/body-junction). However, it is emphasized that the extracted capture cross sections are burdened by large uncertainty.

Table 2: Estimated geometric average capture cross section and surface recombination velocity. The extraction was performed using the fine frequency data of at least five transistors of every interface treatment.

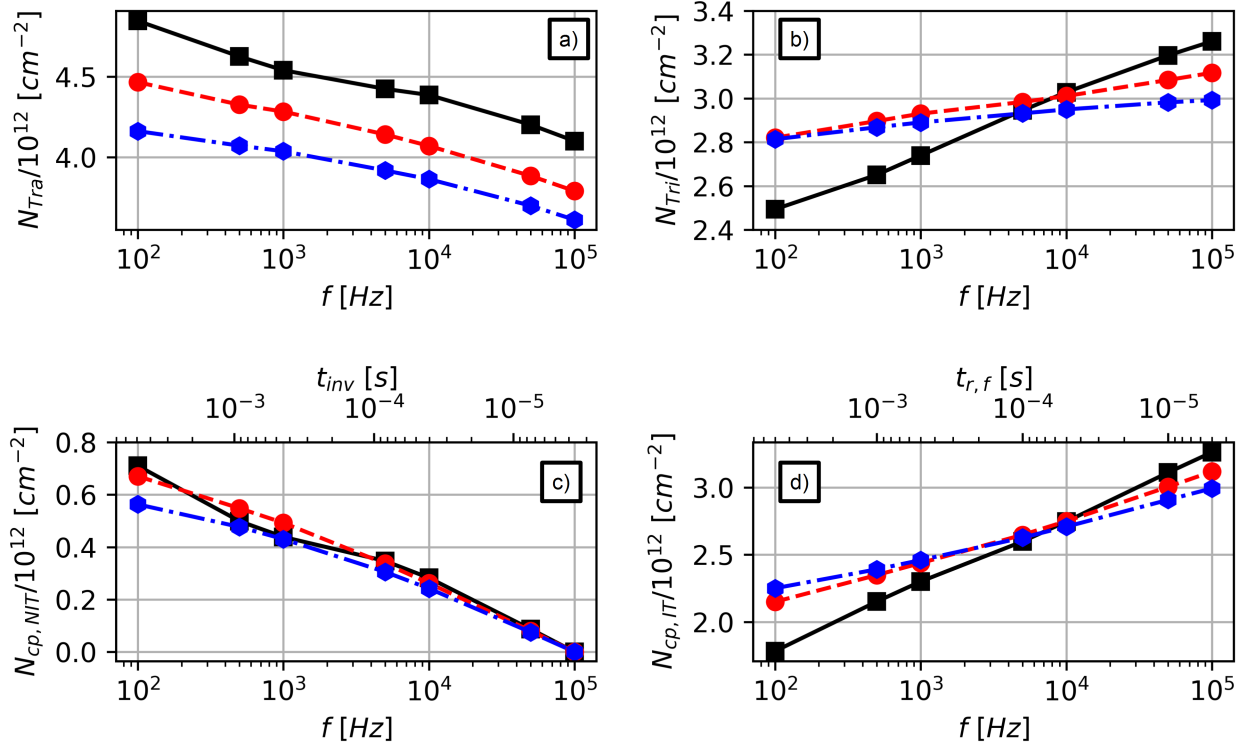| Property	Steam-treated	Dry oxidation	Nitrided
$\sigma_{n,p}$ [cm^2]	5×10^{-12}	6×10^{-15}	3×10^{-17}
s_r [cm/s]	$\sim 2 \times 10^{7}$	$\sim 2 \times 10^{4}$	6×10^{1}

Fig. 5: Fine frequency measurement charge pumping characteristics at 200 °C, averaged over at least five transistors. Solid is steam-treated, dashed is dry oxidation and dash-doted is nitridation. The markers indicate data points. a) Recombined charge versus frequency with trapezoidal pulses. The slope is negative. b) Recombined charge versus frequency with triangular pulses. The slope is weakly positive, due to the conflicting frequency behavior of interface traps and near-interface traps. c) Recombined charge due to near-interface traps versus inversion time and frequency. This is exclusively determined by the data from a). d) Recombined charge due to interface traps versus rise/fall time and frequency. This is determined from the data in a) and b).

Examples of charge trapping measurements by ultrafast pulsed *I-V* is shown in Fig. 6. The rise and fall times are relatively long to reduce transient phenomena (overshoot/ringing) and to have quasi-steady state while ramping the voltage. Once the peak voltage has been reached (100 % rise time), the current decreases with increasing time, as seen in Fig. 6a). This is due to near-interface traps being charged, which shifts the threshold voltage. This gives a hysteresis loop in the *I-V* characteristics, as seen in Fig. 6b). Plotting the time-dependent current in logarithmic scale, as in Fig. 6c), shows an approximate log-linear behavior, in agreement with previous studies [12]. The threshold voltage shift could be power-law, which would be characteristic of bias temperature instability [25], but the stress time was too short to cause permanent damage. Furthermore, the current was replicated with every applied voltage pulse and suggest that there was no permanent damage. It is assumed that the ordinary tunneling front model can be used, which is given by Eq. 6 [9, 10, 7]

$$x_m = \frac{1}{2\kappa} \ln\left(\frac{t}{\tau_0}\right) \; [\mathsf{L}], \tag{6}$$

where x_m is the tunneling depth, t is the tunneling time and τ_0 is the attempt time and its value depends on several assumptions [9, 10]. Using the tunneling front model of Eq. 6, together with several mathematical approximations [7], it can be shown that the time dependent current is given by Eq. 7

$$\frac{\partial I_d}{\partial \ln(t)} \approx -\frac{q \cdot g_m}{2\kappa C_{ox}} \bar{N}_{NIT} \; [\mathsf{I}], \tag{7}$$
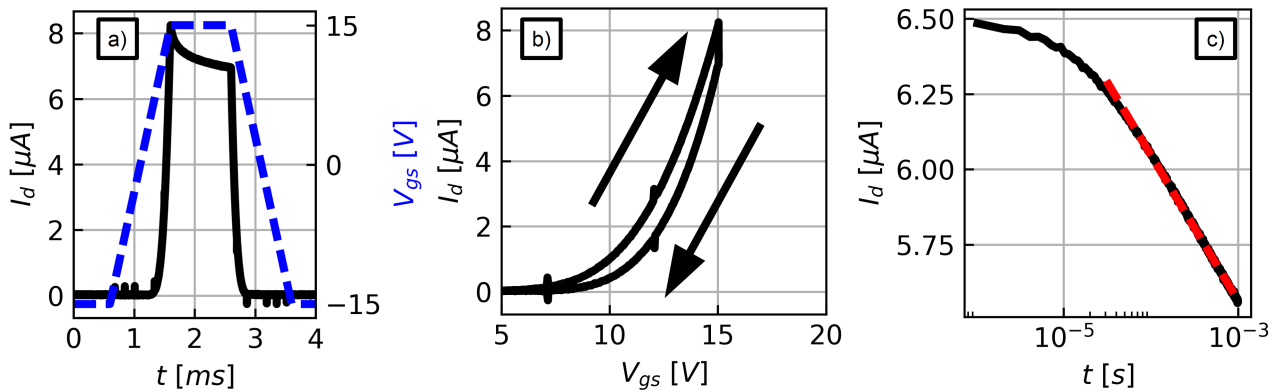
Fig. 6: Charge trapping characteristics of a steam-treated transistor at 200 °C. a) Voltage pulse and current response in linear time-domain. b) The *I-V* hysteresis loop corresponding to a). c) The current response in logarithmic time-domain (time zero set at 100 % rising edge, V_{gs} = +15 V).

where I_d is the drain-current and C_{ox} is the gate oxide capacitance (101.5 nF/cm^2 for 34 nm CET). Fitting a straight-line to the current in logarithmic time, as shown by the dashed line in Fig. 6c), gives a measure of the density of near-interface traps.

The data of all the extractions are given in table 3. The rough charge pumping estimates gave median results that were in good agreement with the fine frequency measurements, which indicates that the high-low approach may be suitable for automatic extraction of MOS interface properties. As already stated, the subthreshold slope is positively correlated with density of interface traps. The two different and independent measures of density of near-interface traps gave comparable results, with the nitrided transistors having the lowest density and the dry oxidized transistors having the highest density. Ultrafast pulsed *I-V* gives more extreme values than charge pumping, possibly because the transistor acts as an amplifier in these measurements. The transconductance, which is a measure of field-effect mobility, is not correlated with density of interface traps - the steam-treated transistors have better transconductance than the dry oxidized transistors, despite having higher density of interface traps. It should be noted that charge pumping measures deep level recombination traps, and such may not detect trap close to the conduction band, which are believed to affect the mobility [2]. The transconductance is negatively correlated with near-interface traps. The charge trapping estimation given by Eq. 7 explicitly links transconductance with near-interface traps, which could explain the correlation. However, it does not explain the correlation to the charge pumping estimate, which is to first-order independent of transconductance. A further link could be made with the threshold voltage, which is positively correlated to the density of near-interface traps. Negatively charged defects could shift the flatband voltage, causing a difference in threshold voltage. Thus, these results imply that mobility degradation by Coloumb scattering and degraded on-state current is more strongly linked to near-interface traps and negatively charged defect inside the gate oxide than to interface traps.

Conclusions

Charge pumping and ultrafast pulsed *I-V* measurement have been performed on differently passivated low-voltage n-channel SiC MOSFETs. Density of interface traps extracted by charge pumping was positively correlated with subthreshold slope, as expected from theory. The extraction of the density of near-interface traps by two independent methods, charge pumping and ultrafast pulsed *I-V* gave comparable results. The voltage normalized transconductance, a measure of mobility, did not show a correlation with the deep-level interface traps extracted by charge pumping. The transconductance did show a negative correlation with threshold voltage and near-interface trap density, suggesting that defects in the gate oxide has a more significant effect on mobility than the deep-level interface traps. Charge pumping is a suitable method for automatic extraction of defect densities, and ultrafast pulsed

Table 3: Properties measured from transistors (100 μm width, 2 μm length), estimated at 200 °C. The CET is 34 nm for all wafers. The presented values are medians (sample standard deviation) from statistical measurements (> 30 transistors per wafer). Charge pumping (CP) is indicated either by fine (F) or rough (R). g_m/V_{ds} and $\bar{N}_{NIT}$ (PIV) and the fine charge pumping (CP, F) results were averaged over five transistors from each wafer.

Property	Steam-treated	Dry oxidation	Nitrided
V_t [V]	8.0 (0.8)	8.3 (1.9)	2.7 (0.4)
SS [mV/dec]	720 (87)	480 (166)	260 (24)
$\bar{D}_{IT}/10^{12}$ (F) [cm^{-2} eV^{-1}]	2.5	1.7	1.4
$\bar{D}_{IT}/10^{12}$ (R) [cm^{-2} eV^{-1}]	2.4 (0.25)	1.7 (0.24)	1.4 (0.8)
$\bar{N}_{NIT}/10^{19}$ (CP, F) [cm^{-3}]	1.0	1.1	0.9
$\bar{N}_{NIT}/10^{19}$ (CP, R) [cm^{-3}]	1.0 (0.54)	1.1 (0.66)	0.9 (1.16)
$N_{NIT}/10^{19}$ (PIV) [cm^{-3}]	0.8	1.4	0.5
g_m/V_{ds} [μS/V]	1.7	0.75	4.85

I-V allows direct detection of the near-interface defects that degrade on-state current. Finally, it was shown that even a relatively short (10 min) nitridation step (N$_2$O) gives superior NMOS-transistors compared to steam-treatment or dry oxidation treatment at 1050 °C, with $\bar{D}_{IT}$ of $1.4{\times}10^{12}$ cm^{-2} eV^{-1}.

References

[1] M. Cabello, V. Soler, G. Rius, J. Montserrat, J. Rebollo and P. Godignon: Mater. Sci. Semicond. Process. Vol. 78 (2018), p. 22.

[2] P. Fiorenza, F. Giannazzo and F. Roccaforte: Energies Vol. 12 (2019), p. 2310.

[3] D. Okamoto, H. Yano, T. Hatayama, Y. Uraoka and T. Fuyuki: IEEE Trans. Electron Devices Vol. 55 (2008), p. 2013.

[4] L. C. Martin, D. Clark, E. P. Ramsay, A. E. Murphy, R. F. Thompson, D. A. Smith, R. A. R. Young, J. D. Cormack, N. G. Wright and A. B. Horsfall: Mater. Sci. Forum Vol. 740-742 (2013), p. 891.

[5] A. Salinaro, G. Pobegen, T. Aichinger, B. Zippelius, D. Peters, P. Friedrichs and L. Frey: IEEE Trans. Electron Devices Vol. 62 (2015), p. 155.

[6] M. Ekström, B. G. Malm and C.-M. Zetterling: IEEE Electron Device Lett. Vol. 40 (2019), p. 670.

[7] M. Ekström: *SiC CMOS and memory devices for high-temperature integrated circuits* (KTH Royal Institute of Technology, Stockholm, Sweden 2019). Available from `http://urn.kb.se/resolve?urn=urn:nbn:se:kth:diva-250276`.

[8] G. Groeseneken, H. E. Maes, N. Beltran and R. F. De Keersmaecker: IEEE Trans. Electron Devices Vol. 31 (1984), p. 42.

[9] R. E. Paulsen and M. H. White: IEEE Trans. Electron Devices Vol. 41 (1994), p. 1213.

[10] D. Bauza and G. Ghibaudo: Solid-State Electron. Vol. 39 (1996), p. 563.

[11] C. J. Scozzie and J. M. McGarrity: Mater. Sci. Forum Vol. 264-268 (1998), p. 985.

[12] A. J. Lelis and R. Green and D. B. Habersat: Mat. Sci. Semicon. Proc. Vol. 78 (2018), p. 32.

[13] Norstel AB, Linköping, Sweden. Homepage: `http://www.norstel.com/`. Accessed 2019-08-28.

[14] J. Woerle, M. Camarda, C. W. Schneider, H. Sigg, U. Grossner and J. Gobrecht: Mater. Sci. Forum Vol. 897 (2017), p. 119.

[15] M. Okamoto, M. Tanaka, T. Yatsuo and K. Fukuda: Appl. Phys. Lett. Vol. 89 (2006), p. 023502.

[16] M. Okamoto, M. Iijima, T. Yatsuo, K. Fukuda and H. Okumura: Mater. Sci. Forum Vol. 645-648 (2010), p. 995.

[17] M. Noborio, J. Suda, S. Beljakowa, M. Krieger and T. Kimoto: Phys. Status Solidi A Vol. 206 (2009), p. 2374.

[18] M. Lenzlinger and E. H. Snow: J. Applied Phys. Vol. 40 (1969), p. 278.

[19] V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl and A. Stesmans: J. Phys.: Condens. Matter Vol. 16 (2004), p. S1839

[20] Y. Matsuya, X. Zhang, D. Okamoto, N. Iwamuro and H. Yano, poster presentation at the International Conference of Silicon Carbide and Related Materials, Kyoto, Japan, (2019).

[21] D. K. Schroder: *Semiconductor Material and Device Characterization, 3rd ed.* , John Wiley & Sons, New Jersey (2006).

[22] M. Hori, T. Tsuchiya and Y. Ono: Appl. Phys. Express Vol. 10 (2017), p. 015701.

[23] M. A. Anders, P. M. Lenahan and A. J. Lelis: Mater. Sci. Forum Vol. 924 (2018), p. 469.

[24] A. S. Grove and D. J. Fitzgerald: Solid-State Electron. Vol. 9 (1966), p. 783.

[25] J. W. McPherson: *Reliability Physics and Engineering: Time-To-Failure Modeling*, Springer, New York (2010).