Wide-Range Prediction of Ultra-High Voltage SiC IGBT Static Performance Using Calibrated TCAD Model

Daniel Johannesson[1,2,a*], Keijo Jacobs[1,b], Staffan Norrga[1,c], Anders Hallén[3,d], Muhammad Nawaz[2,e] and Hans-Peter Nee[1,2,f]

[1]Division of Electric Power and Energy Systems, KTH Royal Institute of Technology, Teknikringen 33, 114 28 Stockholm, Sweden

[2]ABB Corporate Research, Forskargränd 7, 721 78 Västerås, Sweden

[3]Division of Electronics, KTH Royal Institute of Technology, Electrum 229, 166 40 Stockholm, Sweden

[a]djohann@kth.se, [b]keijoj@kth.se, [c]norrga@kth.se, [d]ahallen@kth.se, [e]muhammad.nawaz@se.abb.com, [f]hansi@kth.se

Keywords: Silicon Carbide, 4H-SiC, Ultra-High Voltage Device, SiC IGBT, TCAD simulation.

Abstract. In this paper, a technology computer-aided design (TCAD) model of a silicon carbide (SiC) insulated-gate bipolar transistor (IGBT) has been calibrated against previously reported experimental data. The calibrated TCAD model has been used to predict the static performance of theoretical SiC IGBTs with ultra-high blocking voltage capabilities in the range of 20-50 kV. The simulation results of transfer characteristics, I_C-V_{GE}, forward characteristics, I_C-V_{CE}, and blocking voltage characteristics are studied. The threshold voltage is approximately 5 V, and the forward voltage drop is ranging from $V_F = 4.2$-10.0 V at $I_C = 20$ A, using a charge carrier lifetime of $\tau_A = 20$ μs. Furthermore, the forward voltage drop impact for different process dependent parameters (i.e., carrier lifetimes, mobility/scattering and trap related defects) and junction temperature are investigated in a parametric sensitivity analysis. The wide-range simulation results may be used as an input to facilitate high power converter design and evaluation. In this case, the TCAD simulated static characteristics of SiC IGBTs is compared to silicon (Si) IGBTs in a modular multilevel converter in a general high-power application. The results indicate several benefits and lower conduction energy losses using ultra-high voltage SiC IGBTs compared to Si IGBTs.

Introduction

Traditionally in high power electronic applications, silicon (Si) based bipolar charge carrier transistors (i.e., insulated-gate bipolar transistors (IGBTs) and Thyristors) have been the main choice of semiconductor switches due to low conduction losses, high blocking voltage capability and robustness. As commercial SiC-based power semiconductor devices have begun to enter the low/medium power market in various applications [1], the devices for high power applications are predicted to enter the market when several manufacturing and packaging challenges have been resolved/improved (i.e., high quality SiC substrates, epitaxial growth, contacts and low material defect densities). It is predicted that systems using these high blocking voltage devices may offer system level benefits such as reduced number of submodule cells/devices, less complex system and reduced cooling requirement and station foot-print [2]. For initial converter comparison/evaluation, it is important to perform wide-range theoretical evaluations of high voltage SiC devices to predict the possible impact of these devices in high power applications.

In the research literature, high voltage SiC IGBTs have been experimentally demonstrated up to 27 kV [3] and numerical simulation studies have investigated the SiC IGBT characteristics in the range of 15-25 kV [4] and empirical/analytical calculation results up to 50 kV [5]. Kimoto et al. [6] stated that the forward voltage drop significantly increases for SiC devices with blocking voltage capabilities beyond 50-60 kV, due to band-to-band recombination. Today, no experimental results or finite-element simulation results for ultra-high voltage (25-50 kV) SiC IGBTs are visible in the literature. Therefore, the SiC IGBT characteristics in this blocking voltage range needs thorough

investigation to clarify the potential in different applications and justify/promote further research in this field, which is filled with several manufacturing and packaging challenges. For accurate device design and its electrical behavior predictability, a wide-range numerical simulation approach is required since several of the process dependent parameters (i.e., carrier lifetimes, mobility and trap related defects) of the manufacturing process are still uncertain at this point. A sensitivity analysis of such parameters is a suitable method to investigate future device performance.

TCAD Model Description

A general 4H-SiC IGBT punch-through structure is implemented in the Synopsys Sentaurus TCAD simulation platform according to Fig. 1. The implemented IGBT structure is based on the design of a 22 kV IGBT [7,8] (i.e., drift region thickness (doping) = 180 μm (N_D = 2×10^{14} cm^{-3}), gate oxide thickness = 500 Å, channel length (doping) = 1 μm (N_{CH} = 5×10^{17} cm^{-3}), JFET width = 5 μm, cell pitch = 9.5 μm, buffer layer thickness = 2 μm and area scale factor = 3.9×10^{6}) and is used for calibration of the TCAD model against experimental data [7,8]. A realistic SiC/SiO$_2$ trap profile [9] with increasing trap concentrations at the edges is adapted, which strongly effects the channel mobility due to scattering mechanisms at the interface (i.e., acoustic, surface roughness, coulomb scattering). Furthermore, as the SiC epitaxial growth process is still under evolvement for high voltage devices, the 4H-SiC material contains various levels of deep-level traps and crystal dislocations which limits the charge carrier mobility and lifetime. The epitaxial growth conditions define the defect type, their concentration and their physical location. As-grown n-doped SiC epitaxial-layers may attain trap concentrations in the range of 10^{12} - 10^{15} cm^{-3} depending on growth conditions [10,11]. To obtain a longer charge carrier lifetime, especially for high voltage bipolar devices, defect densities must be decreased to the order of 1×10^{12} cm^{-3} or even lower [12]. For the as-grown epitaxial layer, the measured lifetime of 1.1 μs was obtained and was greatly improved to 26 μs after the defect reduction process in the 220 μm thick epitaxial layer. Generally speaking, thicker epitaxy is more likely to have higher defect densities and thus less likely to reach ideal bulk mobility values due to impurity scattering. Therefore, these process dependent parameters are kept as model parameters and the model was calibrated by using a design of experiment (DOE) approach. Furthermore, previously calibrated 4H-SiC material related parameters were incorporated in the model [13]. The temperature dependent impact ionization coefficients derived by Zhao et al. [14] and anisotropic coefficients by Hatakeyama et al. [15] are used for breakdown voltage simulations. The incorporated physical models are summarized in Table 1.
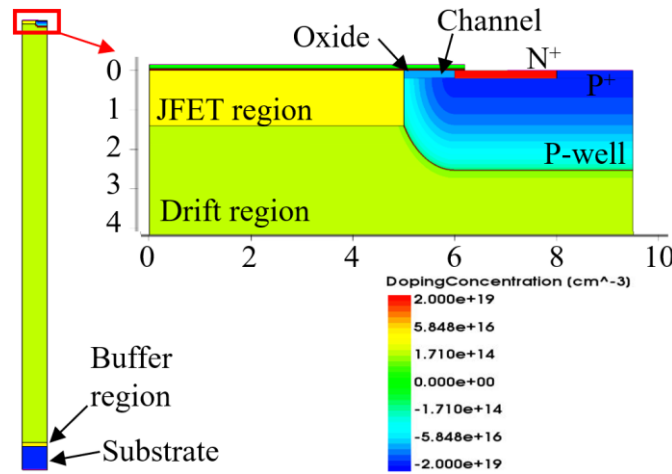

Fig. 1. 4H-SiC IGBT structure implemented in Synopsys Sentaurus TCAD.

Table 1. Models included in the simulations.

Fermi-Dirac Statistics
Incomplete Ionization
4H-SiC Bandgap Properties + Narrowing
Bulk Mobility: Anisotropic, Temperature and Doping dependent, High-Field Effects, Carrier-Carrier Scattering.
Channel Mobility: Lombardi Enormal, Phonon scattering, Coulomb Scattering.
SiC/SiO2 interface traps, Effective Oxide Charge
Recombination: Shockley-Read-Hall, Surface SRH, Auger, Radiative

The calibrated IGBT structure is scaled to blocking voltage classes in the range of 20-50 kV by modification of drift region thickness and doping concentration according to Table 2. The buffer layer

thickness and doping concentration at the bottom side of all four theoretical devices are set to 5 μm and $N_{BL} = 5\times10^{16}$ cm^{-3}.

Table 2. Simulated 20-50 kV SiC IGBT drift region parameter set and breakdown voltage results.

V_B class	Drift Region Device Parameter		Breakdown Voltage	
	Doping Concentration	Thickness	Analytical [16]	TCAD simulated
20 kV	1.75×10^{14} cm^{-3}	160 μm	21.7 kV	21.4 kV
30 kV	1.50×10^{14} cm^{-3}	260 μm	32.0 kV	31.6 kV
40 kV	1.25×10^{14} cm^{-3}	360 μm	41.0 kV	40.9 kV
50 kV	1.00×10^{14} cm^{-3}	460 μm	50.1 kV	49.9 kV

4H-SiC IGBT Simulation Results

Model Calibration. The TCAD IGBT simulation results indicate satisfactory correlation with experimental data provided from [7,8], using a set of process dependent parameters extracted from the DOE process (i.e., SiC/SiO$_2$ D$_{IT}$ = 2.1×10^{13} cm^{-2}eV^{-1}, effective oxide charge = 4.2×10^{12} cm^{-2}, $\mu_{E,MAX}$ = 700 cm^2/Vs $\mu_{H,MAX}$ = 60 cm^2/Vs, τ_A = 2.4 μs and T = 300 K). In this configuration, the MOS-channel mobility is in the range of 30 cm^2/Vs. Overall, a fair correlation between IGBT transfer characteristics (i.e., $V_{TH,EXP}$ = 2.8 V vs. $V_{TH,SIM}$ = 2.6 V) and breakdown voltage (i.e., $V_{B,EXP}$ = 22.6 kV vs. $V_{B,SIM}$ = 20.9 kV) are visible as well as for the forward characteristics (i.e., $V_{F,EXP}$ = 9.1 V vs. $V_{F,SIM}$ = 9.1 V and $R_{DIFF,EXP}$ = 79 mΩcm^2 vs. $R_{DIFF,SIM}$ = 68 mΩcm^2 at I_C = 20 A), as shown in Fig. 2a.
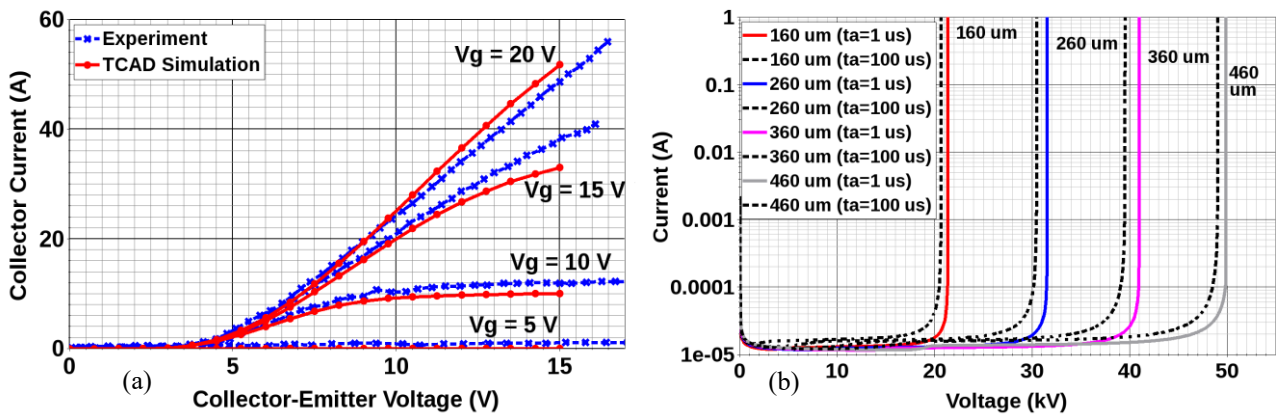

Fig. 2. a) TCAD calibration results of the forward characteristics, I_C-V_{CE}, compared to experimental data of a 22 kV SiC IGBT [7]. b) Charge-carrier lifetime-dependent breakdown voltage characteristics of the four theoretical SiC IGBTs with 20-50 kV blocking voltage capability ($\tau_{A,LOW}$ = 1 μs vs. $\tau_{A,HIGH}$ = 100 μs).

Breakdown Voltage. The breakdown voltage characteristics of the four theoretical devices (20-50 kV) are simulated with the calibrated device structure using the same physical models and parameters but with modifications stated in Table 2. For simplicity, only the active part of the device is simulated, and no junction termination edge is included. The charge-carrier lifetime-dependent breakdown voltage characteristics are presented in Fig. 2b, where $\tau_{A,LOW}$ = 1 μs and $\tau_{A,HIGH}$ = 100 μs, assuming the typical ratio of τ_E/τ_H = 5. As the charge carrier lifetime increases, the thermally generated carriers survive for a longer time and hence more active carriers are available for conduction in the drift region, which increases the leakage current. Similarly, the enhanced number of active carriers reduce the critical point of avalanche multiplication to a lower voltage level, resulting in a lower breakdown voltage capability of the devices.

Forward Characteristics. The room temperature transfer characteristics, I_C-V_{GE}, and forward characteristics, I_C-V_{CE}, of the four theoretical devices are presented in Fig. 3. Here, the threshold voltage is approximately 5 V, and the forward voltage drop is ranging from V_F = 4.2-10.0 V at I_C = 20 A, using a charge carrier lifetime of τ_A = 20 μs. The forward voltage drop increases with

blocking voltage due a to thicker, more resistive drift region of the device, as expected. Using traditional Si packaging technologies (e.g., 300 W/cm^2), the on-state current (density) handling capability ranging from 27-55 A/cm^2 and future SiC packaging technologies (e.g., 500 W/cm^2) [17] results in 39-78 A/cm^2 for the four theoretical devices.
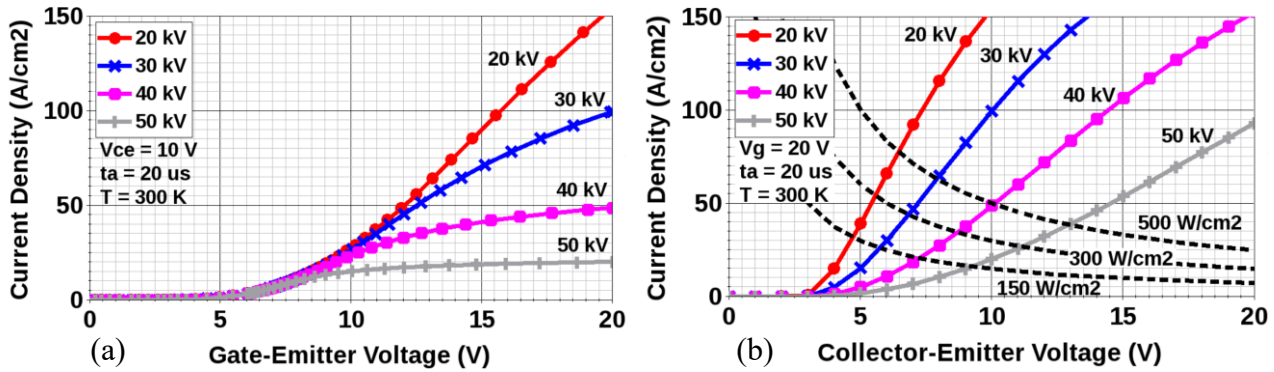

Fig. 3. TCAD simulation results of the four theoretical SiC IGBTs with 20-50 kV blocking voltage capability simulated at room temperature and $\tau_A = 20$ μs, a) transfer characteristics, I_C-V_{GE}, and b) forward characteristics, I_C-V_{CE}.

Parametric Sensitivity Analysis. The 4H-SiC manufacturing technologies are continuously evolving and reduction of defects and traps will improve the process dependent parameters. Therefore, a wide-range parametric sensitivity analysis is performed to study the impact on V_F for process dependent parameters and temperature. These results are presented in Fig. 4. The forward voltage drop decreases with increasing charge carrier lifetime, due to that more carriers in the drift region enables higher level of conductivity modulation. For low carrier lifetimes, the impact of mobility increases with blocking voltage capability. With higher carrier lifetimes, the impact of mobility is not as large and reasonable conductivity modulation is yet achieved. Material quality has a significant impact on the device characteristics and high-quality SiC material is crucial for high voltage devices. The forward voltage drop increases with temperature since bulk mobility reduces with temperature, even though more excess charge carriers are available in the drift region. Furthermore, simulations indicate that the SiC/SiO^2 interface trap density has a minor impact on the forward voltage drop (i.e., $D_{IT} = 2.1 \times 10^{13}$ cm^{-2}eV^{-1} vs. $D_{IT} = 2.1 \times 10^{12}$ cm^{-2}eV^{-1} corresponds approximately to $\Delta V_F \sim 0.1$ V for all four devices in the investigated charge carrier lifetime range). Depending on the gate process conditions, experimental D_{IT} concentrations for SiC devices in the range of $3 \times 10^{11} - 2 \times 10^{14}$ cm^{-2}eV^{-1} have been obtained [9,18].
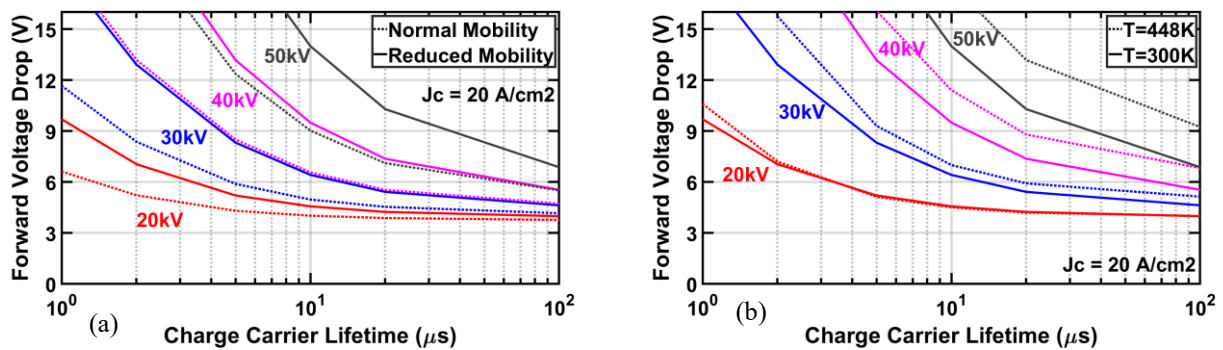

Fig. 4. Impact on SiC IGBT forward voltage drop for different charge-carrier lifetimes and a) mobility (i.e., $\mu_{E/H\_Normal} = 950/125$ cm^2/Vs vs. $\mu_{E/H\_Reduced} = 700/60$ cm^2/Vs at T = 300 K) and b) temperature (i.e., T = 300 K vs. T = 448 K with $\mu_{E/H\_Reduced} = 700/60$ cm^2/Vs).

Comparison of Conduction Losses for Si IGBTs and 4H-SiC IGBTs

The simulation output is used for initial evaluation and comparison between ultra-high voltage SiC IGBTs and Si-based device structures in high power applications. A Modular Multilevel Converter

(MMC) for a high-power application serves as a test case (e.g., system voltage $V_{DC} = 640$ kV, modulation index (M) = 1, rated power S = 1 GW). The modularity of such converters enables a good scalability. The converter cell or power electronic building blocks (PEBB) can be designed with arbitrary voltages. A PEBB with a nominal voltage of 16.8 kV employing 30 kV SiC IGBTs should therefore be compared to a solution with the same voltage rating but using series connected Si IGBTs, or a series connection of PEBBs using a single Si IGBT. Note that both Si BIGT configurations yield the same result, since only the conduction losses are considered here. As an example, a TCAD simulated 30 kV SiC IGBT with antiparallel SiC PiN diode [19] is compared to a state-of-the-art 4.5 kV Si Bi-mode Insulated Gate Transistor (BIGT) [20]. The active area of the employed power semiconductor is kept constant. In a second comparison, it is accounted for a lower active area in the ultra-high voltage SiC devices due to a bigger junction termination edge (JTE) area. The converter test case parameters and semiconductor device parameters are summarized in Table 3.

Table 3. Converter test case parameters and semiconductor device parameters.

Simulation case	Si		SiC	
	Semiconductor			
	Si BIGT [20]		**SiC IGBT**	**SiC PiN Diode [19]**
Blocking voltage (V_B)	4.5 kV		30 kV	30 kV
Nominal operating voltage (V_{NOM})	2.8 kV		16.8 kV	16.8 kV
Active area (A_A)	49 mm^2		100 mm^2	100 mm^2
JTE length	0.8 mm [21]		1.5 mm [3]	1.5 mm [3]
Total area (A_{TOT})	74 mm^2		169 mm^2	169 mm^2
Carrier lifetime (τ_A)	-		20 μs	21.6 μs
	Converter ($V_{DC} = 640$ kV, M = 1, S = 1 GW)			
	Single switch PEBB	**Series conn. within PEBB**	**Single switch PEBB**	
Semiconductor device	Si BIGT	Si BIGT	SiC IGBT + SiC PiN	
PEBB voltage (V_{PEBB})	2.8 kV	16.8 kV	16.8 kV	
Number of PEBBs per arm (N_{PEBB})	229	39	39	
Total number of switches (N_{SW})	5496	5496	936	
MMC cell topology	Full bridge	Full bridge	Full bridge	

A forward characteristics comparison (i.e. on-state voltage drop and current capability) between Si BIGT and SiC IGBT is presented in Fig 5a, where the voltage drop is normalized by the rated blocking voltage. Two cases are presented, the first case with equal active area ($A_A = A_{TOT}$) and the second case with equal total area including the required JTE for each device ($A_A = A_{TOT}-A_{JTE}$). In both cases, the ultra-high voltage SiC device indicates lower normalized voltage drop than Si BIGT counterparts.

Furthermore, the normalized semiconductor conduction losses of the high-power converter conducting active power employing Si BIGTs or SiC IGBTs are visualized in Fig. 5b. Note that the device area for both technologies is scaled to fit the RMS current appearing in the converter. The comparison indicates that the TCAD simulated 30 kV SiC IGBTs are conduction loss competitive with a series connection of state-of-the-art Si BIGT devices; even with a reduced active area due to larger JTE, where a conduction loss reduction of approximately 30 % can be achieved. Together with a reduction of system complexity, control hardware, cables, and fibers (due to a lower amount of PEBBs), this presents a promising alternative to existing high-power converters with high-voltage Si devices.
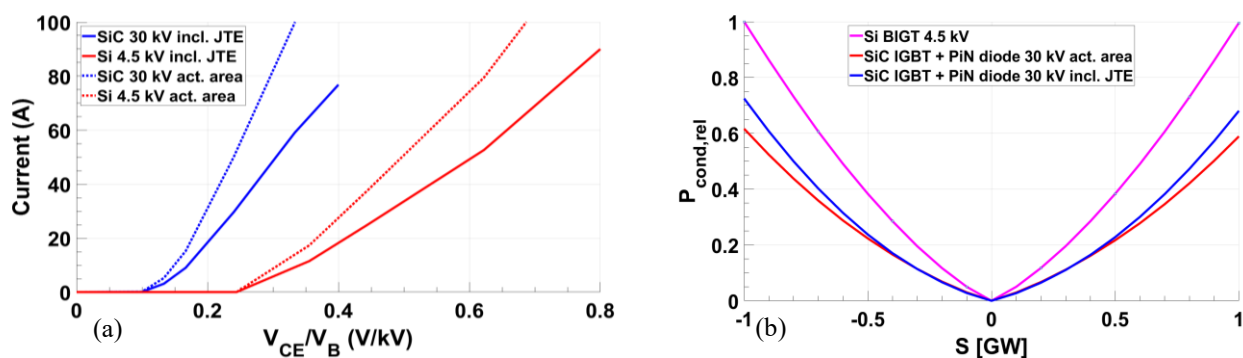
Fig. 5. a) Comparison of conduction capability normalized by blocking voltage with data from 30 kV SiC IGBT TCAD simulation and [20] for equal active area ($A_{A,Si} = A_{A,SiC} = A_{TOT} = 1$ cm^2), and equal total area including JTE ($A_A = A_{TOT}-A_{JTE}$, $A_{A,Si} = 0.706$ cm^2, $A_{A,SiC} = 0.49$ cm^2). b) Conduction loss comparison between Si BIGT and TCAD simulated SiC IGBT in a general high-power system. The losses are normalized to the Si BIGT implementation.

Summary

A 4H-SiC IGBT TCAD model has been calibrated against experimental data and has been used to widely investigate static performance of high voltage SiC IGBTs (20-50 kV). The impact of various process dependent parameters and temperature has been studied. A comparison of conduction energy losses between SiC and Si based converter cells has been evaluated for their potential use in high-power application systems. The calculation indicates that a conduction loss energy reduction of 30 % may be achieved by using 30 kV SiC IGBTs. Furthermore, the wide range simulation data may serve as input to future converter evaluation studies in various high-power applications.

Acknowledgment

References

[1]　X. She et al., IEEE Trans. Ind. Electron., vol. 64, no. 10, p. 8193–8205, Oct. 2017.
[2]　K. Jacobs et al., in Proc. European Conf. Power Electron. and Appl. (EPE'17), p. 1-10, 2017.
[3]　E. van Brunt, et al., Materials Science Forum, Vols. 821-823, pp. 847-850, 2015.
[4]　S. Chowdhury et al., Int. Symp. Power Semicond. Devices & ICs, Jun 12-16, 2016, pp. 75-78.
[5]　D. Johannesson et al., in Proc. Work. Wide Bandgap Power Devices Appl., 2016, pp. 253-258.
[6]　T. Kimoto et al., Energies, 9, 908, 2016.
[7]　M. Hinojosa, et al., Materials Science Forum, Vols. 858, pp. 949-953, 2016.
[8]　E. V. Brunt et al., Int. Symp. Power Semicond. Devices & ICs, Jun 15-19, 2014, pp. 358-361.
[9]　A. Pérez-Tomás et al., Microelectronic Engineering 83, pp. 440–445, 2006.
[10]　T. Kimoto et al., Materials Science in Semiconductor Processing, Vol. 78, pp. 43-56, 2018.
[11]　L. Gelczuk et al., Solid-State Electronics, Vol. 94, pp. 56-60, 2014.
[12]　T. Kimoto 2015 Jpn. J. Appl. Phys. 54 040103
[13]　D. Johannesson et al., Materials Science Forum, Vols. 963, pp. 670-673, 2019.
[14]　Y. Zhao et al., Japanese Journal of Applied Physics 58, 018001, 2019.
[15]　T. Hatakeyama et al., Phys. Lett., vol. 85, pp. 1380–1382, 2004.
[16]　B. J. Baliga, "Advanced High Voltage Power Device Concepts," Springer Media, LLC 2011.
[17]　L. Boteler et al., IEEE Int. Work. on Integrated Power Packaging (IWIPP), 2017, pp. 1-5.
[18]　P. Fiorenza et al., Energies, 12, 2310, 2019.
[19]　N. Kaji et al., IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 374–381, Feb. 2015.
[20]　F. Dugal et al., in Proc. PCIM'17, Nuremberg, Germany, 2017, pp. 1-5.
[21]　H. Jiang et al., Int. Symp. Power Semicond. Devices & ICs, Bruges, 2012, pp. 173-176.