

Review of Sublimation Growth of SiC Bulk Crystals

P.J. Wellmann^{1,a*}, M. Arzig^{1,b}, J. Ihle^{1,c}, M. Kollmuß^{1,d}, J. Steiner^{1,e},
M. Mauceri^{2,f}, D. Crippa^{2,g}, F. LaVia^{3,h}, Salamon^{4,i}, N. Uhlmann^{4,j}, M. Roder^{5,k},
A. Danilewsky^{5,l}, B.D. Nguyen^{6,m}, S. Sandfeld^{7,n}

¹Crystal Growth Lab, Materials Department 6 (i-meet), FAU Erlangen-Nürnberg, Germany

²LPE S.P.A., 95121 Catania and 20021 Baranzate (MI), Italy

³CNR-IMM, Sezione di Catania, Catania 95121, Italy

⁴Development Center for X-Ray Technology (EZRT), Flugplatzstr. 75, D-90768 Fürth, Germany

⁵Crystallography, University of Freiburg, Hermann-Herder-Str. 5, D-79104 Freiburg, Germany

⁶Institute for Advanced Simulations -- Materials Data Science and Informatics (IAS-9),
Forschungszentrum Jülich GmbH, 52425 Jülich, Germany

⁷Chair of Materials Data Science and Materials Informatics, Faculty 5 -- Georesources and
Materials Engineering, RWTH Aachen University, 52056 Aachen, Germany

^apeter.wellmann@fau.de, ^bmatthias.arzig@fau.de, ^cjonas.ihle@fau.de, ^dmanuel.kollmuss@fau.de,

^ejohannes.steiner@fau.de, ^fMarco.Mauceri@lpe-epi.com, ^gdanilo.crippa@lpe-epi.com,

^hFrancesco.LaVia@imm.cnr.it, ⁱmichael.salamon@iis.fraunhofer.de,

^jnorman.uhlmann@iis.fraunhofer.de, ^kmelissa.roder@krist.uni-freiburg.de,

^la.danilewsky@krist.uni-freiburg.de, ^mbi.nguyen@fz-juelich.de, ⁿs.sandfeld@fz-juelich.de

*corresponding author

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Abstract. The review on bulk growth of SiC includes a basic overview on the widely used physical vapor transport method for processing of 4H-SiC boules as well as the discussion of three current research topics: (a) Sublimation bulk growth of large area, freestanding cubic SiC, (b) in-situ Visualization of the PVT Process using 2D and 3D X-ray based imaging and (c) prediction of dislocation formation and motion in SiC using a continuum model of dislocation dynamics (CDD).

Introduction

In recent years SiC has become the key player among semiconductor materials for power electronic applications. Since the first reports of physical vapor transport (PVT) growth of SiC by Tairov and Tsvetkov [1] in 1978 and Ziegler [2] in 1983, a remarkable progress of SiC based crystal growth, epitaxy and device processing can be observed. For a review on the complete topic of SiC fundamentals, technology and application it is referred to [3]; for a comprehensive review on the bulk growth process of SiC please see [4]. The success of SiC is related to its superior materials properties like extremely high electrical break down field and large heat conductivity compared to the standard silicon counterpart and to a meanwhile very well-developed processing technology exhibiting a comparably high yield. The extraordinary physical properties also include obstacles related to the strong chemical bonds and the complex phase diagram of the material that cause challenges in the growth process. Today's technology maturity is the major reason why SiC outperforms other wide bandgap materials like GaN, β -Ga₂O₃, AlN and Diamond, respectively, for application in power electronics [5]. A key issue for the success of SiC compared to the mentioned wide bandgap counterparts is related to the availability of SiC wafers of large diameter (150mm = standard, 200 mm = demonstrated) and high crystalline quality. Beside the power electronic application, there is a rapidly increasing interest to use SiC in novel photonic applications [6-11]. In all cases, high quality SiC wafers exhibiting a low structural defect density are of particular interest. In addition, low unintentional doping emerges as an important property for novel photonics.

The review paper comprises (i) an introduction to the high temperature crystal growth process of SiC including a brief historical overview [4] as well as (ii-iv) a report on three hot research topics on bulk growth of SiC currently studied in the crystal growth lab at FAU. (ii) In the first focal area, challenges and recent progress of sublimation bulk growth of cubic SiC will be reviewed. (iii) 3D in-situ visualization of the growth process by X-ray computed tomography has been applied to investigate the shape of the crystal growth interface as well as the morphology of the consumed SiC powder source. (iv) The third study is attributed to the analysis of the distribution of the dislocation density in 4H-SiC as it evolves during the growth process and the cooling down of the SiC boule.

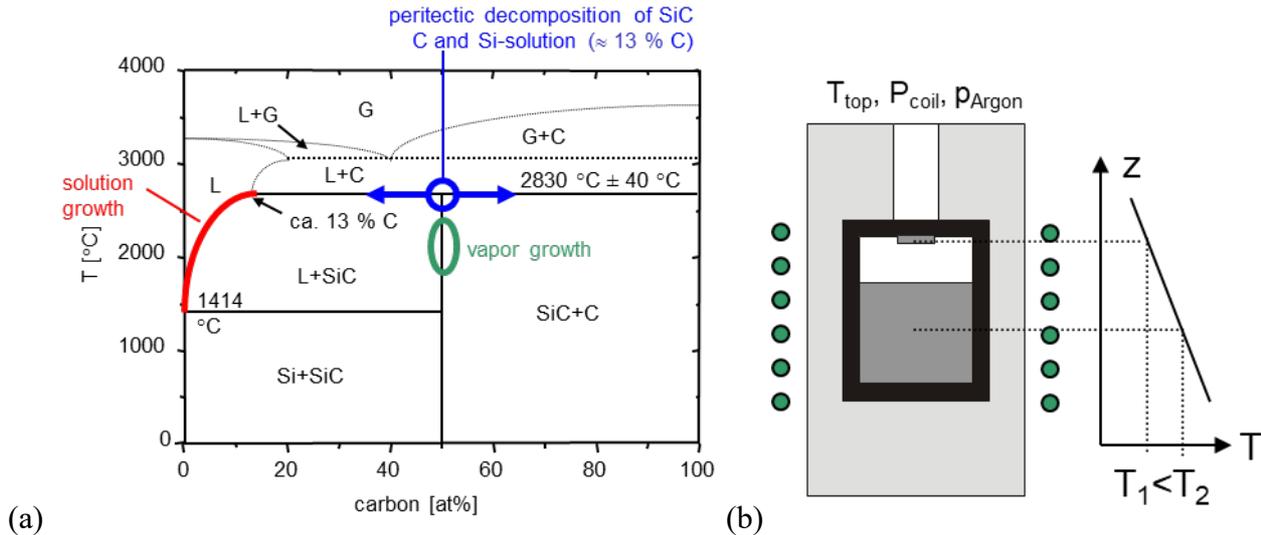


Fig. 1 (a) Phase diagram of SiC. (b) Scheme of the basic PVT process.

Bulk Growth Process of SiC

Since the early days of bulk growth of SiC using the physical vapor transport (PVT) [1, 2] the basic process has hardly changed, however, the technologic implementation went through numerous progress steps which become necessary because of the increasing requirements to reach a higher crystalline quality and a larger crystal size. The process temperature which usually lies above 2000°C demands high temperature stable hot zone components. Carbon materials play a key role for the construction of the growth crucible out of isostatic graphite as well as the surrounding high temperature insulation out of porous graphite or fibrous graphite felt. As crucible material, also bulk TaC or graphite coated with TaC are used. Compared to graphite, TaC shows a greater chemical resistance against chemical reactions with the SiC-related gas species Si and Si₂C. Due to a much lower emissivity of TaC compared to graphite, also an impact on the temperature field distribution inside the growth cell is observed. For the semiconductor application of SiC, purification of graphite crucible parts in a high temperature halide-based cleaning procedure appears inevitable.

Also related to purity, special emphasis must be put on the proper choice of the SiC source material which is often a SiC powder exhibiting a grain size between approximately 100 μm up to a few millimeters. Purity levels should lie in the 6N range if n-type conducting materials like 4H-SiC doped with nitrogen is desired. In the case of semi-insulating SiC for the application in high frequency devices as well as substrates for GaN base electronic switching devices, ever higher demands in the 7N or even 8N range are beneficial. A new demand on high purity SiC comes along with the novel photonic applications of SiC in the field of quantum information. In principle, low background doping levels as low as 10¹³cm⁻³ may be reached using advanced chemical vapor deposition (CVD) of epitaxial layers. Nevertheless, to exclude contamination of the CVD growth cell due to some decomposition of the SiC seeding material, also the SiC wafer applied during homoepitaxial growth needs to fulfil high standards related to low background doping.

The choice of the PVT method as main bulk growth method today is related to the phase diagram of SiC (see Fig.1a) which exhibits a peritectic decomposition of SiC at ca. 2830 °C into carbon and a Si-rich Si-C solution. It should be noted that the thermodynamical data of the phase diagram of SiC

presented in literature still vary. While the decomposition temperature around 2800°C is widely accepted (also unpublished work of the authors confirm this value), the maximum solubility of C in a Si-melt, as well as the precise shape of liquidus line (see curve in Fig. 1a) partially differ. The great technologic advance of the PVT growth method over solution growth of SiC using a Czochralski [12] or Vertical Bridgman [13] configuration could be related to an earlier availability of PVT growth process technology, rather than to large fundamental thermodynamic considerations. It is noteworthy that SiC crystals prepared by solution growth often exhibit a higher crystalline perfection than in the case of PVT growth. The latter is usually attributed to the smaller deviation from thermodynamic equilibrium in the case of solution growth compared to vapor growth. Nevertheless, in terms of crystal size and yield of SiC wafer production, the PVT method outperforms solution growth by far.

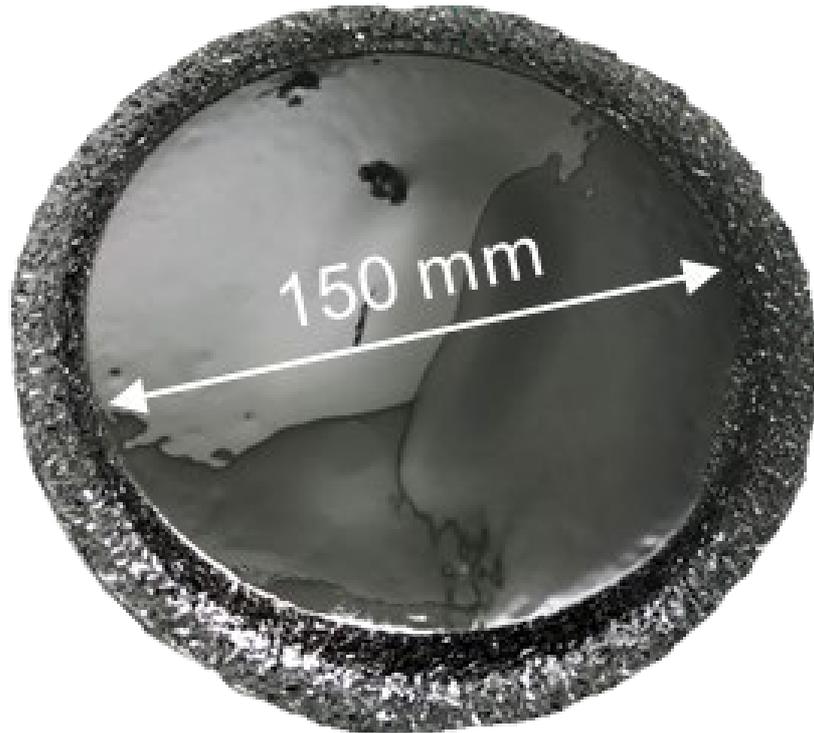


Fig. 2 Image of a state-of-the-art 150 mm 4H-SiC grown in the crystal growth lab of FAU using a SICma 600 PVT machine (PVA-CGS, Germany).

In the basic PVT method, a SiC source material and a SiC seed are placed into a crucible which exhibits a pronounced axial temperature gradient to establish a SiC-based mass transport from the source to the seed. In Fig. 1b the axial temperature gradient is set through a cooling channel which interrupts the heat insulation of the crucible on the top. Major efforts have been put into tailoring and design of the proper temperature distribution inside the growth cell. For this, computer simulation of the thermal field and to a certain extent also of the SiC-based mass transport have become standard tools. The demands are twofold. Firstly, the radial temperature gradient should be minimized as much as possible to reduce thermally induced stress of the growing SiC boule while keeping a medium axial temperature maintaining a constant mass transport from the SiC source to the SiC growth interface. The minimization of stress in the growing SiC boule has become the major challenge for the preparation of large crystal diameters of 150 mm and 200 mm, respectively. Note: Beside thermally induces stress, also doping level variations are known to induce strain in the crystal lattice. Secondly, the gas phase composed mainly out of Si, Si₂C and SiC₂ and the transport paths through the growth cell need to be set properly. Thermodynamically, Si-vapor dominates the gas phase with the highest partial pressure. Chemical reactions with the inner side walls of the growth cell need to be diminished as much as possible. The application of proper graphite materials becomes a key element in the growth cell design. As an option, coating of the graphite surfaces with TaC or even the application of a part or the complete crucible set out of TaC has been reported in literature. Valid

temperature field calculations demand the precise knowledge of the thermal properties of the growth cell components, like the crucible, insulation, SiC source materials and SiC boule.

Initially, the reduction of the defect density during SiC crystal growth was much focused on the reduction of the density of micropipes, which are known to be screw dislocations with a burgers vector exceeding the value of $3c$. Usually, micropipes arise at growth process instabilities related to unintentional polytype switches, at secondary phase inclusion (i.e. carbon inclusions or Si droplets) and at cavities in the crystal lattice [14]. Today, micropipe densities well below 1 cm^{-2} are standard in n-type 4H-SiC wafers. Major research and development efforts target the further reduction of the dislocation density, with basal plane and threading screw dislocations being the most severe line defect for electronic devices. Section “prediction of dislocation formation and motion in SiC” addresses the modeling of the evolution of the dislocation density during PVT bulk growth.

A high yield during production of SiC boules demands a high polytype stability of the growth process. In the case of 4H-SiC, a high C/Si-ratio in the gas phase (or to say a less Si rich gas phase in the growth regime dominated by a high Si partial pressure) and nitrogen doping stabilize the process. From the perspective of fundamental materials science, growth kinetics aspects, i.e. the height and width of the propagating surface steps (either dominated by continuous step flow or by spiral growth), play the key role, rather than thermodynamic energy differences between various SiC polytypes [15]. However, the cubic polytype, i.e. 3C-SiC, exhibits many obstacles related to the fabrication of high quality SiC crystals for application in mid power electronic switches and novel photonic devices. In the next section “progress of bulk growth of 3C-SiC” the newest achievements and ongoing limitations will be presented.

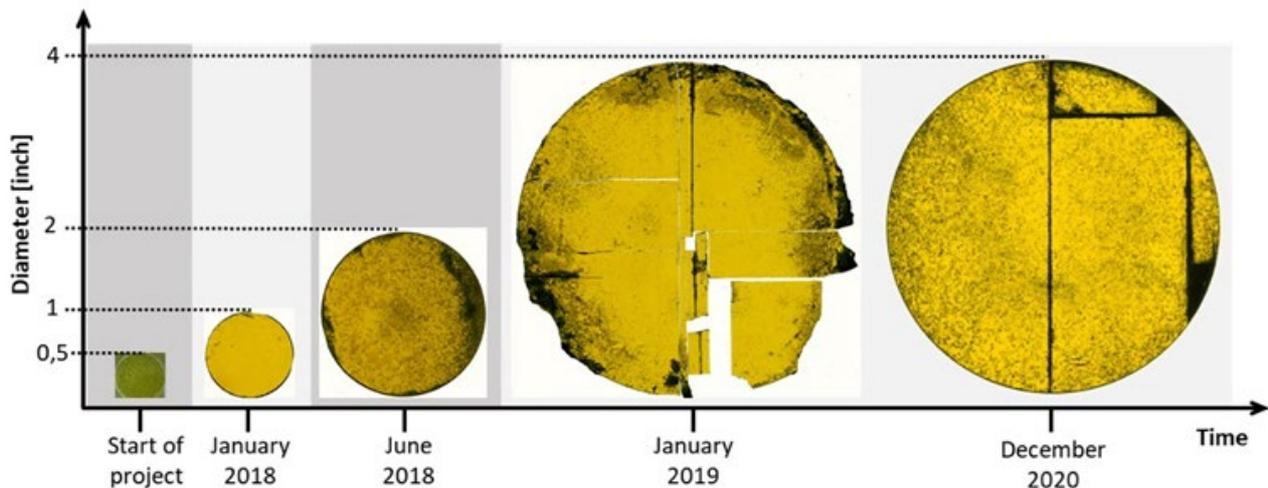


Fig. 3 Evolution of the diameter of free standing 3C-SiC by sublimation growth on CVD 3C-SiC-on-Si seeds.

Progress of Bulk Growth of 3C-SiC

Contrary to 4H-SiC where homoepitaxial seeding is standard, 3C-SiC bulk growth has been mainly carried out using heteroepitaxial seeding either on (0001) oriented 6H-SiC and 4H-SiC or on (111) and (100) oriented thin epitaxial 3C-SiC-on-Si films. Already the first 3C-SiC bulk growth attempts by [16, 17] followed this procedure. Later, several investigations focused on the investigation of proper process parameters that enable stable growth of 3C-SiC by sublimation growth [16-28]. Today, it is generally accepted that a silicon rich gas phase, a high supersaturation at the growth interface and a processing temperature $T < 2000 \text{ }^\circ\text{C}$ are important to crystallize the cubic polytype. Nucleation of 3C-SiC on hexagonal (0001) oriented SiC is usually accompanied by formation of double positioning grain boundaries (DPBs). Note: DPBs do not occur during nucleation of 3C-SiC on (100) oriented Si. Other structural defects which have been observed after heteroepitaxial nucleation of 3C-SiC are stacking faults (SFs) and antiphase boundaries (APBs). It has been recently demonstrated that SFs and APBs can be significantly reduced or even diminished during 3C-SiC nucleation on undulant, off-axis (100) oriented Si substrates [29]. Motivated by this preliminary work, a new effort was started to prepare large area bulk cubic SiC wafers. Thin (thickness = 12 to $50 \text{ }\mu\text{m}$) CVD grown 3C-SiC-on-

Si layers were removed from the Si-substrates and transferred to high-temperature stable poly-SiC wafer carriers. These new seed stacks were placed into a CS-PVT setup which can easily provide the large axial temperature gradients necessary to reach the anticipated high supersaturation for stable 3C-SiC growth (for process details it is referred to [30-33] and chapter 5 in [3]). Fig. 3 depicts the quick evolution of diameter increase of the free standing 3C-SiC wafer materials with a thickness of up to 1mm which is related to the availability of larger seeding materials as well as to the up-scaling of CS-PVT growth cell. A further increase of the thickness to values of a few and several millimetres failed so far because of the presence of the so-called protrusion defects. Protrusions start from inverse pyramidal defects at the initial Si-SiC seeding interface and enlarge during growth due to their surrounding SF structure (Fig. 4).



Fig. 4 Cross sectional view of a 3 mm thick free standing 3C-SiC boule. Even in the case of a low density, the expansion of the protrusion defects during growth (bottom = early growth stage, top = final crystal surface) leads to an almost complete spreading of the distorted crystal at the crystal end.

3C-SiC areas not affected by the expansion of protrusions, however, exhibit a perfect crystalline structure and prove the stable growth condition in the newly developed CS-PVT setup. For special cases of (100) 3C-SiC seeding layers with a 4° off-axis declination towards [100] a significant overgrowth of protrusions was observed by Schöler et al. [34]. Nevertheless, as a long-term goal, the presence of protrusions needs to be completely diminished in order to develop a real bulk growth process with boule thicknesses beyond 10 mm, respectively. To review the current status: While 50 mm freestanding 3C-SiC wafers with high crystalline quality are fabricated on a regular base, the preparation of bulk 3C-SiC with a diameter of 100 mm and 150 mm suffers from unintentional cracking of the thin seeding layers. A complete description of the current status of large area growth of free standing 3C-SiC wafers using the CS-PVT method is described in chapter 5 in [3].

2D/3D In-Situ Visualization of the PVT Process

In-situ visualization methods of the growth process play a key role to develop a bulk growth process as well as to carry out production processing with high reproducibility. Temperature measurements at the top and at the bottom of the growth cell using optical pyrometers may be called standard. Highly advanced 2D and 3D X-ray based in-situ visualization of the PVT process bridges between production and basic process development. While 2D X-ray visualization [35] could be applied to monitor the progress of the SiC boule production, the technical efforts for 3D X-ray CT [36] pay off only for special R&D problems under investigation. Advantages of the 3D X-ray CT in-situ visualization are the ability to precisely determine the evolution of the size and position of the (000-1) facet of the 4H-SiC crystal growth interface [37] (see right image in Fig. 5). In addition, the evolution of the SiC source material may be determined with high precision. In particular, the anisotropy of the step-by-step densified feedstock can be acquired. In conjunction with a newly developed physical model of the heat transfer in anisotropic porous media, the real temperature distribution inside the growth cell has been determined [38]. A correlation of the curvature of the growth interface and predominant step flow mechanism was presented in [39].

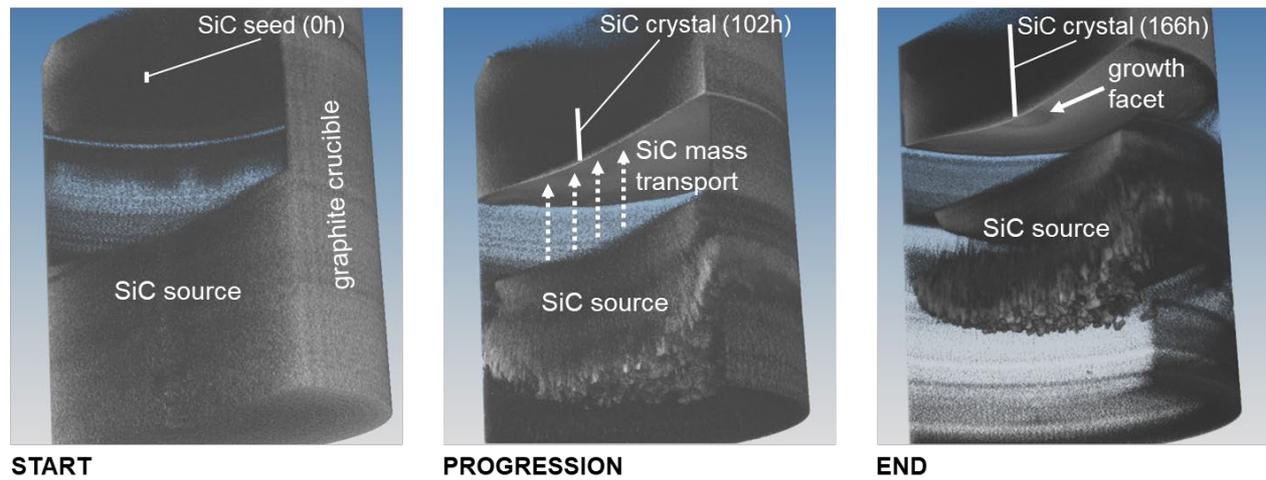


Fig. 5 Series of in-situ 3D computed tomography views inside the PVT growth cell at $T > 2000^\circ\text{C}$. The imaging allows to track the evolution of the crystal growth interface including the shape, size and position of the faceted growth area. In addition, a high-resolution visualization of the SiC source material enables the precise determination of the temperature field and related growth conditions inside the growth cell.

Prediction of dislocation formation and motion in SiC

Dislocations are known to be one of the major lifetime-limiting defects in semiconductor materials. In SiC, the micropipe, a hollow core screw dislocation of pure or mixed type exhibiting a Burgers $b \geq 3c$, is known to cause an immediate device failure [40]. Under bipolar device operation basal plane dislocations appeared to act as source for stacking fault generation and propagation in SiC which causes early device failure [41]. Screw dislocations increase the reverse-blocking current in SiC Schottky barrier diodes and alter the performance of SiC MOSFET devices. Even threading edge dislocation are detrimental for device operation if a line up is observed. In general, dislocation formation is observed in the presence of thermally or mechanically induced stress during crystal growth, including the final cooling to room temperature.

From a characterization point of view, dislocation may be visualized using KOH defect etching of SiC wafers (see Fig. 6e)[42, 43] and in a more advanced way by X-ray topography methods [44]. In recent years, using white beam X-ray topography a deep insight in dislocation generation, propagation as well as interaction has been gained (see [45, 46] and chapter 7 in [3]).

To relate the formation of dislocations during crystal growth with the thermal boundary conditions, the thermoelastic strain in the growing SiC crystal as well as the critical shear stress have been considered [47, 48]. For a deeper analysis the so called Alexander-Haasen (AH) model [49] may be applied which uses a continuum model for predicting the evolution of dislocation density in semiconductors through a local dislocation multiplication law. The adaption of the AH model to the complex crystal structure of hexagonal SiC has been carried out by [50]. Recently, Nguyen and Sandfeld ([51] and chapter 8 in [3]) pointed out the limitations of the AH model concerning the lack of motion of dislocations and introduced a more general continuum model of dislocation dynamics (CDD) which explicitly considers dislocation fluxes. Using the AH-GROMA approach for CDD-modeling, the authors show that the consideration of motion of dislocation can have significant impact on the evolution and final distribution of dislocation density. As a result, the calculated evolution of the dislocation density in the growing SiC crystals and the related local plasticity differ significantly between the AH- and the CDD-model. In the AH-model a pile up of dislocation density and plasticity in the area of the maximum shear stress inside the SiC boule is predicted. Due to dislocation motion, however, in the CDD-model dislocations migrate into crystal zones of low shear stress (like into the center of the SiC boule) resulting in a completely different dislocation and plasticity distribution which matches better with experimental data than the AH-model. Fig. 6 shows a comparison of the AH-model and the CDD-model with experimental data. The final dislocation density in the real SiC boule exhibits a maximum in the central area of the SiC boule which is also well predicted in the

more advanced CDD. The AH-model however fails to explain the experimental findings due to the lack of implementation of dislocation motion.

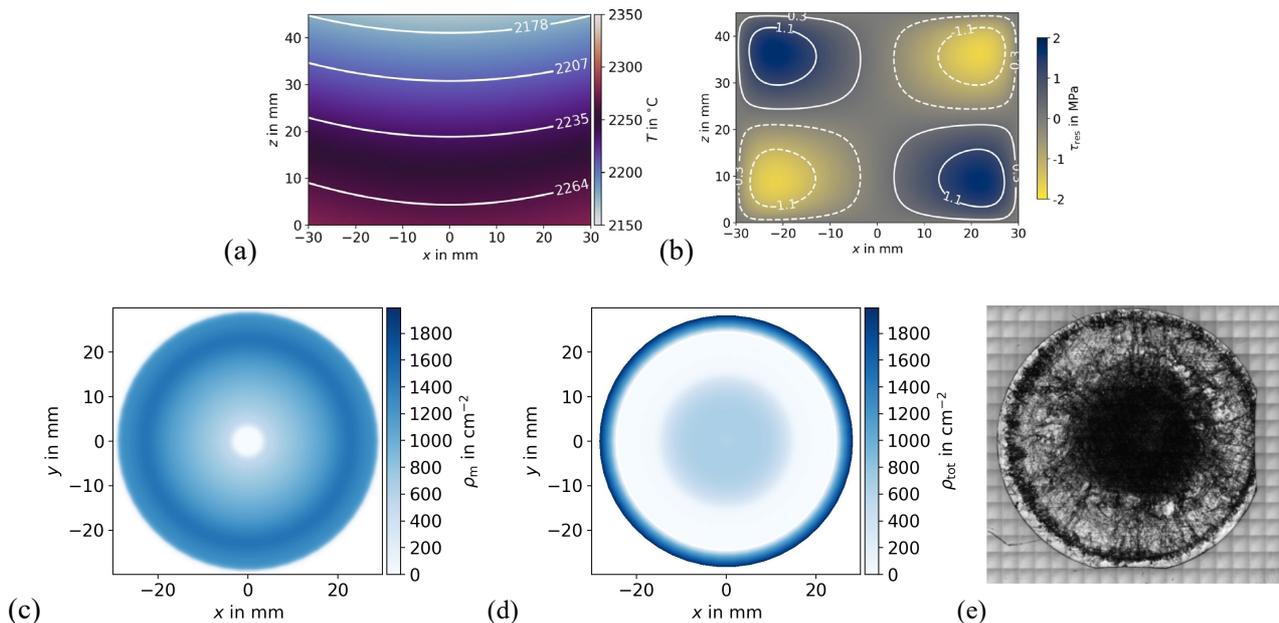


Fig. 6 Comparison of the final dislocation distribution during SiC PVT growth at ca. 2200 °C: (a) and (b) are longitudinal cuts through the SiC boule, while (c) and (d) represent cross sections at $z = 9$ mm. (a) T-field of the model-SiC boule. (b) Related calculated shear stress inside the SiC boule. (c) dislocation distribution after AH-modelling. (d) dislocation distribution after CDD-modeling using a so-called AH-GROMA approach. (e) Image of a SiC wafer that has been sliced from a SiC boule which growth conditions match quite well the modeling assumptions. KOH defect etching was carried out to visualize dislocations. Dark areas represent a high dislocation density.

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