

Defect Reduction in Epilayers for SiC Trench MOSFETs by Enhanced Epitaxial Growth

D. Baierhofer^{1,a*}, B. Thomas^{1,b}, F. Staiger^{1,c}, B. Marchetti^{1,d}, C. Förster^{1,e},
T. Erlbacher^{2,f}

¹Robert Bosch GmbH, Tübinger Str. 123, 72762 Reutlingen, Germany

²Friedrich-Alexander-Universität Erlangen-Nürnberg, Lehrstuhl für Elektronische Bauelemente,
Cauerstr. 6, 91058 Erlangen, Germany

^aDaniel.Baierhofer@de.bosch.com, ^bBernd.Thomas@de.bosch.com,

^cFrank.Staiger@de.bosch.com, ^dBenjamin.Marchetti@de.bosch.com,

^eChristian.Foerster@de.bosch.com, ^fTobias.Erlbacher@iisb.fraunhofer.de

Keywords: defect detection, epitaxial layer, defect classification, growth parameters, usable area

Abstract. The yield of high power 4H-SiC Trench-MOSFET devices, especially for those with large chip area, is largely dependent on the quality of the underlying epitaxial layers and therefore low densities of critical defects are of utmost importance. Different growth conditions for the deposition of epitaxial layers were investigated to reduce the impact of defects on electrical device performance.

For this investigation, 12 µm thick n-type epitaxial layers were grown varying growth rates for the buffer and the drift layer in a warm-wall chemical vapor deposition reactor. The defects in the epitaxial layers were characterized utilizing surface microscopy as well as ultra-violet photoluminescence techniques. A quantitative comparison of surface defects and crystallographic defects between the different growth conditions was conducted with these methods. The impact of the growth conditions on the formation of critical defects is discussed in detail. The reduction of critical defects, which resulted in an increase of the predicted die yield, as well as an outlook on future investigations, is discussed.

Introduction

Silicon carbide (SiC), more precisely the 4H polytype, is of increasing interest as a material for high power and high voltage devices due to its wide band-gap, electrical properties as well as thermal properties [1–3]. These characteristics allow the fabrication of small and efficient devices, compared to established silicon technology, e.g. high power supply inverter consisting of high breakdown voltage SiC trench metal oxide semiconductors (MOSFETs) [3, 4].

Homo-epitaxial layers of highest quality have to be grown on mono-crystalline substrates for such devices to work reliably. This includes the quality of layer thickness, roughness, doping concentration and respective homogeneities, as well as surface and crystallographic defect densities [4–6]. Existing imperfections in the SiC substrate can act as nucleation centres for additional defects in the epitaxial layer [1, 4, 6]. Carefully chosen epitaxial growth parameters allow for the transformation into other defect types, harmless for device operation [1, 4, 6]. Further classification in device critical defects (CDs) and non-critical defects has to be made, since not all defects present in the epitaxial layer cause device failures or device degradation, as their effect is also dependent on the device type [7].

This paper presents a method to reduce known CDs for trench MOSFETs by varying epitaxial growth parameters which reduces various types of stacking faults. This work focuses on the influence of the growth rate of the epitaxial buffer and drift layer on the resulting defect density while keeping all other growth parameters constant.

Experimental Procedure

Commercial 150 mm 4H-SiC substrates (all from the same supplier) with low micropipe density and off cut angle of 4° towards the $[11\bar{2}0]$ direction were used for this investigation. A homo-epitaxial n-type layer was grown on the “epi ready” polished and wet chemical cleaned Si-face substrates using a multi-wafer warm-wall chemical vapor deposition epitaxy reactor. Mitigation of generic boule impact was assured by using wafers from four different crystal boules, consequently abbreviated with the first two letters of the vendor code, LG and RF, as well as LT and TQ for the combinations of the varied growth rates (5 wafers each boule). Lasertec’s SICA88 was used for surface and crystallographic defect analysis utilizing confocal optics for surface inspection and ultra-violet photoluminescence (UV-PL) imaging.

Results

A growth run using standard conditions (STD) served as base line for comparison. The growth rate was varied to a lower growth rate (LGR) and a higher growth rate (HGR) for buffer and drift layers in various combinations. For example, a variation of the buffer growth rate was combined with a standard drift layer growth rate and vice versa. Compared to the standard process HGR refers to an increase of 50% in growth rate while LGR was carried out with a 50% decreased growth rate. All other process parameters during the epitaxial layer growth were maintained constant for all growth rate variations.

Fig. 1 shows the normalized CD counts for each wafer/crystal and growth rate. CDs include carbon inclusions and micropipe clusters, scratches, basal plane dislocations, downfalls as well as downfall related polytype inclusions and stacking faults detected on the surface (triangles and partial triangles).

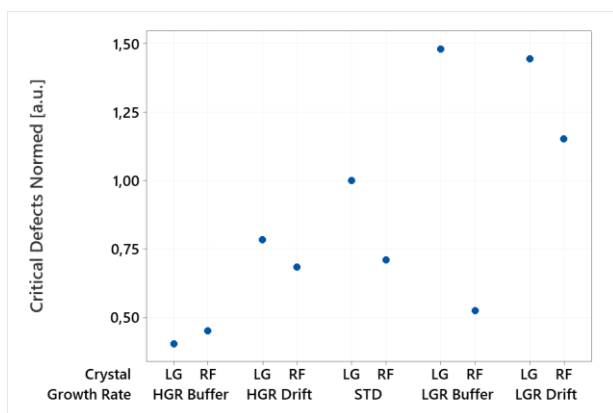


Fig. 1. Normalized critical defect counts vs. crystal and growth rate with HGR/LGR referring to high and low growth rate of the respective layer.

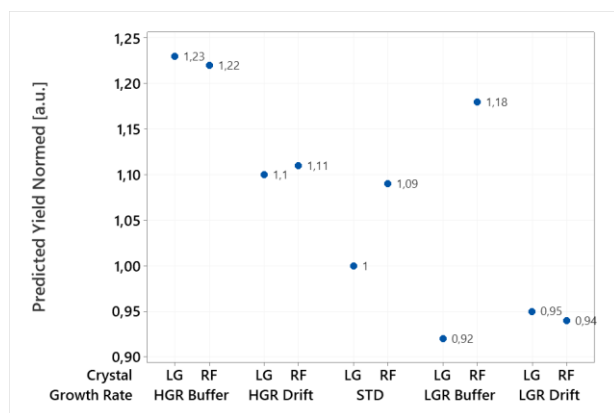


Fig. 2. Normalized predicted yield vs. crystal and growth rate with a $5 \times 5 \text{ mm}^2$ die size considering critical defects only.

In Fig. 1 and Fig. 2, the defect counts for the STD layer grown on the LG crystal were set to 1. The highest number of defects was detected with LGR of the buffer layer with 1.48 on crystal LG. Whereas in the LGR drift layer 1.44 and 1.15 critical defects for LG and RF were detected respectively, and a HGR buffer resulted in the lowest critical defect counts, 0.40 for LG and 0.45 for RF. A predicted yield for a $5 \times 5 \text{ mm}^2$ die size was calculated for each epilayer and was normalized by setting the LG crystal with standard growth rate to 1 as shown in Fig. 2. Only CDs were considered for the yield prediction. The results are consistent with those shown in Fig. 1, where high yields can be predicted with HGR Buffer, 1.23 and 1.22 for LG and RF, while low yields would result from LGR Buffer of LG, 0.92, and LGR Drift with 0.95 for LG and 0.94 for RF.

In Fig. 3, the critical defect counts are split in several detected defect class groups and plotted vs. epitaxial layer growth rate normalized by setting the standard growth parameters to 1. These defect

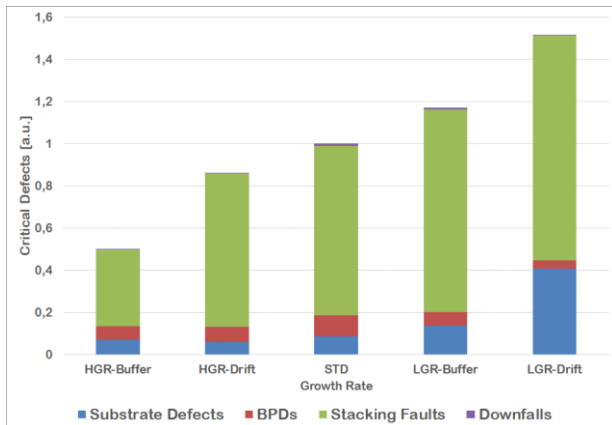


Fig. 3. Separated defect class counts included in critical defects vs. growth rate and combined for the crystals.

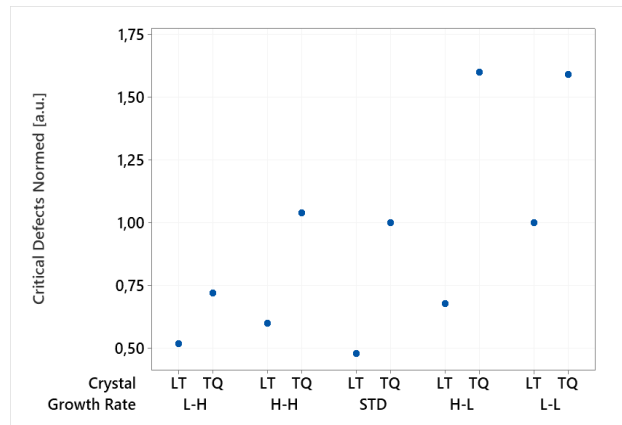


Fig. 4. Normalized critical defect counts vs crystal and growth rate with L/H referring to a lower/higher growth rate in buffer-drift.

class groups are substrate defects, i.e., scratches and polytype inclusions originated in the substrate, basal plane dislocations, various types of stacking faults excluding UV-PL only types, as well as downfalls and downfall related defects. In this graph an almost linear increase of CDs from HGR-Buffer, 0.5 defect counts, to LGR-Drift, 1.52 defect counts, can be seen.

Combinations of different growth rates were carried out based on these findings and the resulting CD counts can be seen in Fig. 4, as well as the resulting stacking fault (SF) counts in Fig. 5. In this figure, L/H refers to a lower/higher growth rate, same as previously described, for the buffer and drift layer separately with respect to the STD labeled standard growth rate for both layers which is normalized to 1 for crystal TQ. The lowest CD counts were achieved by low buffer/high drift rate combination (L-H) with 0.52 and 0.72 for the LT and TQ crystal, respectively, while the highest CD counts were detected by the low buffer and drift rate combination (L-L) with 1 for LT and 1.59 for TQ. Where STD growth rates resulted in 0.48 CD counts for the LT crystal.

Fig. 5 shows the detected CD counts of various types of surface protruding SFs. These defects, out of all defect classes considered for the CD counts shown in Fig. 4, were affected the most by the different growth rates. The number of SFs detected on the TQ crystal with STD growth rates is normed to 1. The lowest SF counts were detected by L-H with 0.79 and 0.65 for the LT and TQ crystal while highest SF counts were again detected by L-L with 1.53 for LT and 1.80 for TQ. For the LT crystal the lowest SF counts very detected by STD growth rates with 0.70.

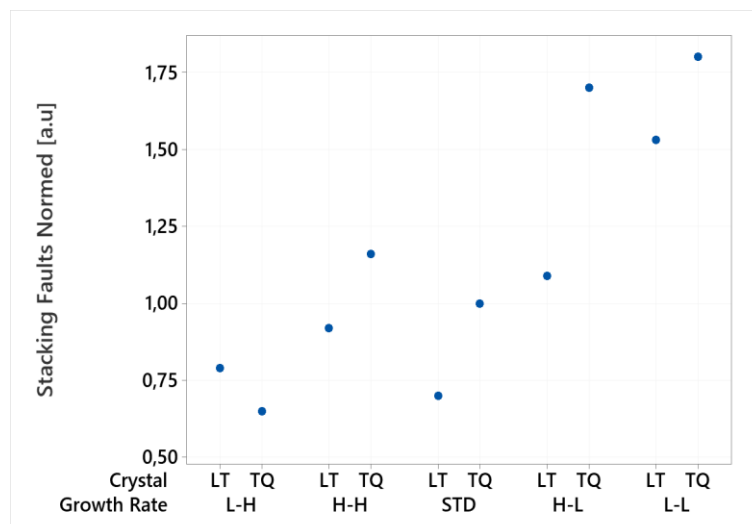


Fig. 5. Normalized stacking fault counts vs crystal and growth rate with L/H referring to a lower/higher growth rate in buffer-drift.

Discussion

Defect measurements carried out after varying either the buffer or drift layer growth rate separately, as depicted in Fig. 1, show that the LGR buffer layer deposition reduces the counts of CDs on LG by 60% and 37% on RF. Whereas using the HGR drift reduced the CDs by 22% and 3% for LG and RF. The LGR drift increases the CDs by 44% for LG and 62% for RF. The LGR buffer results in 48% more CDs on LG and 27% less CDs on RF. These values show that long deposition times, especially LGR drift, result in a consistent increase in CDs due to additional etching at high temperatures under H₂ atmosphere during the epitaxial layer deposition. In this case a significant increase in surface detected scratches on the wafer edge are mainly responsible for the increase of CD counts. The variations of the buffer layer growth rate show improved step-flow growth conditions due to a statistical saturation of the substrate surface with C and Si atoms. The reduction in CDs can consequently be seen in an increase of the predicted yield when using a generic 5x5 mm² die size grid in Fig. 2. Therefore, no significant additional bunching of CDs occurred. Combining the CD counts by growth rate, Fig. 3, shows a mostly linear increase from 50% to 152% where substrate defects, i.e., scratches, and stacking faults are impacted the most. Varying both buffer and drift layer growth rates simultaneously, Fig. 4, shows that for the L-H combination the lowest CD counts are achieved, whereas H-H results in slightly higher and similar CD counts to the standard parameter. Highest CD counts were achieved by L-L, due to significant additional etching of the surface during the layer deposition which is detected as additional scratches. During this increased growth time no additional downfall related polytype inclusions could be detected. The generation of triangular stacking faults, Fig. 5, was suppressed by the low growth rate of the buffer layer, which allows for well-defined step-flow growth and a high conversion of basal plane dislocations. The additional fast drift layer deposition reduced etching of the surface and the statistical chance of downfall related defects.

Conclusion

This paper highlights the impact of different growth conditions for buffer and epitaxy layer, i.e., growth rates and combinations thereof, on the reduction of defects with a focus on macroscopic surface protruding stacking faults in epitaxial layers of silicon carbide wafers by one vendor. Defect analysis of the 12 µm homo-epitaxial layer grown with different buffer and drift layer growth rates showed a significant difference and reduction in defects, especially those grouped as Trench-MOSFET device critical defects. In the first part of the experiment, it was established that a high buffer growth rate resulted in the lowest counts of critical defects, while the highest critical defect counts were achieved by a low drift-layer growth rate. These defect counts resulted consequently in the highest and lowest yield predictions when a generic 5x5 mm² die size grid was applied, for high buffer and low drift layer growth rate, respectively. The class of substrate defects, e.g., scratches, as well as triangular stacking faults are further identified to be impacted the most by different growth rates. Additionally, it is shown that further growth rate combinations, low buffer/high drift rate combination, resulted in lower critical defects and especially a reduction in device critical triangular stacking faults. We were able to show that the growth rate of both buffer and drift layer, affect the critical defect generation differently and play an important role in achieving highest quality epitaxial layers. Verifying the defect related improved growth conditions by comparing correlated electrical yield data will be the subject of future investigations.

Funding

This work was supported by the IPCEI project (BMW i 16IPCEI625) by the German Federal Ministry for Economic Affairs and Energy by resolution of the German Bundestag.

References

- [1] D. Baierhofer, Current SiC Power Device Development, Material Defect Measurements and Characterization at Bosch, in: 49th ESSDERC, IEEE, 2019, pp. 31–34.
- [2] B.J. Baliga, Synopsys, in: Wide Bandgap Semiconductor Power Devices, Elsevier, 2019, pp. 373–388.
- [3] T. Kimoto, SiC material properties, in: Wide Bandgap Semiconductor Power Devices, Elsevier, 2019, pp. 21–42.
- [4] T. Kimoto, H. Watanabe, Defect engineering in SiC technology for high-voltage power devices, *Appl. Phys. Express* 13 (2020) 120101.
- [5] S. Ha, P. Mieszkowski, M. Skowronski, L.B. Rowland, Dislocation conversion in 4H silicon carbide epitaxy, *Journal of Crystal Growth* 244 (2002) 257–266.
- [6] B. Kallinger, B. Thomas, S. Polster, P. Berwian, J. Friedrich, Dislocation Conversion and Propagation during Homoepitaxial Growth of 4H-SiC, *MSF* 645-648 (2010) 299–302.
- [7] H. Das, S. Sunkari, J. Justice, H. Pham, K.S. Park, Effect of Defects in Silicon Carbide Epitaxial Layers on Yield and Reliability, *MSF* 963 (2019) 284–287.