

## 150 mm SiC Engineered Substrates for High-Voltage Power Devices

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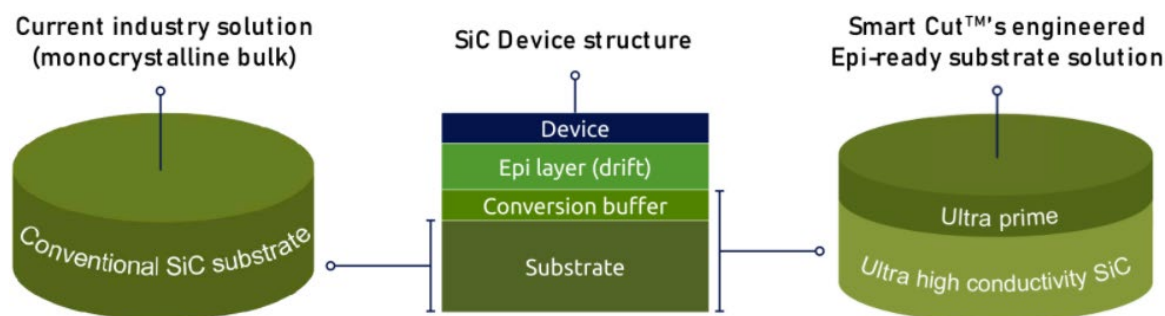
**Abstract.** Silicon Carbide (SiC) Power Devices have emerged as a breakthrough technology for a wide range of applications in the frame of high power electronics. Despite the continuously improving quality and supply of 4H-SiC substrates, the availability of such wafers is still insufficient. An advantageous opportunity is offered by the Smart Cut™ technology with the integration of a very high quality SiC layer transferred to a low resistivity handle wafer. This bi-layer material enables a significant yield optimization and improvement of the device's electrical performance. Moreover, an additional key feature of the Smart Cut™ technology is the possibility to re-use multiple times the donor wafer, leading to reduced manufacturing costs and enabling the high volume production of SiC wafers. In this paper, we report the latest advances in the development of such so called SmartSiC™ substrates.

### Introduction

Among its unique properties, including high electric field breakdown strength and high thermal conductivity, Silicon carbide (SiC) is a material of choice for power devices allowing a higher frequency operation but also to reduce the size and the power losses of the devices. Thus, SiC is a key material for devices developed for high growth applications such as automotive or renewable energy [1]. Semiconductor companies are currently facing an urgent need for capacity expansion to meet the growing market demands. Despite the recent progress in 4H-SiC material with a continuous improvement of the quality and the supply, the availability of near defect-free wafers, enabling very high yields, is still insufficient. In this context, we have developed an innovative bi-layer SiC substrate, and installed a dedicated Pilot Line to support the technology development and initial sampling. Thanks to the Smart Cut™ technology [2], a very high quality 4H-SiC layer is transferred to a specific handle wafer with low resistivity leading to improvement of the device yield and electrical performance.

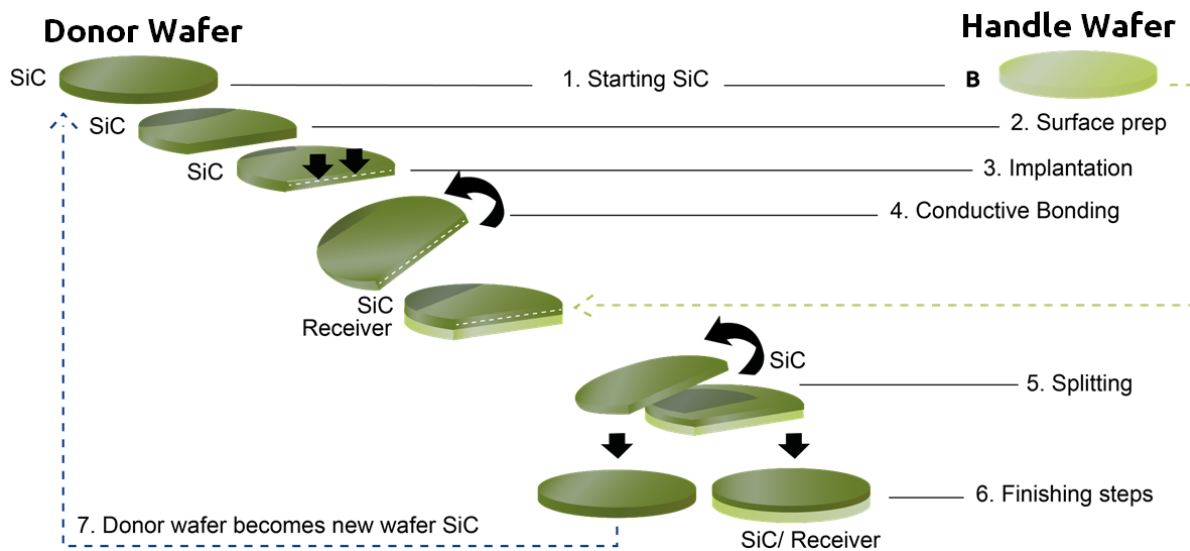
### Smart Cut™ Technology and Low Resistivity Material

For over 30 years, the Smart Cut™ technology has been used to produce several millions of wafers, through high volume manufacturing processes, mostly silicon wafers. The process has been successfully adapted for SiC material by transferring a high quality crystalline SiC layer to a low resistive wafer support (Fig. 1) [2-5]. Thereby the engineered SmartSiC™ substrate is epi-ready and the epitaxy growth process to be performed is simpler than for conventional SiC wafers, as the conversion buffer layer is already done.



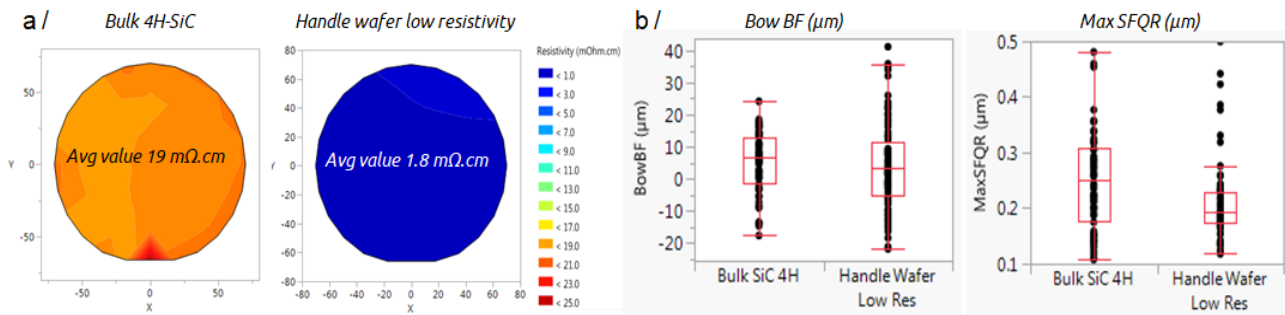
**Figure 1:** SmartSiC™ versus bulk 4H-SiC substrates for power devices [2-3]

The Smart Cut™ technology, described in the following figure (Fig. 2), is based on several key steps like the hydrogen implantation of the donor wafer, allowing to control the thickness of the transferred layer (from 0.1  $\mu\text{m}$  to 1  $\mu\text{m}$ ). A key element of the transfer process is the realization of a highly conductive bonding interface to ensure excellent vertical conductivity through the newly formed substrate. The finishing steps ensure excellent roughness and thermal stability, to prepare an EPI-ready surface. The donor wafer is re-used multiple times, opening the path for high volume wafer production.



**Figure 2:** Smart Cut™ process description [2-3]

The geometrical and electrical properties of the finished product are closely driven by those of the handle wafer. Fig. 3 illustrates the low resistivity values obtained within the engineered substrate in comparison to commercially available bulk 4H-SiC (Fig. 3a) – the electrical resistivity of the innovated substrate is at least 4 times lower than standard bulk 4H-SiC. Moreover, in addition to the improved electrical conductivity, the shape of product, measured through wafer diameters, the thickness, the edge shape, the bow, the warp, the Site Front sQuare focal plane Range (SFQR) and the Total Thickness Variation (TTV) is equivalent to commercial bulk 4H-SiC wafers. (Fig. 3b)



**Figure 3:** 3.a/ Resistivity mapping by Eddy Current measurement on 4H-SiC compared to handle wafer low resistivity. 3.b/ BOW & SFQR values distribution on both the reference 4H-SiC bulk wafer and the low resistivity handle wafer

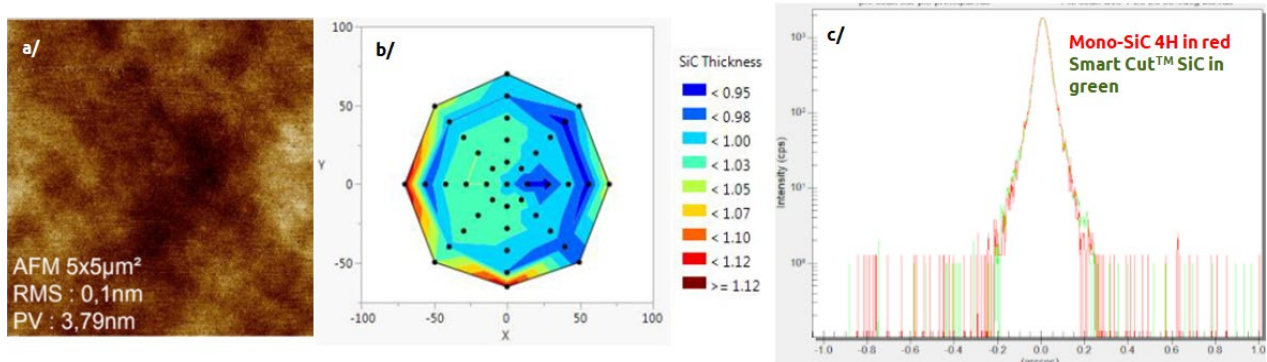
### SmartSiC™ Performance and Validation

An excellent 4H-SiC layer integrity and quality is demonstrated. The picture on Fig 4 shows a 150 mm SmartSiC™ substrate, highlighting the defect-free surface quality, including the small edge crown width (< 5 mm).



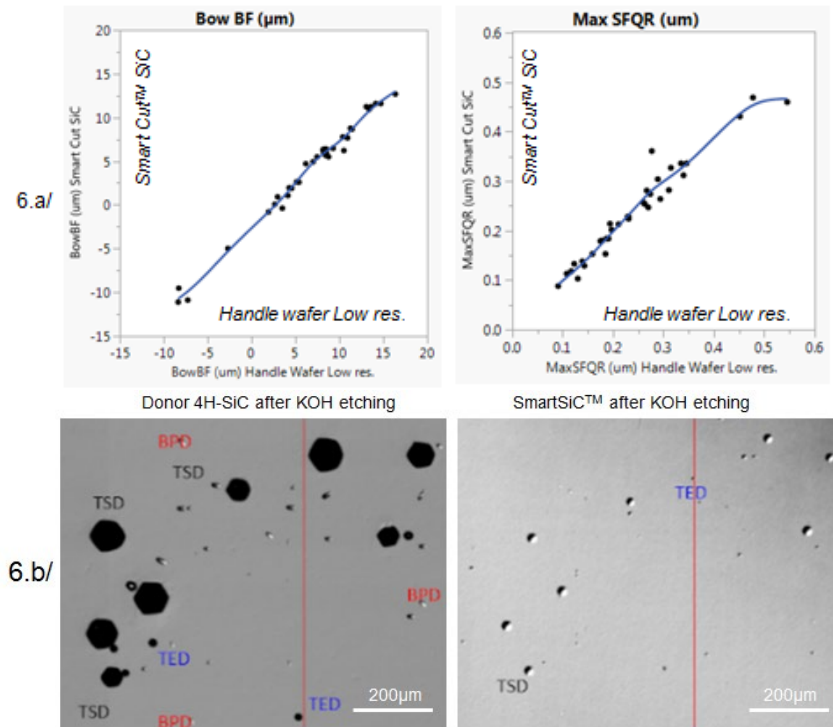
**Figure 4:** Picture of a Smart SiC™ substrate

Intensive physical, chemical and electrical characterizations have been conducted on the SmartSiC™ to assess the performance of the engineered substrate. Thus, the roughness measurements carried out by AFM in 5x5 μm<sup>2</sup> scan confirm the achievement of a smooth surface with  $R_q < 1 \text{ Å}$  (Fig. 5a), similar to a standard 4H-SiC substrate. The thickness uniformity of the transferred layer was also measured and a standard deviation lower than 4% was determined (Fig. 5b). The grazing incidence diffraction by X-Ray (GID) on {11-20} plane shows that the 4H-SiC layer on the final product is fully stress relaxed (Fig. 5c). Thus, the top 4H-SiC layer on the Smart Cut™ substrate is guaranteed to be EPI-ready.



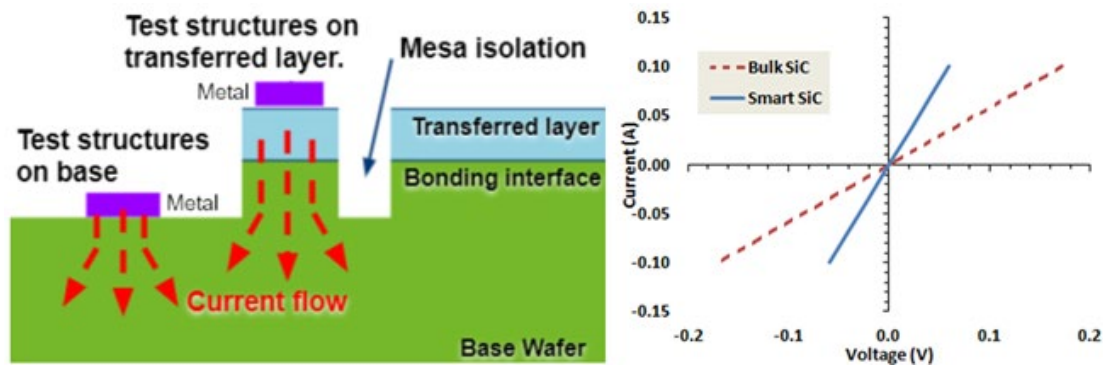
**Figure 5:** 5.a/ AFM on SmartSiC™ & 5.b/ SmartSiC™ Layer uniformity & 5.c/ GID on {11-20} plane 4H-SiC comparison with SmartSiC™

From the well-known manufacturing experience, the Smart Cut™ process does not impact the geometry of the incoming material. Thus, SmartSiC™ exhibits the same performance on wafer geometry parameters like flatness, bow, warp and TTV compared to the handle wafer low resistivity (Fig. 6a). The crystal quality of the final substrate is directly linked to that of the donor wafer. We have developed a specific characterization by KOH etching (specially adapted to analyze a thin film), and this one confirms the absence of crystal defect creation during the Smart Cut™ process. SICA inspections on SmartSiC™ and 4H-SiC donors after KOH etching show exactly the same defect density trend (Fig. 6b).



**Figure 6:** 6.a/ SmartSiC™ geometry & 6.b/ SICA on 4H-SiC donor & SmartSiC™ after KOH etching (same scan position)

Last but not least, to monitor the electrical performance of the composite wafer, a test structure has been developed to determine the resistivity of the bonding interface (Ohmic behavior with an interface resistivity  $< 0.1 \text{ m}\Omega\cdot\text{cm}^2$ ). I(V) curves show that SmartSiC™ has a lower resistivity than conventional 4H-SiC (Fig. 7). Thus, this SiC substrate improves the total vertical resistance by a factor of at least 2 (wafer thickness at 100 μm) to 3 (wafer thickness at 350 μm) versus 4H-SiC.



**Figure 7:** Electrical test structure and I(V) result

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## Conclusions

The Smart Cut™ technology provides for the power devices manufacturers an innovative SmartSiC™ substrate with high crystal quality and low electrical resistivity. The recycling of the initial (donor) SiC wafer enables cost-effective manufacturing of very large volumes with reduced investments. A pilot line is currently ready for 150 mm substrates and 200 mm substrates preparation will be engaged beginning of 2022.

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