

Vanadium Incorporation in 3C-SiC Epilayers and its Consequences for Electrical Properties of 3C-SiC Material

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Abstract. The present experimental study demonstrates the feasibility of Vanadium doping of 3C-SiC hetero-epitaxial material. Vanadium concentration in 3C-SiC is determined from SIMS measurements. Some of Vanadium incorporation trends as well as the influence of Vanadium doping on 3C-SiC resistivity are observed.

Introduction

Semi-insulating (SI) Silicon Carbide is used at industrial scale as substrate material for high frequency GaN based devices in order to minimize the parasitic conduction that reduces the device performance. During last 10 years it became also the support of choice for graphene related devices. Highly resistive SiC substrates were obtained through the introduction of Vanadium (V) doping in PVT bulk growth in mid-90's. However, the V concentration close to solubility limit, necessary to compensate important residual doping of the crystal, was at the origin of degradation of structural quality of bulk material. Progressively, V-doped SiC substrates were replaced by high purity semi-insulating material using intrinsic defects (ex C-vacancies) to compensate the residual doping.

A renewed interest in Vanadium doping came in late 2010's with the possibility of introducing V in epitaxially grown 4H-SiC. Strongly resistive epilayers of well controlled thickness and resistivity were obtained within (relatively) cheap CVD growth process [1, 2].

In the case of cubic silicon carbide (3C-SiC), one of the issues that prevent the development of electronic devices based on heteroepitaxial 3C-SiC epilayers is the presence of important leakage current related to existence of intrinsic structural defects within the material (stacking faults, μ -twins, grain boundaries) [3, 4], especially in the near interface region of the epilayer. One could expect that the incorporation of Vanadium, especially during the first phase of the growth, should reduce the leakage and improve the electrical properties of the material.

In the present contribution we test the feasibility of Vanadium doping of 3C-SiC epilayers grown on silicon, investigate some of incorporation trends and evaluate the influence of Vanadium incorporation on electrical properties of 3C-SiC material.

Experimental Details

CVD setup. Previously described horizontal, low pressure, resistively heated hot wall CVD system with rotating sample holder [5] was employed for deposition of SiC epilayers, with standard chemistry: purified hydrogen (H_2) as carrier gas, high purity (5N) silane (SiH_4) and propane (C_3H_8) as principal precursors. We chose Vanadium tetrachloride (VTC, VCl_4) as Vanadium precursor. The VCl_4 bubbler under stabilized pressure / temperature was connected to an H_2 dilution line. This approach allowed the control of VCl_4 flowrates in the range $1 \times 10^{-4} - 2.0$ sccm.

Sample description. Standard characteristics of 3C-SiC epilayers were described in [6]. For the present study, three series of 3C-SiC/Si samples were prepared. First, a batch of 4 μm thick 3C-

SiC(100) epilayers were grown with various VCl_4 flowrates to establish the maximum Vanadium supply that does not deteriorate the structural / morphological properties of 3C-SiC. In second series, multilayer 3C-SiC(100) and (111) samples with variable Vanadium supply were prepared for SIMS analyses. Finally, a series of thin ($< 0.6 \mu\text{m}$) 3C-SiC epilayers was grown on highly resistive Si(111) substrates ($\rho > 5 \text{ k}\Omega\text{cm}$). Contactless sheet resistance measurements were performed on these epiwafers after backside polishing (necessary to remove the parasitic conductive poly-3C-SiC deposited on the backside).

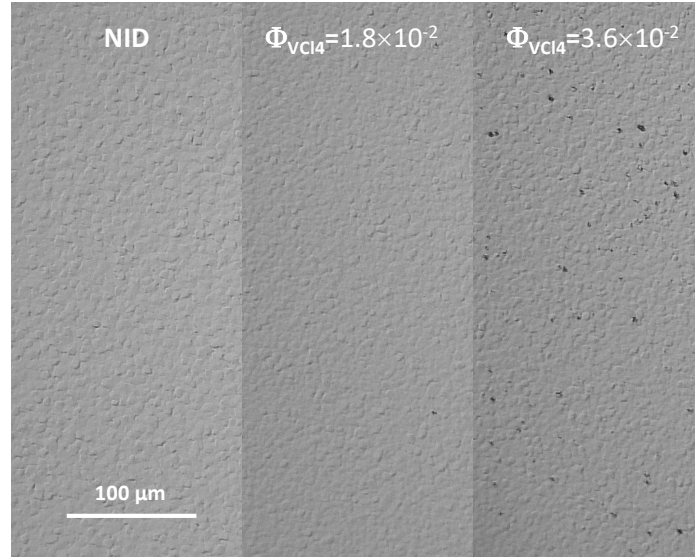


Figure 1. Optical microscopy images of $4 \mu\text{m}$ thick 3C-SiC(100) epilayers. Left: standard NID film. Center and right: V doped films. VCl_4 flowrate is indicated on the top of the image.

To allow the comparison with literature results that exist for hexagonal polytype, 4H-SiC multilayer stacks for SIMS analyzes and single layer samples were prepared. High resistivity SiC films were grown with Vanadium concentration $[\text{V}]$ estimated at $[\text{V}] \sim 4 \times 10^{15} \text{ at}/\text{cm}^3$.

Experimental Results and Discussion

Vanadium incorporation in 3C-SiC. Figure 1 shows typical optical microscopy images of $4 \mu\text{m}$ thick 3C-SiC(100) epilayers. Films with VCl_4 flowrates up to $1.8 \times 10^{-2} \text{ sccm}$ present the same morphology as for standard, undoped (NID) film. For higher Vanadium supply (starting from $3.6 \times 10^{-2} \text{ sccm}$), surface defects appear.

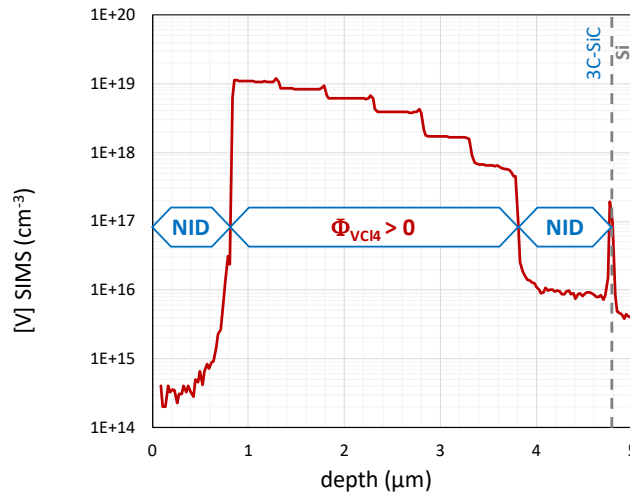


Figure 2. Example of SIMS depth profile of Vanadium incorporation in 3C-SiC(100).

Figure 2 shows the depth profile of Vanadium incorporation [V] measured by SIMS in 3C-SiC(100) film grown under VCl_4 supply increasing step by step. SIMS analyses were precisely calibrated using reference sample with controlled Vanadium concentration. To avoid the structural deterioration of the sample we limited the Vanadium supply to 1.8×10^{-2} sccm. Sublayers are clearly defined and the interface between strongly V doped and the topmost, V-free, sublayer is sharp ([V] drop > 4 decades). Minor Vanadium memory effect persists however, as reflected by presence of small [V] peak at 3C-SiC/Si interface.

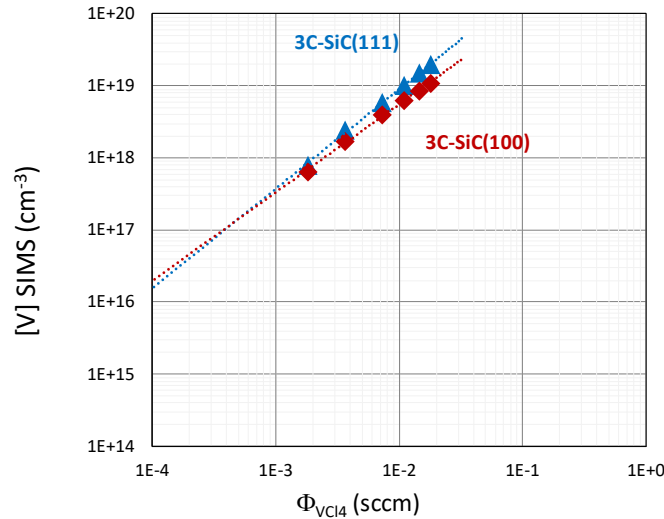


Figure 3. Vanadium incorporation as a function of VCl_4 supply in 3C-SiC(100) and 3C-SiC(111).

In Figure 3 we show the Vanadium incorporation, deduced from SIMS analysis of multilayer samples as a function of VCl_4 flowrate. Vanadium incorporation in (111) oriented 3C-SiC is slightly higher than for (100) orientation. For both orientations the experimental data can be fitted with power function (exponent ~ 1.4 for (111) and 1.3 for (100) orientation).

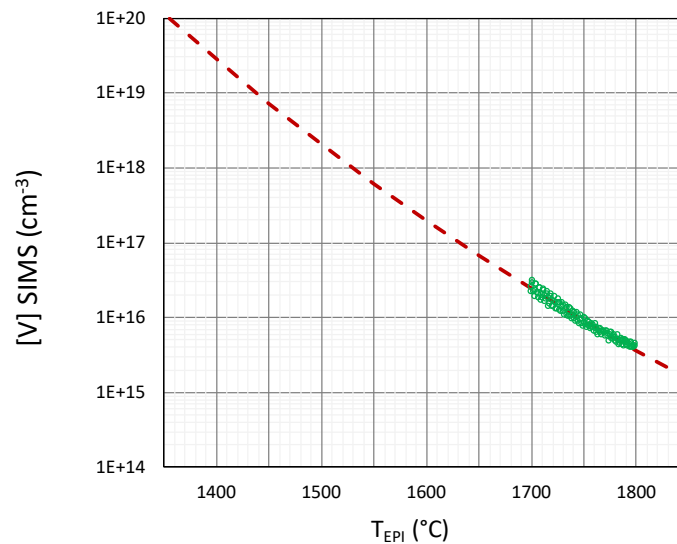


Figure 4. Growth temperature dependence of Vanadium incorporation in 4H-SiC, extrapolated to lower temperature range.

Taking into account literature data on V solubility in 4H-SiC (solubility limit $\sim 10^{17} \text{ cm}^{-3}$) and low applied flowrates of VCl_4 (< 0.02 sccm), Vanadium concentration range indicated on the figures 2 and 3 ($1 \times 10^{18} - 1 \times 10^{19} \text{ cm}^{-3}$) may appear overestimated. To evacuate the possible doubts on validity of SIMS calibration and ensure the compatibility of our data with existing literature results, we performed some comparative growth experiments on Si-face 4H-SiC. We show in

Figure 4 SIMS results taken from a 4H-SiC epilayer grown during a slow temperature ramp between 1700°C – 1800°C. Their extrapolation down to 3C-SiC deposition regime (<1400°C) allows to estimate Vanadium incorporation above $1 \times 10^{19} \text{ cm}^{-3}$ at 1400°C, i.e. 3 decades higher than in 4H-SiC.

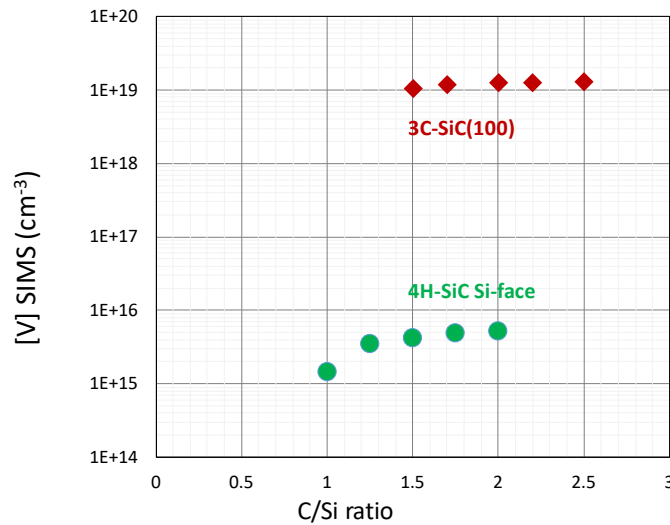


Figure 5. Vanadium incorporation as a function of C/Si ratio in 3C-SiC(100) and 4H-SiC Si-face.

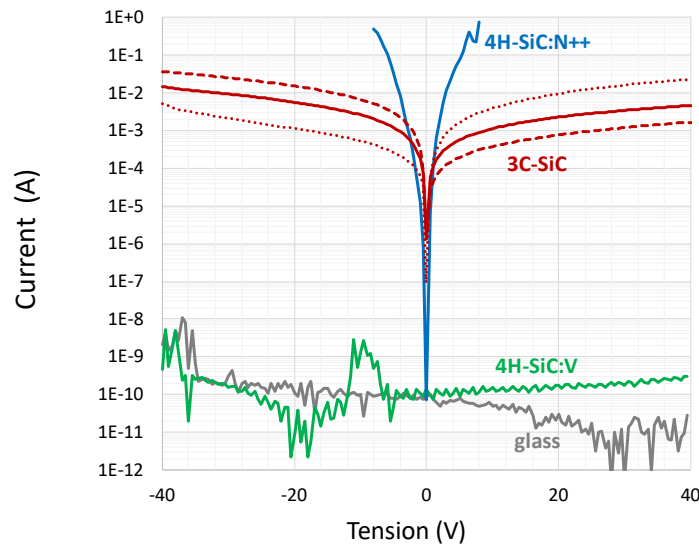


Figure 6. DC I-V curves recorded in vertical configuration for n-doped 4H-SiC substrate (blue), 4H-SiC:V (green), glass (grey), 3C-SiC:V (red, continuous), 3C-SiC:N+ (red, dots) and 3C-SiC NID (red, dashed line).

We compare in Figure 5 the influence of C/Si ratio on [V] in 4H-SiC Si-face and 3C-SiC(100) under same VCl_4 supply $\Phi_{\text{VCl}_4} = 5.4 \times 10^{-3} \text{ sccm}$. In 4H-SiC, [V] slightly increases with increasing C/Si ratio, suggesting preferential incorporation on Si sites, which is expected taking into account atomic radii. In 3C-SiC this increase is marginal (but the study could be performed only for $\text{C/Si} > 1.5$). Together with almost identical incorporation in (100) and (111) oriented samples (Fig. 3), the results obtained in 3C-SiC do not confirm that Vanadium incorporates on Si-sites.

Electric properties of 3C-SiC:V. The conditions of Vanadium supply during the growth of a series of thin, highly resistive 3C-SiC/Si(111) templates are reported in Table I. Eddy current sheet resistance of standard, Vanadium-free reference sample (A) is $2 \text{ k}\Omega/\text{sq}$ (mean value of 17 points cartography on 100mm diameter wafer). The resistance of sample (B), with V-doping in topmost part of epilayer increases to $9 \text{ k}\Omega/\text{sq}$. In Sample (C), where the Vanadium was supplied during

entire CVD step, further increase to 14 k Ω /sq was recorded. Introduction of VCl₄ during carbonization step does not seem to further enhance the epilayer sheet resistance (sample D). Finally, for thicker epilayer with increased V supply we recorded 15 k Ω /sq. This enhancement of sheet resistance with respect to Vanadium free epilayer is certainly due to Vanadium doping. However, taking into account the reduced 3C-SiC thickness (0.4-0.6 μ m), corresponding 3C-SiC resistivity remains below 1 Ω cm, very far from the values of bulk SI 4H-SiC material (typically >10¹⁰ Ω cm).

Table 1. List of 3C-SiC/Si(111) (H.R.) samples and conditions of Vanadium supply. “V” and “2V” stand for VCl₄ flowrate of, respectively, 1.8 \times 10⁻³ sccm and 3.6 \times 10⁻³ sccm. Related Vanadium concentration in 3C-SiC epilayer is, respectively, 0.8 \times 10¹⁸ cm⁻³ 2.4 \times 10¹⁸ cm⁻³.

Sample:	(A)	(B)	(C)	(D)	(E)
Carbonization:	no V	no V	no V	V	V
Epitaxy:	0.4 μ m NID	0.1 μ m NID 0.3 μ m V	0.4 μ m V	0.4 μ m V	0.6 μ m 2V
R _{SHEET}	2 k Ω /sq	9 k Ω /sq	14 k Ω /sq	11 k Ω /sq	15 k Ω /sq

I-V measurements were performed using Hg probe in vertical configuration (Hg contact, $\phi \sim 0.8$ mm, on the topside of the wafer, mechanical metal contact, $\phi \sim 25$ mm, on the backside) for different types of SiC material. The DC I-V curves (in ± 40 V range) are reported in Figure 6. Obviously, this approach does not allow us to statue quantitatively on the resistivity of SiC material. However, a qualitative differences can be clearly seen: for highly conductive 4H-SiC:N+ substrate ($\rho \sim 0.02$ Ω cm), 1 A current range is reached for voltages below ± 10 V. After the deposition of 20 μ m thick 4H-SiC:V epilayer ($[V] \sim 4 \times 10^{15}$ at/cm³) on such conductive substrate, the I-V vertical characteristics become similar to those of insulating glass (measured current below 10⁻⁹ A).

For 3C-SiC/Si the I-V curves are reported for 3 samples with differently doped 3C-SiC epilayer: NID, $[N] > 10^{19}$ cm⁻³, $[V] \sim 10^{19}$ cm⁻³, grown on lowly conductive substrate ($\rho > 200$ Ω cm). All the samples exhibit similar electric behavior indicating that vertical conduction is dominated by the substrate resistivity. The Vanadium related increase of 3C-SiC resistivity is too small to reduce significantly the vertical conductance of the epiwafer. We may conjecture that despite high Vanadium concentration, not all V atoms are acting as traps or that conduction through extended defects paths in 3C-SiC cannot be screened by the presence of V atoms. Even if at this stage we did not observe by optical microscopy any big precipitation defects reported in [1], we can't exclude the formation of submicron, V-rich clusters. The study will be continued to verify this hypothesis.

Conclusion

Through this study we demonstrated the feasibility of V doping of CVD grown 3C-SiC epilayers and validated the V-related increase of 3C-SiC resistivity. The effect of Vanadium introduction is not as spectacular as in 4H-SiC epilayers, where semi-insulating character of epilayer was achieved. However, observed increase of epilayer resistivity may still be useful ex. in preparation of templates for III-N based RF HEMT devices.

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