Charge Trapping Mechanisms in Nitridated SiO_2/4H-SiC MOSFET Interfaces: Threshold Voltage Instability and Interface Chemistry

P. Fiorenza[1,a*], C. Bongiorno[1,b], A. Messina[2,c], M. Saggio[2,d], F. Giannazzo[1,e], F. Roccaforte[1,f]

[1]CNR-IMM, Strada VIII 5 95121, Catania, Italy

[2]STMicroelectronics Stradale Primosole 50 95121, Catania, Italy

[a]patrick.fiorenza@imm.cnr.it, [b]corrado.bongiorno@imm.cnr.it, [c]angelo.messina@st.com, [d]mario.saggio@st.com, [e]filippo.giannazzo@imm.cnr.it, [f]fabrizio.roccaforte@imm.cnr.it

*corresponding author

Abstract. Silicon dioxide (SiO_2) layers deposited on 4H-SiC and subjected to different post deposition annealing (PDA) in NO and N_2O were studied to identify the key factors influencing the channel mobility and threshold voltage stability in lateral implanted 4H-SiC MOSFETs. Cyclic gate bias stress measurements allowed to separate the contributions of interface states (N_{it}) and near interface oxide traps (NIOTs) in the two oxides. The reduction of these traps in the NO annealed sample is due to the lower amounts of sub-stoichiometric silicon oxide (~1nm) and carbon-related defects (<1nm) at the interface, as could be demonstrated by Electron Energy Loss Spectroscopy. The experimental results indicate that limiting the SiC re-oxidation during post-deposition annealing in MOSFET technology is a key factor to improve the mobility and threshold voltage stability.

Introduction

The performances of 4H-SiC MOSFETs are strongly influenced by the processing of the SiO_2/4H-SiC interface [1,2]. In particular, threshold voltage (V_{th}) instability phenomena [3,4] and poor field effect channel mobility (μ_{FE}) [5,6] often occur in these devices and can be partially mitigated by post oxidation annealings (POA) or post oxide deposition annealings (PDAs) [5]. Hence, a great attention of the scientific community is devoted to optimize the SiO_2/4H-SiC interface by POAs or PDAs. However, while the introduction of Nitrogen or others atomic species can produce some benefits in the interfacial carrier transport, they can introduce additional trapping states, which are detrimental for the V_{th} stability [7]. Hence, the introduction of such undesired traps at the SiO_2/4H-SiC interface should be limited.

On the other hand, it is mandatory to develop reliable, fast and accurate V_{th} determination methods, able to minimize the amount of undetected traps during the investigation [8].

In this paper, SiO_2/4H-SiC interfaces on implanted p-type 4H-SiC, formed with deposited SiO_2 subjected to different PDAs in NO or N_2O, were investigated by cyclic gate stress measurements to determine the amount of trapped charges. Furthermore, nanoscale structural/chemical analyses allowed to identify the key factors influencing the channel mobility and V_{th} stability in lateral MOSFETs. In particular, a correlation between the chemical disorder at the deposited SiO_2/4H-SiC interface after the PDAs and the electrical properties of the lateral MOSFETs is presented.

Experimental

In this paper, different lateral MOSFETs were fabricated on 4∘-off-axis n-type (0001) 4H-SiC epitaxial layers (1×10^{16} cm^{-3}), with a p-type Al-implanted body region ($N_A \sim 10^{17}$cm^{-3}). The gate oxide was a 40 nm thick deposited SiO_2 layer [9]. Different PDAs were performed in a horizontal furnace in a sub-atmospheric pressure regime at 1150 °C in NO or N_2O [10], in order to investigate the electrical and chemical impact on the SiO_2/4H-SiC interface.

The MOSFETs were characterized by means of current voltage (I_D-V_G) transfer characteristics measured in a CASCADE Microtech probe station, using a Keysight B1505A parameter analyzer. The MOSFETs chemistry interface was investigated by Scanning Transmission Electron Microscopy (STEM) analyses (JEOL ARM200CF at a primary beam energy of 200 keV) and electron energy loss spectroscopy (EELS).

Results and Discussion

The standard procedure to determine the threshold voltage V_{th} in lateral MOSFETs uses the linear fit of $I_D^{0.5}$ vs V_G. However, this method requires the gate bias sweep and can be not sensitive to an eventual variation of the charge state in the insulator during the measurement. Hence, it is important to minimize the system perturbation induced by the V_{th} measurement itself. Recently, we have presented a method to measure the V_{th} variation by means of a single point I_D measurement, avoiding relaxing effects on the majority of trapped charge [8]. The whole semiconductor bandgap trapping states were probed by varying the gate bias stress from inversion to accumulation and backward followed by a single point V_{th} measurement at $V_G = V_{read} = +8$ V.

Fig. 1a describes schematically the cyclic gate bias sequence used to probe the whole 4H-SiC bandgap and to probe the V_{th} variations. Fig. 1b shows how the I_D measured at $V_{read} = +8$ V varied upon the cyclic gate bias stress is applied. The I_D variation can be correlated to the V_{th} variation.

The V_{th} variation occurring from the minimum and maximum V_G stress values can be associated to the total amount of electrons (N_{it}) that can be trapped at the interface traps [8]. On the other hand, closing the cyclic gate bias sequence it is possible to notice a residual V_{th} variation at $V_G = 0$ V. This can be associated to the remaining amount of charge at the near interface oxide traps (NIOTs) [8]. Fig. 1b shows the I_D values measured at $V_{read}=+8$V for each stress point according to Fig. 1a on the sample after a PDA in N_2O. Those single point I_D measurements can converted to threshold voltage variation ΔV_{th}. If this variation ΔV_{th} is monitored at different temperatures (e.g., from 25 °C up to 200 °C), it is possible to monitor the amount of detectable N_{it} and NIOTs in the two systems.
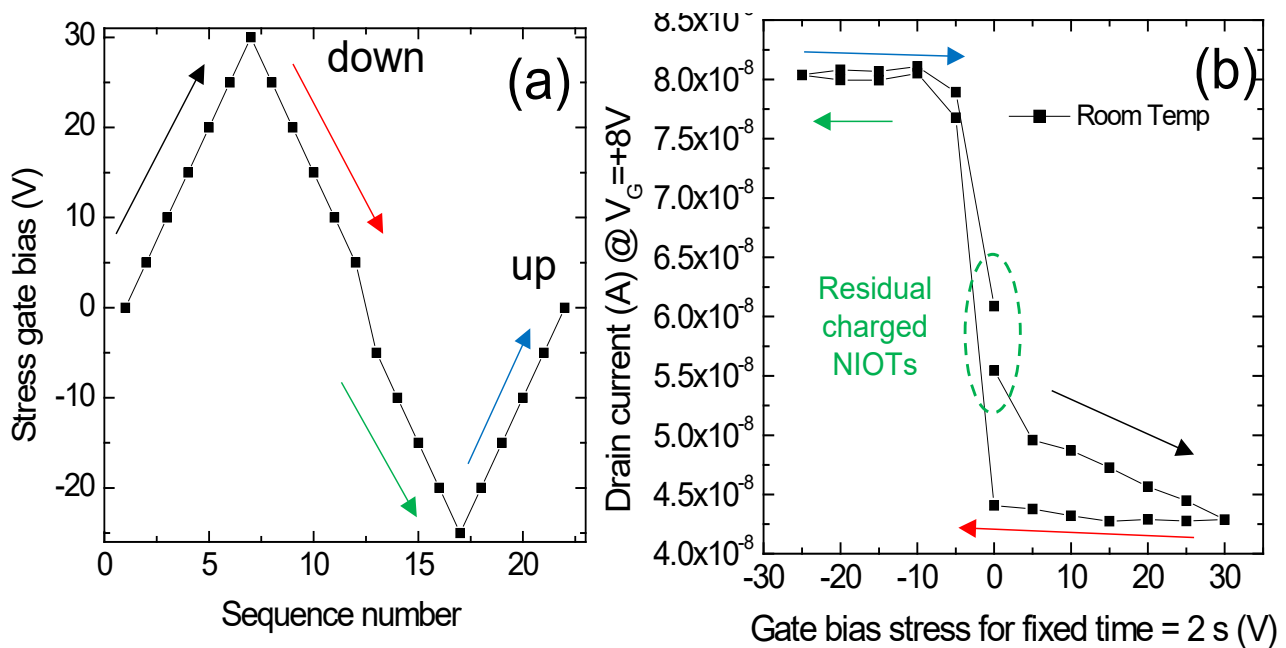

Fig. 1. (a) Schematic illustration of the cycling gate bias stress sequence. (b) Experimental single V_G point measured I_D during the cyclic gate bias stress for a fixed time of 2 s used to extrapolate the V_{th} variation.

By repeating the experimental procedure on the samples under investigation, it is possible to estimate the total amount of traps at the interface N_{it} and in the oxide NIOTs. In particular, the amount of detected N_{it} decreases with the increasing temperature (from 6×10^{11} cm^{-2}), while the detected NIOTs are nearly constant in the investigated temperature range (about 1×10^{11} cm^{-2}) [8,11]. This behavior can be associated to a tunneling mechanism from the semiconductor into a trap located into the insulator [11-13]. On the other hand, it has been demonstrated that the V_{th} main variation is due to the N_{it} and their charge retention capability has an activation energy of $E_A=0.1$ eV, which in turn can be associated to the intrinsic interface state defects of the $SiO_2/4H$-SiC system [13].

The PDAs performed in NO or N_2O resulted into a different MOSFET electrical behavior. For example, the maximum field effect mobility value after annealing in NO (55 cm^{2}V^{-1}s^{-1}) was more than twice larger than the value measured in the sample annealed in N_2O (20 cm^{2}V^{-1}s^{-1}). Moreover, the different PDAs performed in NO or N_2O produced different V_{th} variation under the cyclic bias stress. As described previously, from the cyclic bias stress it is possible to extract both the N_{it} and the NIOTs. Hence, the relative amount of the N_{it} and NIOTs can be varied by a fine tuning of the PDA. As an example a PDA in NO reduced both trapping mechanisms reducing the V_{th} instability (and increasing the field effect mobility). In particular, Fig. 2a shows the comparison between the V_{th} variation during the cyclic stress obtained on the samples after PDAs in NO and N_2O respectively. As can be seen in the highlighted region of Fig. 2a, the PDA in NO demonstrates a reduction of both the N_{it} and NIOTs with respect of the PDA in N_2O [14]. Evidently, the two $SiO_2/4H$-SiC interfaces produced with the two different PDAs are different. Such difference has to be pursued at the intimate chemical nature of the interface.

Fig. 2b shows the comparison of the EELS profile collected on both PDA SiO_2/SiC interfaces, demonstrating that the improved N_{it} and NIOTs in the NO sample can be associated to a reduced amount of SiO_x and C-based defects [14].
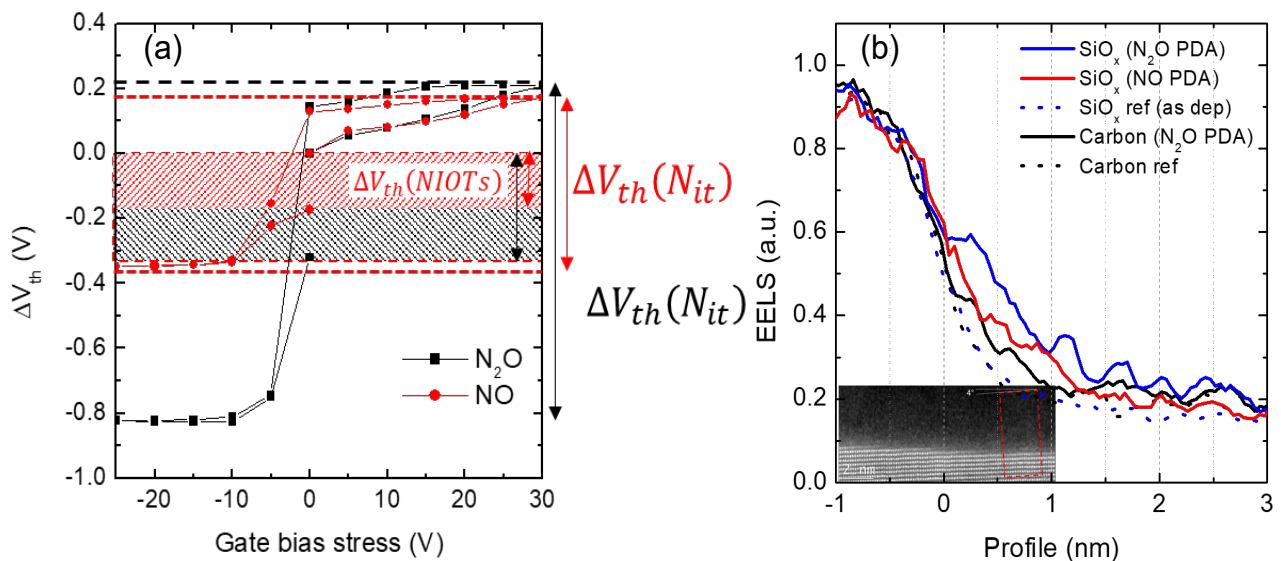

Fig. 2. (a) V_{th} variation during the cyclic gate bias stress on N_2O and NO samples. V_{th} variation between $V_G = -25$ V and $+30$ V corresponds to the total N_{it} and the residual V_{th} variation at $V_G = 0$ V corresponds to theNIOTs. (b) EELS profiles of SiO_x and carbon for PDA in N_2O and NO.

Fig. 2b shows the carbon and SiO_x EELS profiles collected on both N_2O and NO samples. The PDAs signals are compared to those collected on the as deposited reference sample. The as deposited interface shows carbon and SiO_x profiles that represent the steepest transition between the SiC substrate and the SiO_2 insulator. As can be noticed, both PDAs produced a broader interface element transition compared to the as deposited sample. This progressive change in the SiO_x and carbon profiles across the $SiO_2/4H$-SiC interface are due to the slight re-oxidation induced by the PDA. These results allowed to draw the correlation between the electrical properties and the chemical order at the $SiO_2/4H$-SiC interface. In particular, it is worth noticing that the smaller amount of interface traps in

the sample annealed in NO can be associated to a thinner and steeper sub-stoichiometric SiO_x layer with respect to the N_2O case. Furthermore, both samples show similar carbon. In particular, the carbon profiles show a decreasing tail within the oxide. The carbon tails extend from the SiC interface into the oxide for about 1.2 nm and 0.9 nm for the sample annealed in N_2O in NO, respectively. It has to be emphasized that in Fig. 2b only the carbon profile of the sample annealed in N_2O is shown for the sake of clarity. These carbon-related defects within the insulator can be associated to the residual NIOTs detected by the cyclic gate bias stress procedure.

Conclusion

In this paper, a combined electrical/chemical study of deposited SiO_2/4H-SiC interfaces on implanted p-type 4H-SiC, subjected to different PDAs in NO or N_2O is presented. The lateral MOSFETs were investigated by cyclic gate stress measurements and nanoscale structural/chemical analyses. This basic study allowed to identify the key factors influencing the channel mobility and V_{th} stability in lateral MOSFETs. The results demonstrated that the threshold voltage instability of 4H-SiC MOSFETs, associated to different trapping mechanisms, is directly related to the SiO_2/SiC interface chemistry and can be mitigated by an accurate control of the nitridation conditions of deposited oxides. In particular, interface traps can be associated to a sub-stoichiometric SiO_x layer and near interface oxide traps can be associated to carbon tails extending from the SiC interface into the oxide due to the interface re-oxidation occurred during the PDAs.

Acknowledgments

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