Impact of Dislocation on Warpage of Thinned 4H-SiC Wafers

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Abstract. In this work the relationship between changes in wafer center bow after thinning process and the wafer morphology has been shown. KOH wet etching allowed the observation and counting of dislocations in 4H-SiC substrate. In deep a correspondence between changes in wafer center bow and the dislocations density of the SiC substrate has been observed. By using a counting software, a relationship between the basal plane dislocations and center bow has also been observed.

Introduction

Wide band-gap semiconductor SiC material can overcome the limitations of Si for high voltage/high power devices due to its high electron mobility, high electron saturation drift velocity and high thermal conductivity. SiC based devices such as diodes and power MOSFET are nowadays a reality in the semiconductor industry and their electrical performances are quite comparable, if not superior for some aspects, with the Si counterpart. For semiconductor application wafer thinning plays an important role on device performances guaranteeing for example strong reduction on ON-Resistance (Ron) on power devices. The thinning process, having SiC material low fracture toughness and extreme brittleness, has to be properly performed in order to achieve high quality and crack-free substrate. Moreover, during the grinding process, the part of the SiC substrate directly in contact with the grinding wheel damages, with cracks and amorphous regions clearly visible by morphological analysis. This part of the substrate can be considered as a film, whose thickness depends on the size of grinding wheel [1], which causes variations on wafer bowing, introducing a compressive stress on the wafer surface [2,3].

In this work we will focus on the study of relationship between SiC wafers which undergoes a thinning process and the defect density (dislocation mainly) [4-5]. Variations on wafer center bow (C-bow) for three different SiC substrate properly selected for defect density has been shown as a function of the defect density. A series of analyses have been carried out to investigate the morphological changes and defectivity of the SiC wafer surface.

Experimental Setup

Commercially available 4H-SiC substrate with 4° off-angle and 350 μm thickness have been used in this experiment. Wafers have been thinned down to 180 μm by performing a mechanical grinding on the C-faces using a conventional in-feed grinding process. Warpage measurements have been performed by E+H MX 102-204-RA-2C tool [6]. Sample surface roughness (Sq) and the peak to valley height line parameter (Rt) have been measured by optical profilometry analysis (MicroXaM). Dislocations have been identified by KOH etching. The etching has been performed in molten KOH inside a nickel crucible at a temperature of 500 °C for a period of 5–10 min. Major dislocations in SiC substrates include threading screw dislocations (TSD), threading edge dislocations (TED), and basal-plane dislocations (BPD). EPD (Etch Pit Density) and BPD etch pits densities have been calculated based on the observation under fully automated (X, Y and Z) optical microscopy (nSPEC by Nanotronics). With a powerful software for the image analysis coupled with high-resolution microscope, a 6 inches wafer map with detailed dislocations count and classification has been obtained [7].

Results and Discussion

Figure 1 shows large area (152 x116 um) optical profilometer analyses performed on SiC C-face before and after grinding process. As received wafers show a quite flat face with a surface roughness (Sq) of about 0.6 nm and a peak to valley height (Rt) of about 3 nm (fig. 1 a)). As a consequence of the thinning process the shape of the surface remarkably changes showing grinding wheel marks, a surface roughness (Sq) of about 4.6 nm and a maximum height of the profile (Rt) of about 29 nm (fig. 1b)). The corresponding morphology in section, investigated by TEM analysis (images not shown), reveals a damaged region with lateral and median cracks extending for a depth of about 600 nm. This damaged region is an area with high density dislocations and large strain [8,9].
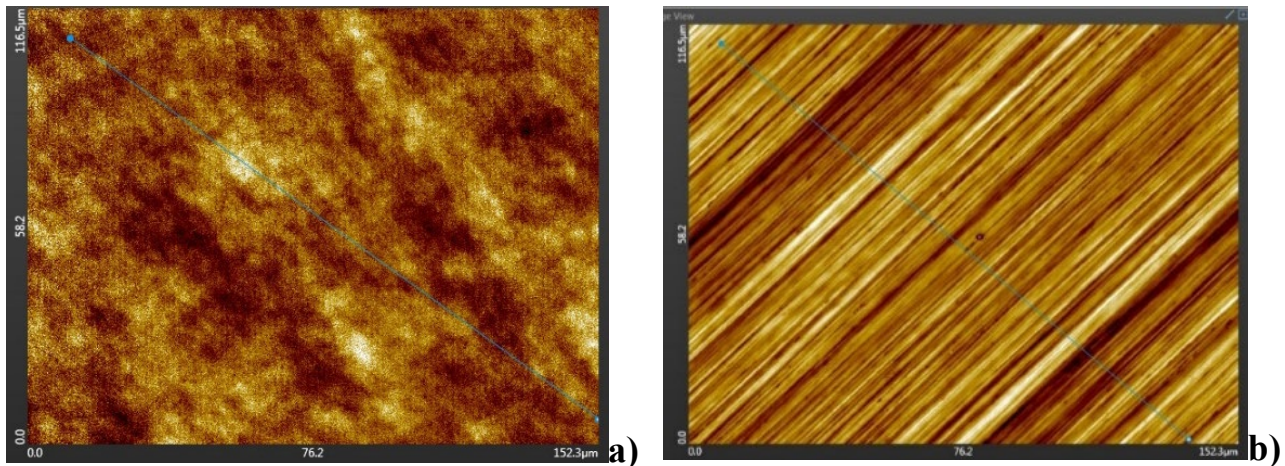
 a) b)

Figure 1. Optical profilometer images of the as received SiC C- face surface a) and grinded surface b)

Despite the same grinding process has been performed on all SiC wafers under investigation, different Cbow values have been measured as it is possible to see from data collected in fig. 2 where Cbow values normalized (N Cbow) to the lowest one, obtained for wafer 1, have been collected. It is to note an increasing by a factor of about 1.6 and 2.4 in Cbow values respectively for wafer 2 and wafer 3. The differences found cannot be accounted for in terms of grinding process variation since the same grinding process has been performed on all wafers and we wonder if a correlation exists among variations in wafer Cbow and wafer defect density (mainly dislocation).
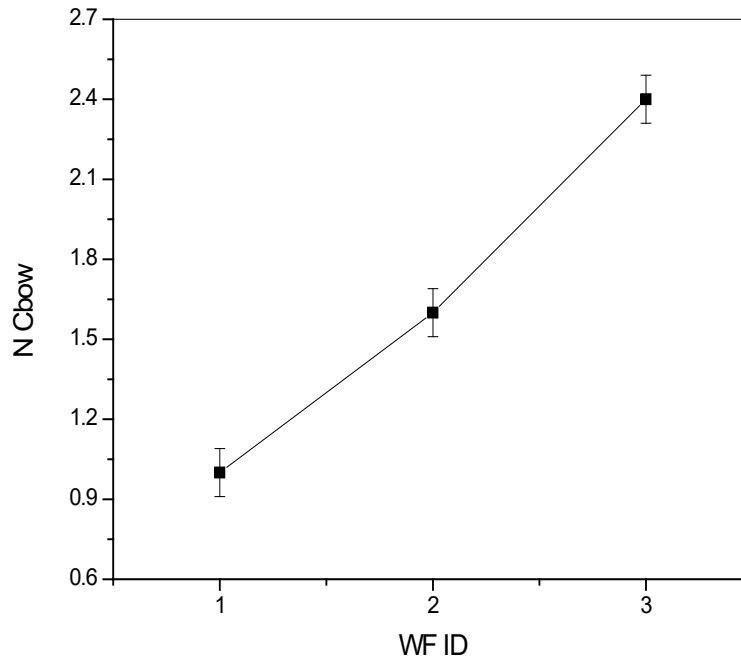
Figure 2. Normalized Cbow (N Cbow) values for wafers under investigation. The Cbow value increase by a factor of 1.6 and 2.4 on wafer 2 and 3 respectively.

Fig. 3 shows the whole defect count maps of wafers 1 and wafer 3 having respectively the lower and higher value of Cbow. With the nspec tool, the high-resolution map (about 14.000 tiles) allows observing with high level of detail the entire wafer, counting the whole Etch Pits Density (EPD) with the possibility to distinguish within all the pits the different type of dislocations (BPD, TSD and TED).
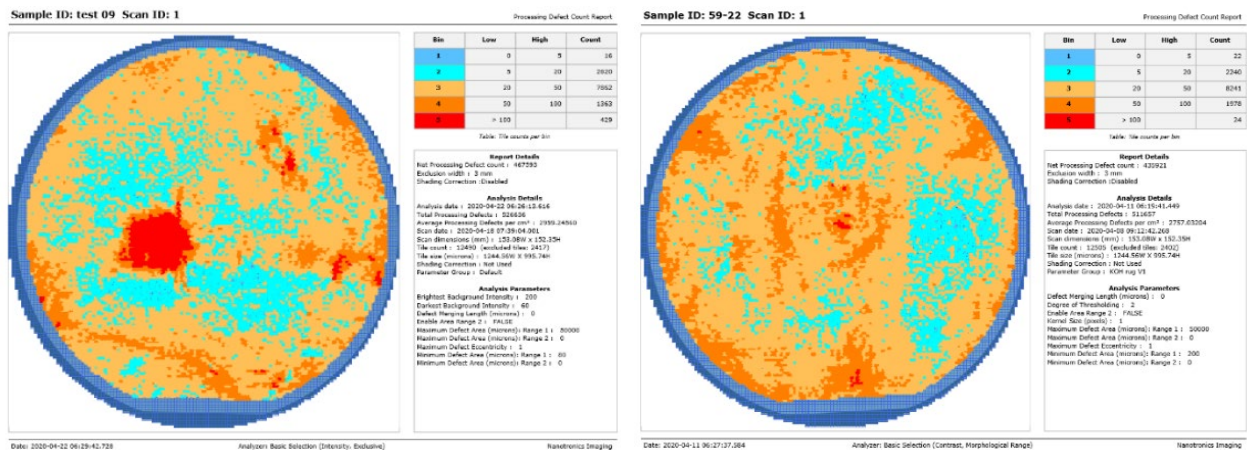

Figure 3. High resolution whole wafer map of the 6 inch. samples with the higher value of dislocation density (left) and lower valuer (right). The EPD density is 3500 ± 200 pits/cm^2 for sample 1 (left) and 2900 ± 100 pits/cm^2 for sample 3 (right). The edge exclusion is 2 mm for both maps.

The EPD density is 3500 ± 200 pits/cm^2 for sample 1 and 2900 ± 100 pits/cm^2 for sample 3. A deep analysis allowed a better classification of dislocation type and the same trend was observed for the basal plane dislocation (BPD) that are between 1900 and 2000 pits/cm^2 for sample 1 and less than 200 pits/cm^2 for sample 3. This means that in sample 1 over than 60% the pits are made by BPD.

In figure 4 the relationship between the Cbow and the etch pits density (EPD) has been reported. From the figure the correspondence between the high value of Cbow and the lower value of dislocation density is clearly observable. The wafer that exhibits the highest wafer bowing (wafer 3) shows also the lowest EPD count.

For energetic reason the defect (mainly dislocation in SiC substrate was observed) is a preferential way to release the internal stress of the wafer after the growth. For this reason the highly defect sample correspond to the lower bended samples and vice versa.
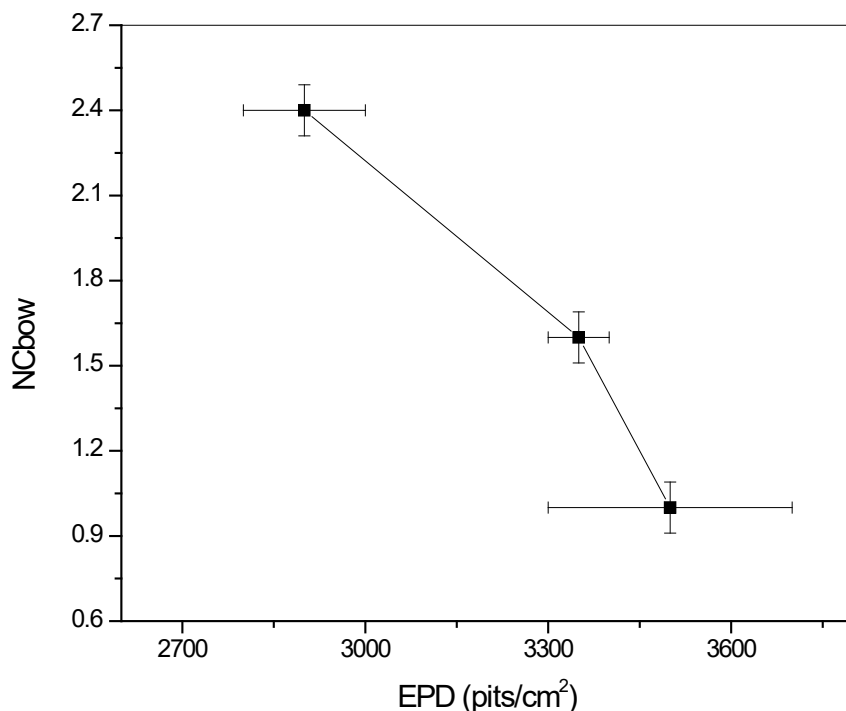

Figure 4. Center bow (Cbow) as a function of Etch pit density (EPD). All the three wafers have been measured after the same thinning process.

Summary

In this work, a different behaviour in terms of wafer Cbow after the thinning process has been reported for the three wafers under investigation. Since the same thinning process has been performed on the three wafers, we investigated whether this finding can be ascribed to different characteristics of the wafers. Indeed we have observed that the three wafers show differences in terms of dislocation density (EPD) with the highest values obtained in correspondence of the lowest wafer bowing measured. In details, a difference was observed also for basal plane dislocation density that is higher in the sample with lower center bow.

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