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Polish Scratch Simulation vs. Polish Tool Type

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Abstract Wafer scratching from handling and processing can impact the performance of devices grown on a substrate. Knowledge of process conditions and modeling of scratches on wafers can be used to elucidate the root cause of scratches so that they can be eliminated.

Introduction

Semiconductor wafers for epitaxy and device manufacture are required to be flat and defect-free within tight manufacturing tolerances. The negative impacts of surface damage on device manufacture are well known [1,2,3]. Wafer processing from a wire sawn wafer may include multiple grinding, lapping, and polishing steps. Ideally each step improves the surface quality of the wafer from the previous processing step.

Of particular concern for a finished wafer is the presence of remnant scratches on the surface. Such scratches can retain residual contamination from processing and can lead to killer defects in initial epitaxy layers. The final CMP (Chemical Mechanical Polishing) step is intended to remove all residual scratching from prior processing steps without creating new scratches [4]. One potential scratch source after CMP is polish removal that was insufficient to eliminate prior scratching. Contaminant particles in the CMP process, potentially introduced by insufficiently cleaned wafers, can also cause random scratches [5]. Finally, the wafer itself can be a source of scratches. Chips of material, usually separated from wafer edges, can cause singular scratches, or become embedded in the polishing pad to cause multiple scratches. In the case of a batch polisher a single such particle can scratch multiple wafers.

Experimental

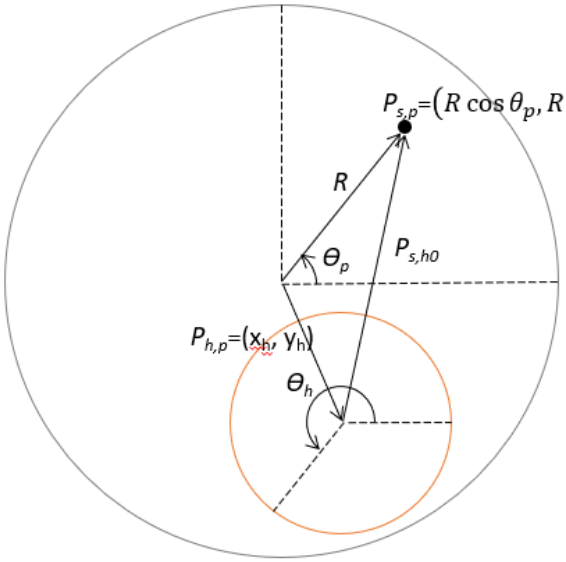
Modeling of scratch patterns from batch and single wafer polish processes was performed using Visual Studio C++ and Microsoft Excel programs. The geometry of the system for a single wafer polisher, is shown in Fig. 1. For the model, the wafer head is considered fixed in space at coordinates x_h,y_h and rotates through angle q_h in unit time. Since the head is rotating, its coordinates also rotate as shown. The scratch source p is fixed on the pad at radius R from the center and rotates through angle q_p as a function of time. With each revolution of the pad, the scratch source moves across the wafer surface describing an arc scratch. Modeling for a batch wafer polisher is the same as for the single wafer polisher except that the coordinate of the wafer has eccentricity from center of the head.

Discussion

Wafering lines can experience “excursions” in which end-of-line wafers exhibit increased defectivity. Often, increased scratch levels due to polishing failures are the issue. With multiple processing steps in the line, modeling of scratch shapes can be a useful tool to identify the problematic step in the process and to help isolate the source of scratch generation.

The shape of a wafer scratch is dependent on several parameters, including platen speed, polish head speed, particle location on the platen, and wafer location for a single wafer polish process. Head oscillation will contribute a known variability to scratch shape. Scratch shape on a batch polisher is

affected by these same factors plus the additional parameter of wafer distance from the center of the polishing head.



$$\overrightarrow{P_{s,p}} = \begin{pmatrix} R\cos\theta_p \\ R\sin\theta_p \end{pmatrix}$$

$$\overrightarrow{P_{h,p}} = \begin{pmatrix} x_h \\ y_h \end{pmatrix}$$

$$\overrightarrow{P_{s,h0}} = \overrightarrow{P_{s,h}} - \overrightarrow{P_{h,p}} = \begin{pmatrix} R\cos\theta_p - x_h \\ R\sin\theta_p - y_h \end{pmatrix}$$

Coordinate system for the polish head.

$$\overrightarrow{P_{s,h}} = \begin{pmatrix} \cos(-\theta_h)\cdot(R\cos\theta_p - x_h) - \sin(-\theta_h)\cdot(R\sin\theta_p - y_h) \\ \sin(-\theta_h)\cdot(R\cos\theta_p - x_h) + \cos(-\theta_h)\cdot(R\sin\theta_p - y_h) \end{pmatrix}$$

Figure 1: Geometry and relative motion of the coordinate system for a single wafer polisher.

Shown in Fig. 2 is a comparison of relative motions for single vs. batch polishers. For both systems, the wafers and the platen turn in the same direction. The batch polisher, however, holds multiple wafers on a single polish head. Fig. 3 demonstrates the change in scratch shape for a particle stuck in a polish pad as a function of relative distance from the center of the platen. As shown, the curvature of a resulting scratch increases with increasing distance from the center of the platen and is higher for the smaller diameter platen.

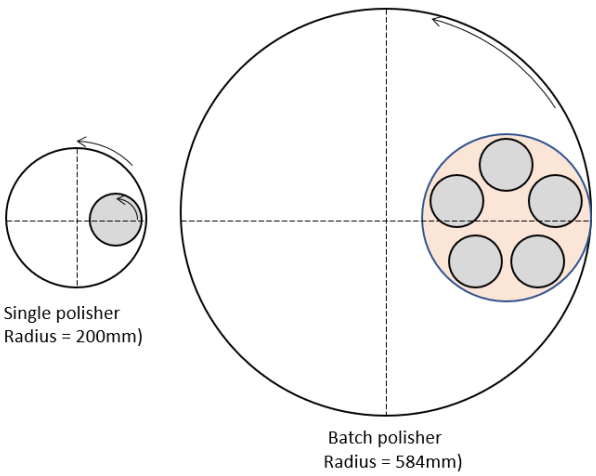


Figure 2: Comparison of polish setup for a batch and single wafer polisher.

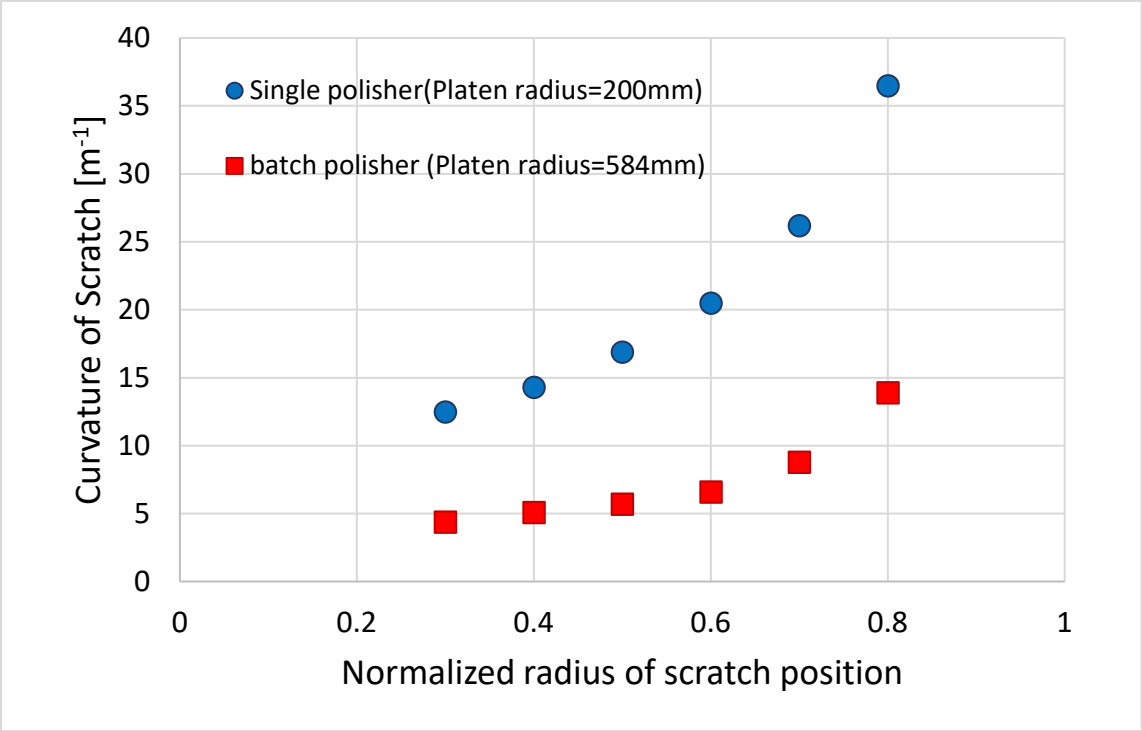


Figure 3: Curvature of a scratch as a function of particle location from the platen center for the batch and single wafer polishers of Fig. 2. Both datasets were obtained using 35 rpm platen and polish head speeds.

For a batch polisher, the number of scratched wafers is further affected by the amount of time the scratch source (particle) is on (or embedded in) a pad. Many scratch events last for less than a single revolution of the platen before the originating particle is flushed off of the pad or into a pad groove (Fig. 4a). When the particle is on the pad for longer times, scratching can be more severe. In the simplest case in which the platen and head rpms are matched, a particle stuck in a pad will produce a single visible scratch regardless of time on the pad. It is difficult to exactly match these speeds, however, and some processes intentionally use different head and platen speeds. In this case, a particle will create a new wafer scratch with each revolution as shown in Fig. 4b. Note that due to the offset in platen speed (40 rpm) and head speed (38 rpm) the long duration event will scratch every wafer in the head. The offset of these scratches is dependent upon the speed and speed differential between the head and platen in the process.

An example of modeling of scratch patterns for a polished wafer is shown in Fig. 5. In this case, light scratching is seen as a series of blue dots on the wafer metrology image in Fig. 5a. Using the tool configuration and polishing parameters, the scratch pattern was modeled in Fig. 5b). Fitting of the model to the data is shown in Fig. 5c. As shown, 5 individual scratches are identified indicating that the scratch source was present on the polish pad for at least 5 revolutions.

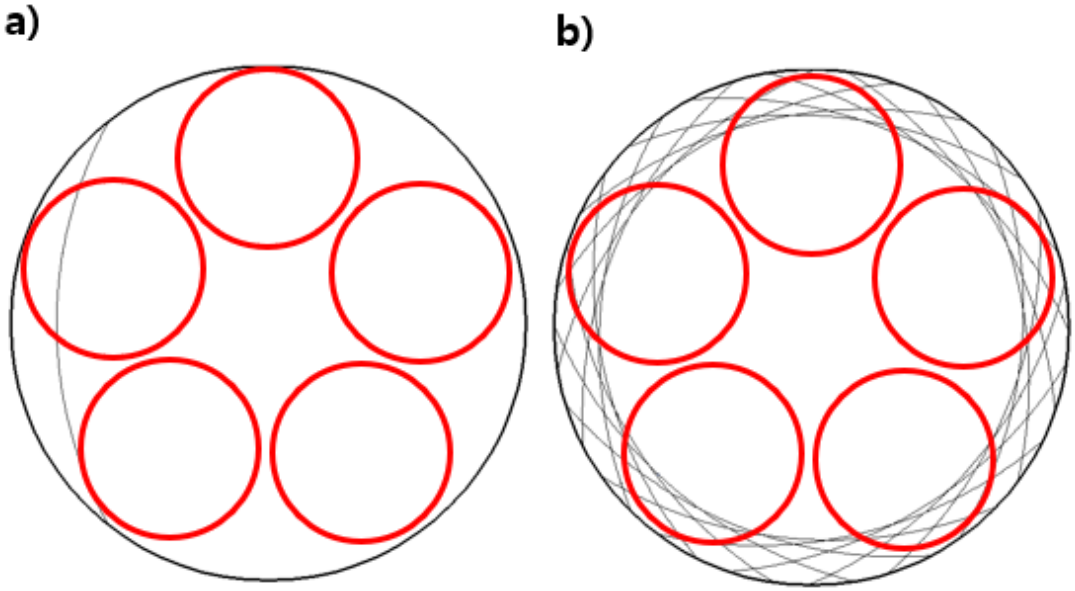


Figure 4: For a batch polish process with 40 rpm platen speed and 38 rpm head speed. a) Polish scratch for particle on the pad for <1 revolution, and: b) Polish scratches for the same particle on the pad for many revolutions.

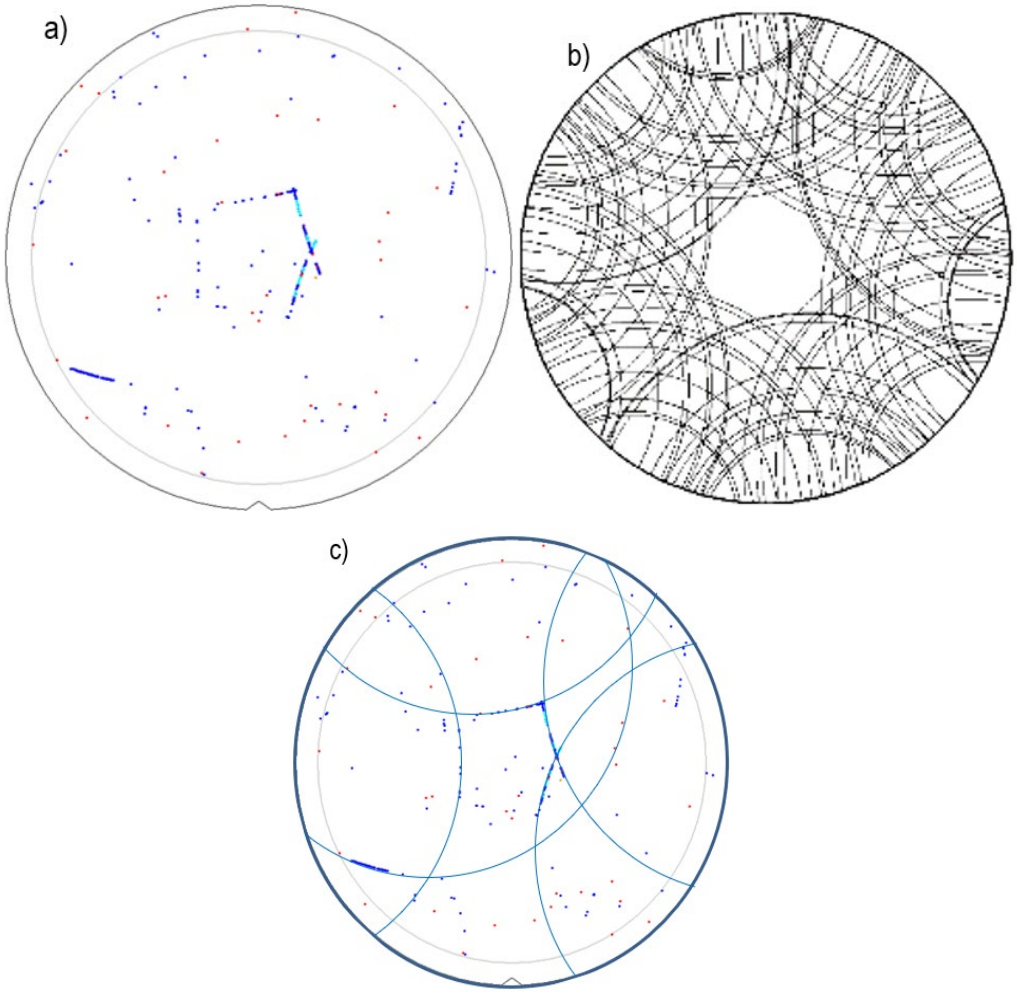


Figure 5: Modeling of a scratched wafer from a single wafer polisher. a) Defect metrology map of scratched wafer: b) Modeled scratch map: c) Alignment of modeled scratches with metrology data.

Conclusions

Scratch defects from polish and lapping processes are dependent upon process configuration and process conditions. Knowing these parameters, the formation of scratches on a wafer can be readily modeled. This modeling and simulation can be used to help determine the location and lifetime of individual scratch sources. For multistep processes, modeling can help identify individual process steps that contribute to scratching events.

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