

Via Size-Dependent Properties of TiAl Ohmic Contacts on 4H-SiC

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Abstract. P-type Ti/Al-based contact vias of different sizes but identical processing were electrically characterized using linear transfer length method (TLM) patterns and metal-oxide-semiconductor (MOS) transistors. While the TLM patterns and MOS transistors with large vias follow ohmic contact behavior, Schottky contact properties were observed for smaller contact via dimensions. Focused ion beam (FIB) analysis of the contact vias verified the presence of Ti₃SiC₂ on large 66 μm x 25 μm contact vias and its absence on smaller 16 μm x 3 μm ones, correlating its absence with the electrical Schottky properties.

Introduction

Limitations for Silicon, e.g. high power or high frequency application and operation in harsh environment such as high temperature, open up the market for high-bandgap materials like silicon carbide (SiC). The 4H polytype is the technologically most mature one, featuring among others high electric field breakdown strength and high thermal conductivity [1].

To optimize SiC technology, it is essential to minimize power loss, e.g. by ensuring a low resistive ohmic contact. Due to its band gap, no natural chemical element allowing a p-type ohmic metal semiconductor interface by reducing the Schottky barrier height to nearly zero exists for SiC. Therefore, metal stacks are traditionally employed in combination with a sintering process, also referred to as silicidation process, to partially overcome this issue [1, 2].

Ti/Al emerged as one of the most prominent p-type stack choices with the ability to form contacts with low contact resistivity due to the formation of the max phase Ti₃SiC₂ at around 1000 °C [1–3]. The presence of Al enhances the Ti₃SiC₂ formation on the 4H-SiC surface, which correlates to a reduction of Schottky barrier height and lower specific contact resistance [1–3].

However, the impact of the contact dimensions has not been researched in detail. Therefore, this work investigates the influence of contact via dimensions of TLM patterns and MOS transistors on Ti/Al-based p-type ohmic contact formation on 4H-SiC.

Sample Fabrication

Samples on 100 mm wafers were fabricated with a 4H-SiC 1 μm double-well CMOS process using 13 different lithography masks [4]. Wells and contact implantations (nplus and pplus) have been realized using room temperature ion implantation and subsequent 1700 °C annealing for 30 min in Ar ambient with a carbon capping layer. A total dose of $5 \cdot 10^{14} \text{ cm}^{-2}$ was implanted in the pplus region, resulting in a plateau within the first 100 nm with a nominal Al surface concentration of around $6 \cdot 10^{19} \text{ cm}^{-3}$. The gate stack consists of 50 nm thermally grown gate oxide that was NO densified at 1300 °C for 30 min and 500 nm polycrystalline silicon (PolySi). Employed contact materials were 50 nm NiAl for n-type and Ti/Al for p-type with 80 nm Ti and 300 nm Al. This nearly 80 at% Al is supposed to be sufficient for successful ohmic contact formation [1, 5].

It has been previously observed, that Al has a strong tendency to diffuse into SiO₂ during contact annealing [3, 6], damaging or even destroying circuits. Hence, spacing between oxide and contact area is essential. An additional design rule was implemented, extending all edges of contact areas by

2 μm , forming the new spacing area structured via dry etching. The original contact vias were patterned inside the spacing area with separate lithography and lift-off steps afterwards. A 2 min annealing step in Ar atmosphere at 980 $^{\circ}\text{C}$ activated the silicidation. Finally, Ti/Al/Ti (50/700/20 nm) was deposited as metallization. The resulting MOS structures are depicted schematically in Fig. 1a).

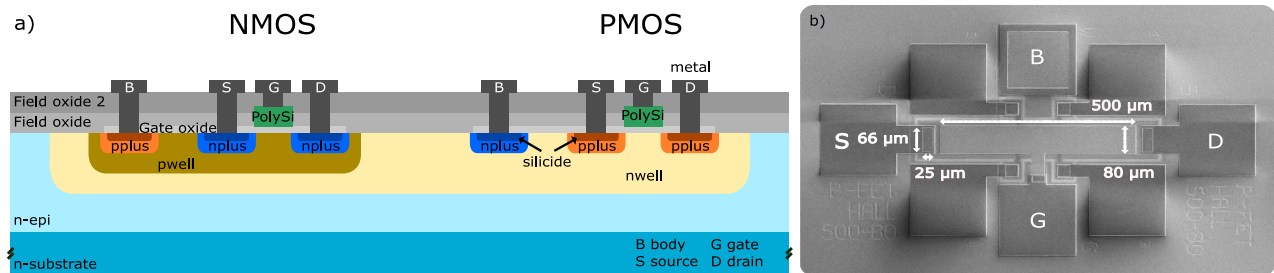


Fig. 1: a) schematic of NMOS and PMOS cross view and b) electron beam image of a PMOS fabricated by IISB with labeled channel and contact via dimensions.

Results and Discussion

In the following, channel length and width of transistors are abbreviated to width in μm - length in μm (e.g. 80-500). Contact via dimensions share the same nomenclature with the first number as the width in μm and the second as the length in μm via (e.g. 66-25), as labeled in Fig. 1b).

TLM patterns and transistors were characterized at room temperature using an Agilent 4156C Precision Semiconductor Parameter Analyzer and a Cascade PA200 probe with a Keithley SCS-4200 measuring unit.

TLM structures were designed and evaluated as described in detail by Schroder [7], consisting of five different evaluation distances, namely 15, 30, 60, 120 and 240 μm , with two metal pads per 100 μm x 100 μm contact via. Measurements were performed with four probes to prevent contact and line resistances of the measuring probes influencing electrical measurements. Table 1 presents the results, namely sheet resistance R_{sh} , contact resistance R_{C} , transfer length L_{T} , contact resistivity ρ_{C} , all including standard deviation (StdDev), and coefficient of determination R^2 .

Table 1: Averaged results of 14 TLM measurements for Ti/Al-based p-type contacts with pplus implantation including wafer level deviation.

R_{sh} [Ω/sq]	StdDev [%]	R_{C} [Ω]	StdDev [%]	L_{T} [μm]	StdDev [%]	ρ_{C} [$\text{m}\Omega\text{cm}^2$]	StdDev [%]	R^2 [-]
23700	2	1370	9	5.8	10	8.0	18	0.999

Contact resistivities between 10^{-5} and $10^{-4} \Omega\text{cm}^2$ have been observed in literature [1, 2, 5, 8, 9], leaving the results one to two orders of magnitude higher, but still showing ohmic contact behavior for all structures evaluated.

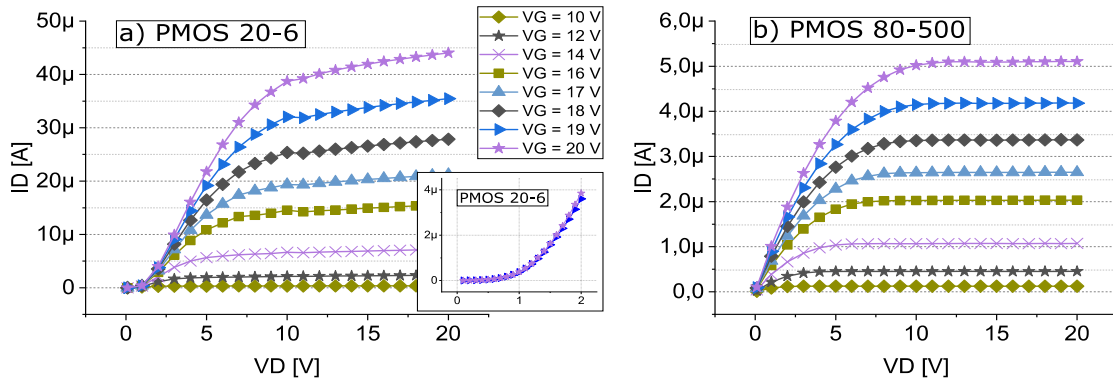


Fig. 2: Output characteristics of a) PMOS 20-6 and b) PMOS 80-500 from a center die. The inset shows a higher resolution of the first 2 V of V_D for V_G s of 19 V and 20 V from the PMOS 20-6.

Similarly to the TLM results, a PMOS 80-500 with a contact via of 66-25 exhibits ohmic output results, depicted in Fig. 2b). However, a PMOS 20-6 with a 16-3 contact via shows Schottky properties, displayed in Fig. 2a), indicated by the nonlinear slope between 0 V and 1.5 V, see inset in Fig. 2. This phenomenon was also observed for PMOS with higher widths having 96-3 and 396-3 contact vias and on devices from other dies and wafers. Due to not having any process variation, it is assumed that the geometries of the contact via contribute to this effect. Therefore, the width can be excluded as a sole cause.

To get behind this effect, contact vias of the electrically characterized transistors were investigated via FIB, presented in Fig. 3, using a Helios G4 PFIB CXe from ThermoFisher Scientific to visualize possible differences in their contact regions. On the 66-25 contact via, a formed Ti_3SiC_2 layer can be identified, indicated by its terrace like 4° off-axis epitaxial growth, as depicted in Fig. 3c) [2, 3]. However, it is not present on the 16-3 via shown in Fig. 3e), which, due to identical processing, correlates the missing Ti_3SiC_2 formation to the different dimensions of the contact via. This also matches the observed electrical properties at the beginning of the output characteristics with the presence or absence of the Ti_3SiC_2 layer.

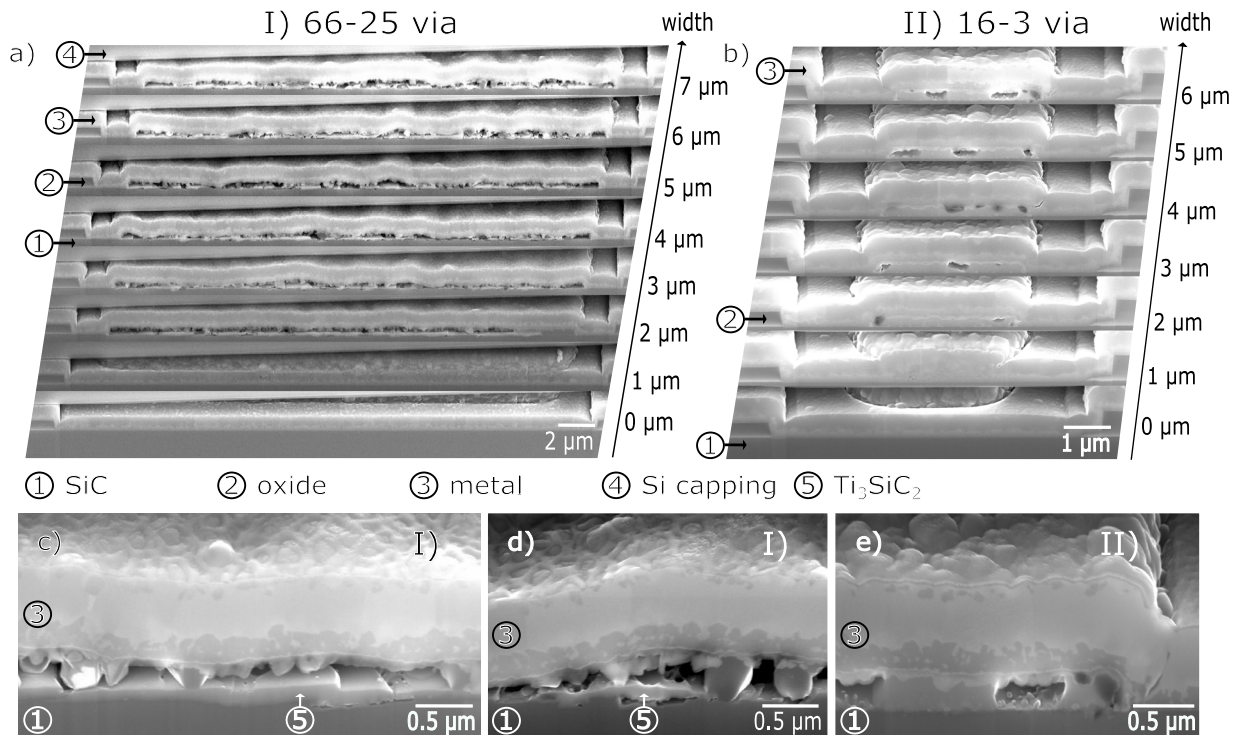


Fig. 3: Tilted SEM images of FIB prepared cross sections of I) 66-25 {a), c) and d)} and II) 16-3 Ti/Al-based contact vias {b) and e)} after finished processing. Multiple cuts across the complete via length, which start in the oxide free spacing area, with 1 μm width distance between them and larger magnifications of the SiC contact interface {c) – e)} are depicted for both via sizes.

Interestingly, the Ti_3SiC_2 layer is not observed to continuously span across the whole contact area, as seen in Fig. 3d), and is additionally not completely connected with the metallization above, resulting in some sort of cavities on the interface. Both effects lead to a smaller than expected effective contact area, also explaining the discrepancies between the TLM results and literature values of the contact resistivity. As verified by FIB, complete coverage and connectivity, which is assumed for the evaluation, is not given. This negatively affects the accuracy of the TLM results.

These cavities are present over the whole 66-25 contact via, while the smaller one has only a few, displayed in Fig. 3a) and 3b). The connections between Ti_3SiC_2 and the metallization appear to be grains with some crystalline character. While not forming Ti_3SiC_2 , other material combinations from the Al-Ti-Si-C quaternary system are present at the 16-3 contact via. Possible materials could be AlTi_3 , Al-12%Si, Al_4C_3 or Ti_5Si_3 [2, 9, 10]. The small grains on the SiC surface of the 16-3 via are assumed to be Al-rich [8]. The reason for the change in morphology indicates differences in the reaction kinetics. This might occur due to varying surface conditions and activation energies or a temperature distribution deviation during the RTP process.

Further investigation using X-ray diffraction and transmission electron microscopy is required to understand the materials at the small contact via. Also, the cavities formed above the Ti_3SiC_2 layer and the critical contact via dimensions remain undetermined and open possibilities for future research.

Summary

The anomaly of Schottky properties on transistors related to small Ti/Al-based contact via dimensions was observed, in contrast to ohmic contact behavior of larger ones. Here, two transistors were investigated via FIB, revealing a formed Ti_3SiC_2 layer at the SiC surface for the larger via and a lack of Ti_3SiC_2 for the smaller via. With identical processing and the design being the only variation, this correlates the missing formation of Ti_3SiC_2 with the electrically observed Schottky properties. Further investigation is required to determine the reactions taking place at the smaller contact via, explain the absence of Ti_3SiC_2 and comprehend the formed cavities above the Ti_3SiC_2 layer.

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