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A Novel Tool Layout and Process for Single Side Wet Electrochemical Processing of Porous Silicon Carbide Layers without Edge Exclusion

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Abstract. In this paper we present a novel tool layout for wet chemical processing of porous silicon carbide layers. The novel tool concept includes single side processing without edge exclusion. There is no need to contact the backside of the wafer. We show SEM cross sections of the porous layer made by different currents densities. With increased current density the porosity increases. After optimization of the process conditions, we achieve a layer thickness non-uniformity of 10%.

Introduction

Silicon carbide (SiC) is the material of choice for next generation power devices in fast growing applications like electromobility and renewable energies. Due to its inertness, SiC cannot be easily structured by wet chemical processes at room temperature. A porous SiC layer can be obtained by wet electrochemical treatment of SiC [1]. The porous SiC layer can be used e.g. for structuring purposes [2] or e.g. as seed layer for the growth of a SiC epitaxial layer with improved properties [3,4].

Tool Description

In this paper, we present a novel tool for SiC wet etching named ACE (Advanced electro-Chemical Etching). It uses a wet electrochemical process to generate a porous SiC layer and allows for the single side processing of SiC substrates. The double-tank electrochemical cell is already well known as state-of-art concept for semiconductor porosification [5]. In this double-tank principle, each side of the wafer is contacted with a separated electrolyte tank system. In one electrolyte tank system the wafer is contacted by the electrolyte and in the other electrolyte tank system the electrochemical porosification process takes place. This conventional set up requires sealing of the wafers which complicates the implantation of the system into a full automatic tool. Moreover, the sealing does not allow to etch the wafer all the way to the edge as required for some applications. In this paper, we demonstrate a new tool concept where only one side of the wafer is contacted with two separated electrolyte tank systems as depicted in figure 1. One main advantage of the novel tool concept is that only one side of the wafer is contacted with chemistry which ensures single side processing. A general view of the tool showing the handling system is shown in figure 2. The wafer is in contact with the electrolyte bath on the bottom side only. It is hold by a simple handling system parallel to the medium surface and positioned over the etching bath. The

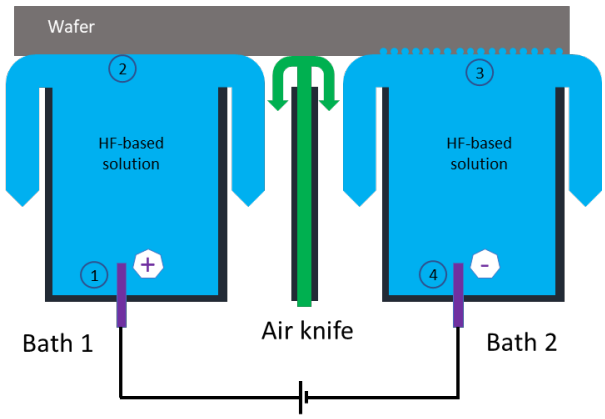

Figure 1: Schematic of the tool principle the numbers refer to the reaction as described in the text

motion and rotation of the wafer allows for a homogeneous full area porosification of the SiC wafer surface without edge exclusion, an important feature not available in most electrochemical setups. The system does not require the wafer to be metallized for contacting and works without the need of complex mechanical handling and sealing.

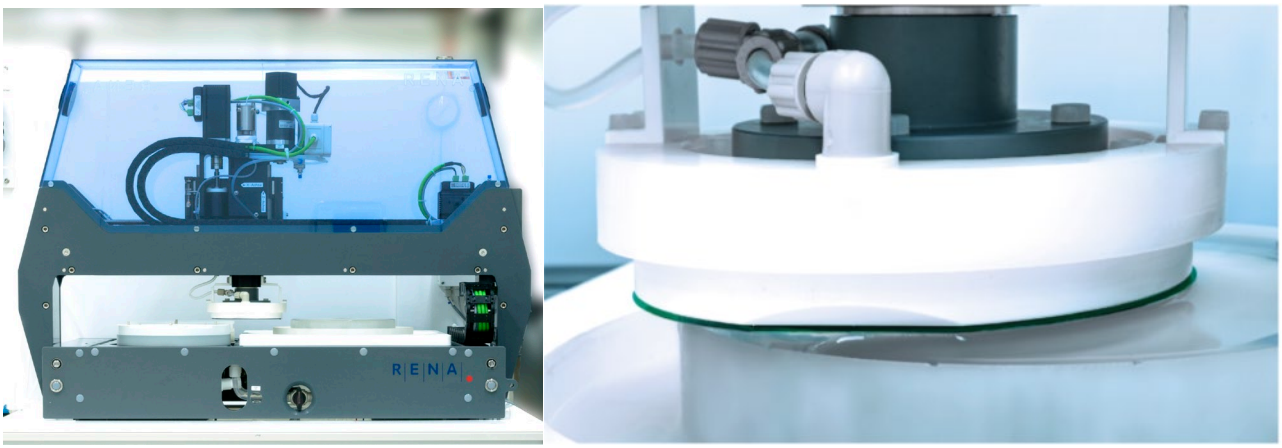

Figure 2: Table top version of advanced electro-chemical etching (ACE) tool.

SiC Porosification

The electrochemical porosification of SiC is a two-step process. In the first step SiC is electrochemically oxidized which is described in Equation 3a and 3b. In the second step, the formed SiO_2 is chemically dissolved which is described in equation 3c. The holes which are needed for the oxidation process are laterally transported through the wafer and generated at the wafer surface in the opposite tank (see equation 2). At the electrodes in each tank, the holes are generated and absorbed to close the electrical circuit (equations 1 and 4).

Electrode Reaction:	$2H_2O + 4h^+ \rightarrow O_2\uparrow + 4H^+$	(1)
Wafer Reaction:	$4H^+ \rightarrow 2H_2 + 4h^+$	(2)
1. Step of SiC Porosification:	$SiC + 3H_2O + 6h^+ \rightarrow SiO_2 + CO + 6H^+$	(3a)
1. Step of SiC Porosification:	$SiC + 4H_2O + 8h^+ \rightarrow SiO_2 + CO_2 + 8H^+$	(3b)
2. Step of SiC Porosification:	$SiO_2 + 6HF \rightarrow H_2SiF_2 + 2H_2O$	(3c)
Electrode Reaction:	$4H^+ \rightarrow 4h^+ + 2H_2\uparrow$	(4)

Experimental Results

The described test setup is used to process 6” SiC wafers. The wafer material is 4H SiC with 4° c-axis tilt. The n-type doped (N) SiC has a resistivity in the range of 12 to 25 mΩ.cm. The wafer thickness is 350µm. A diluted HF based medium is used as etching solution. The current density is determined as the total current over the contact surface between the porosification bath and the wafer and is varied in the range of a few tens of mA/cm². The circulation flow and the distance between wafer and processing bath are optimized for a good wetting of the wafer surface. The porosity of the obtained layer is estimated by using the measured thickness and the weight difference before and after processing.

A first trial with a low current density is performed. The SiC wafer is processed on its full surface for approximately 30 min. A well-defined porous SiC layer is obtained on the wafer surface as can be seen in figure 3. The pore structure is homogenous over the complete porous layer thickness.

A scanning electron microscope picture of the obtained pore structure can be seen in figure 3a and b.

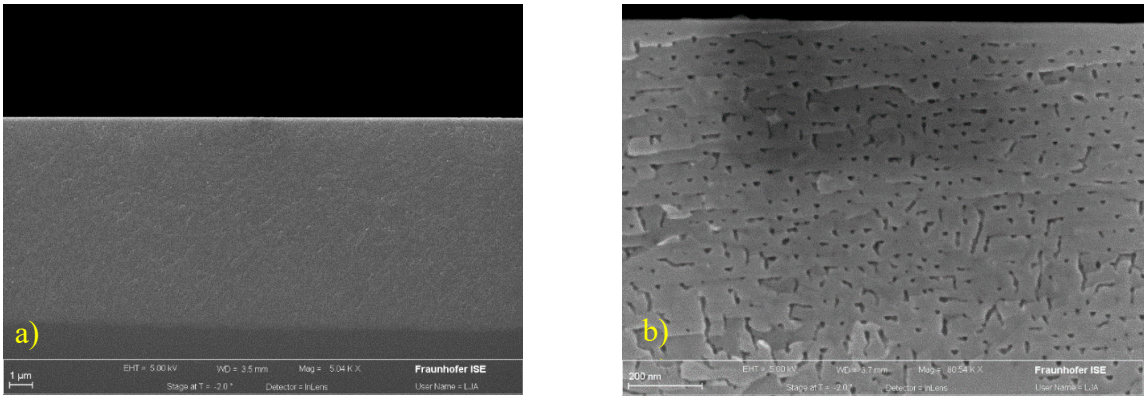

Figure 3: Scanning electron microscope images of the porous SiC layer with a low current density overview a) detailed view from the top of the layer b)

In a further step, we investigate the effect of the current density on the porosity and on the pore structure. Samples with a mid and high current density are prepared and characterized. The pore size gets bigger with increasing current density as it can be seen on figure 4. The porosity is also found to increase with increasing current density. This shows that the porosity of the obtained porous layer can be controlled by adjusting the current density in our test setup.

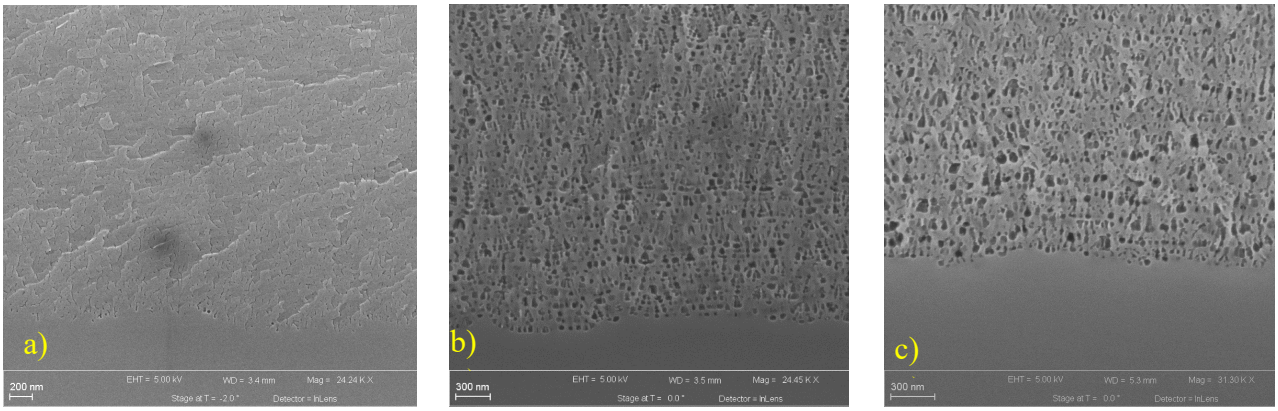

Figure 4: Scanning electron microscope pictures of the obtained porous SiC layer for a) low b) mid and c) high current densities

To investigate the non-uniformity of the etching, the thickness of the porous layer was determined by SEM measurements along the diameter of the wafer. The results are shown in figure 5. The results confirm the capability of the system to etch the wafer all the way to the edge, independently from the process settings. However, an optimization of the parameters was necessary to achieve satisfactory process uniformity. The non-uniformity is calculated as the ratio (max-min)/(max+min).

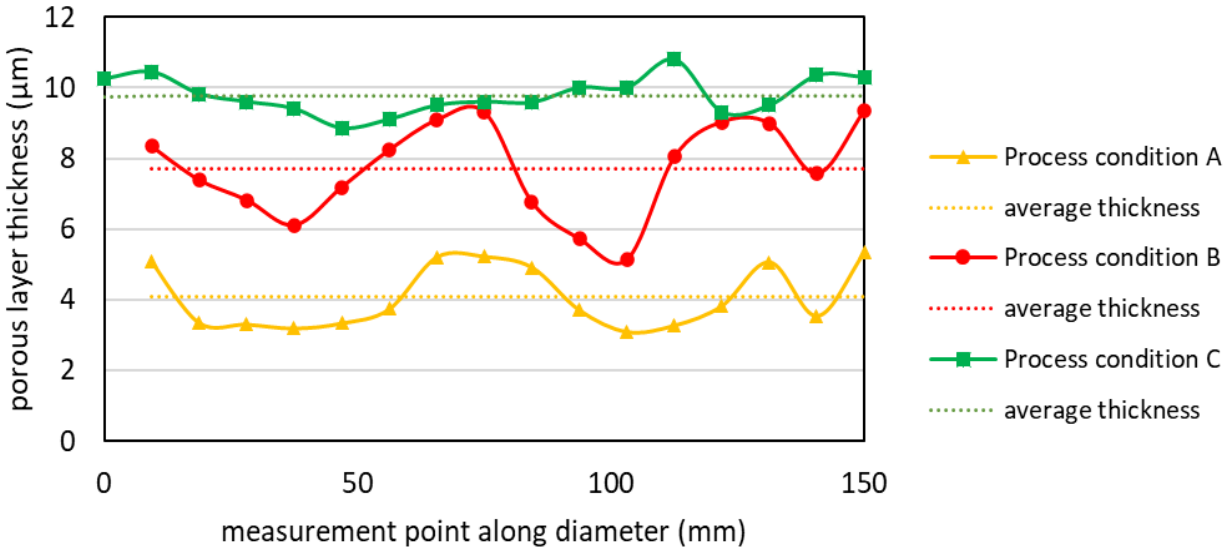

Figure 5: Porous layer thickness of 3 SiC wafers with different process conditions.

In table 1 we have summarized our results. Process condition C results in a significant better layer non-uniformity. We have achieved a very good layer non-uniformity of 10%.

Table 1: Summary of process results

process	average porous layer [µm]	weight loss [mg]	porosification time [min]	porosity [%]	layer non-uniformity [%]
Process condition A	4,08	13,1	30	5,8	27
Process condition B	7,69	38,8	30	9,2	29
Process condition C	9,76	82,8	30	15,4	10

Conclusion and Outlook

In this work, we show a new tool layout for a single-sided electrochemical etching process for SiC substrates. The system does not require the wafer to be metallized for contacting and works without the need of complex mechanical handling and sealing. Initial trials show that this setup allows for porosification of the SiC wafer over its full area without edge exclusion. Typical layer thickness of several µm can be achieved. The porosity of the obtained layer can be varied by varying the applied current density and other process conditions. A low non-uniformity is achieved with optimized process conditions. Further work is ongoing to improve the porosification non-uniformity and removal rate.

This shows the feasibility of such a system for applications where a porous SiC layer is of interest.

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