

Highest Quality and Repeatability for Single Wafer 150mm SiC CMP Designed for High Volume Manufacturing

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Abstract. Silicon Carbide (SiC) provides superior thermal conductivity, high carrier mobility and extreme chemical stability in comparison with those of Silicon (Si). SiC is already showing significant device performance benefits in power devices, communication, and LED lighting. However, SiC presents many challenges for wafer surface treatment due to its high hardness and remarkable chemical inertness.

Today, mechanical polishing techniques on industrial batch CMP tools are the predominant methods for SiC wafer surface treatment, but material removal rate (MRR), surface defects and wafer flatness control are reaching fundamental limits with increasing wafer diameter. Batch processing typically results in a higher amount of surface scratches and defects, higher wafer to wafer variability, and higher wafer breakage rates.

A unique single wafer chemical mechanical polishing (CMP) technique on 150mm n-doped, 4° off-axis, single crystal, 4H-SiC wafers was developed to create a virtually defect-free surface. A polishing head has been designed to manipulate polishing pressures at various zones of the wafer. The removal thickness at each region of wafer surface is modulated and resulting in a highly uniform wafer profile. Additionally, a CMP slurry has been formulated to maximize MRR from 2µm/hr to over 8.5µm/hr.

Scratch-free wafer surfaces are observed with atomic force microscopy (AFM) and bright field (BF) and dark field (DF) inspection techniques. Roughness on the Si face is reduced to below 0.08nm. Total length of surface scratches was reduced to 10mm or less. Industrial metrics of wafer flatness, including total thickness variation (TTV) and local thickness variation (LTV) are modulated and improved. A test run completed on 25-wafers shows an overall 31% improvement of TTV post CMP process.

1. Introduction

Silicon carbide (SiC) devices are superior in higher operating voltages, greater current carrying capacity, high operating frequency, capability of working in higher temperature, greater heat dissipation capability and higher reliability, as compared with those of silicon (Si). SiC has a great potential in the applications of electronic transistors, GaN-based LED, high-temperature energy conversion devices, and sensors that can operate in extremely high temperature and chemically corrosive environments.

SiC devices require a high-quality epitaxial layer which is dependent upon a defect-free substrate surface known as epi-ready surface. Currently, mechanical polishing techniques including lapping and grinding are the predominant methods for the SiC wafer surface treatment. However, a diamond abrasive is often used in these processes which produces surface containing defects and lattice dislocations. ^[1,2] In addition, low material removal rate (MRR) and limited wafer flatness control

extends the process time and affects the yield in mass production. In response to these limitations, we developed a novel chemical mechanical polishing (CMP) technique on 150mm n-doped, 4° off-axis, single crystal, 4H-SiC wafers. The CMP process removes subsurface damage and produce a surface of highest quality and repeatability for the growth of epitaxial SiC.

The material removal rate (MRR) and the quality of finished wafer surface which includes roughness, defectivity and scratches are the two major factors for a SiC CMP process. The slurry has an important impact to both factors. Previous research has been performed to study the abrasive and oxidizer within the slurry and the resultant impact for the SiC substrate surface. Su et al. [3] studied the influencing factors for the material removal rate of 2 inch SiC crystal (0001) Si and (0001) C surfaces. These factors include size and concentration of abrasive alumina (Al_2O_3), pH value, dispersants and oxidants, and process parameters. Yin et al. [4] evaluated the MRR of 4-inch SiC wafers by adding KMnO_4 as strong oxidant in slurry. Increasing the KMnO_4 concentration improved the MRR to a maximum of 1.5 $\mu\text{m/hr}$. Wang et al. [5] developed a two-step CMP process for 4H-SiC substrate, with the maximum MRR of 1.4 $\mu\text{m/hr}$ on Si-face. In conclusion, based upon these studies, the KMnO_4 oxidant and alumina abrasive-based slurry can improve the MRR. However, the reported MRR rates are not efficient enough for scaling SiC CMP product commercialization for larger diameter wafers.

The advantage of single wafer CMP process over batch wafer process lies in the wafer-to-wafer consistency and wafer surface quality. However, the MRR for single wafer CMP must reach greater than 5 $\mu\text{m/hr}$ for substrate production. This requirement is driven by the 1.5 μm Si-face removal target for effective elimination of both surfaces and subsurface damage from incoming grind or lapping.

In addition to MRR demands, wafer flatness control capability is equally essential for a CMP process. A uniform polish from the wafer center to edge is essential to reduce the edge exclusion and improve the total usable area. For SiC CMP, edge exclusion refers to the area around the wafer edge where thickness variation exceeds the specification and cannot be used for device fabrication. The total substrate usable area is increased more than 4% if edge exclusion is minimized from 5mm to 3mm for a 150mm substrate.

2. Experimental

2.1 Study of MRR

In this study, a SiC CMP process is developed for the purpose of ultra-rapid polishing to ensure the process efficiency and improved surface quality. The slurries are acidic solutions containing α -alumina abrasive particles and KMnO_4 as the oxidant. A thermoplastic polyurethane rigid pad with designed concentric and radial grooving at pad surface was utilized. 150mm 4H-SiC wafers were purchased from a commercial substrate supplier. These wafers were polished by Applied Materials Mirra Durum® CMP configured with a membrane polishing head. The polished SiC wafers were post-CMP cleaned in a brush scrubber equipped with an inline spin rinse dryer (SRD). The weight of SiC wafer is measured by an electronic analytical balance. The MRR is calculated by the equation below:

$$MRR = \frac{\Delta M}{C \cdot t}$$
 Here, ΔM is the overall weight removed by CMP process, t is the polishing time in seconds. C is a constant which equals the mass density of SiC multiplied by the surface area of SiC wafer. CMP MRR typically follows Preston's law^[6], which is a linear function of the platen speed and the applied pressure (Fig.1). Three (3) types of slurries exhibit the Prestonian effect. As seen in Figure 1, the Si-face MRR is directly proportional to the platen speed and the applied pressure. The Durum® single wafer polisher can produce $MRR = 8.5\mu\text{m/hr}$. A 6.4 $\mu\text{m/hr}$ MRR demonstrates very low Wafer-To-Wafer Non-Uniformity (WTWNU) throughout a 20-wafer run as shown in Figure 2. This is ideal for high volume manufacturing. The MRR and Ra for both faces is listed in Table 1.

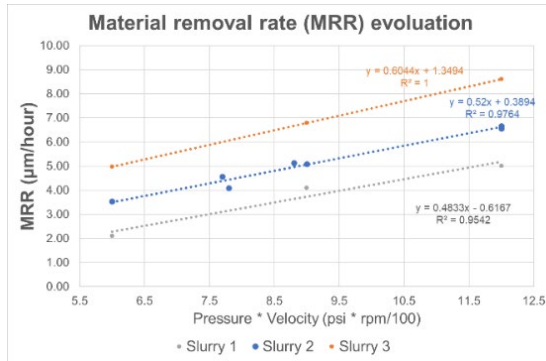


Fig. 1. MRR of Si face CMP as a function of P*V (pressure x velocity) for 3 commercial slurries

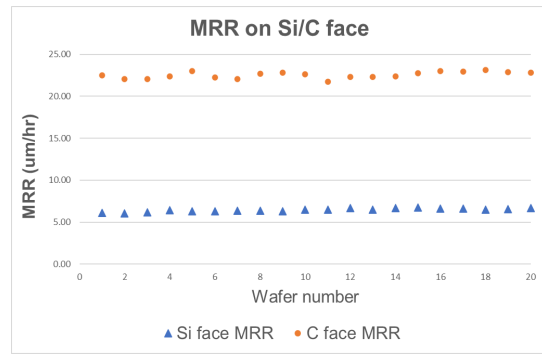


Fig. 2. Excellent MRR repeatability on 20 SiC wafers run. This is ideal for mass production.

Table 1. MRR and Ra for 6.4um/hr polishing process. High removal rate with great surface finish is demonstrated.

	Si face MRR (um/hr)	C face MRR (um/hr)	Si face Ra (nm)	C face Ra (nm)
Bulk polish	6.4	22.5	0.10	0.4

2.2 Study of wafer flatness

Tropel non-contact metrology from Corning Inc. is an industry standard characterization tool for wafer flatness measurement. In this study, wafers are measured on a Tropel before and after the CMP process. The measured parameter changes indicate the impact of CMP process on wafer overall shape. In the SEMI standards, total thickness variation (TTV) is a general indication of overall thickness variation. Local thickness variation (LTV) indicates the thickness variation within a defined local window. In this study, a 10mm x 10mm area is defined as the LTV measuring window. Thus, a 6-inch wafer thickness map consists of 137 windows with a 3mm edge exclusion (EE). As illustrated in Figure 3 (a) and (b), $TTV = a - b$ and $LTV_i = a_i - b_i$ with units in microns.

Experiments were conducted to characterize wafer flatness, which bases upon total amount of thickness removed from both faces. SiC wafers are first polished on C-face with a removed thickness of 2.0um. The wafer is then automatically flipped in the Mirra Durum®. The Si-face CMP follows with a target removal of 1.5um. The wafer thickness profile, TTV, LTV, and linescan plot of wafer thickness across wafer diameter were characterized.

The thickness map profile and LTV distribution before and after CMP are shown in Figure 3. Wafer thickness profile and LTV before CMP process is shown in Figure 3 (c) and (d). This wafer was then polished utilizing a head with single membrane zone, the result exhibits an MRR edge-fast process. After removing 2.0um and 1.5um from the C-face and Si-face respectively, the wafer exhibits a ‘Dome’ shape thickness profile as indicated in Figure 3 (e). Consequently, due to the dramatic thickness change on wafer edge, the LTVs on edge were increased to above 2.0um, as Figure 3 (f). This edge fast removal is also confirmed by the removal thickness map shown in Figure 3(g).

A polishing head has been designed to manipulate polishing pressures at various zones across the wafer. The removal thickness can be modulated at each region on the wafer surface resulting in a highly uniform wafer profile. The new designed polishing head enables adjustment of pressure exerted to the edge of the wafer. Figure 3(h) illustrates the effect of +/- 15% pressure difference on edge zone for the wafer thickness removal profile. Total removed thickness was 2.5um for each wafer (both faces were polished). Compared with the linescan plot of removed thickness of a single zone head CMP process, the uniformity of MRR across wafer diameter has been greatly improved (Figure 3(i)).

In Figure 3 (j) and (k), the wafer thickness profile from the pre-CMP Tropel measurement indicates that the wafer edge area is thicker than the center area. The multi-zone polishing head was adjusted to the thickness distribution map and the wafer was planarized to achieve the flatness uniformity specification. This is shown in Figure 3 (l) and (m).

A set of 25 SiC 150mm wafers were then processed utilizing the new multi-zone polishing head to demonstrate repeatability of the improved post CMP wafer shape. As shown in Figure 3(n), TTV improvement of 31% in average has been achieved.

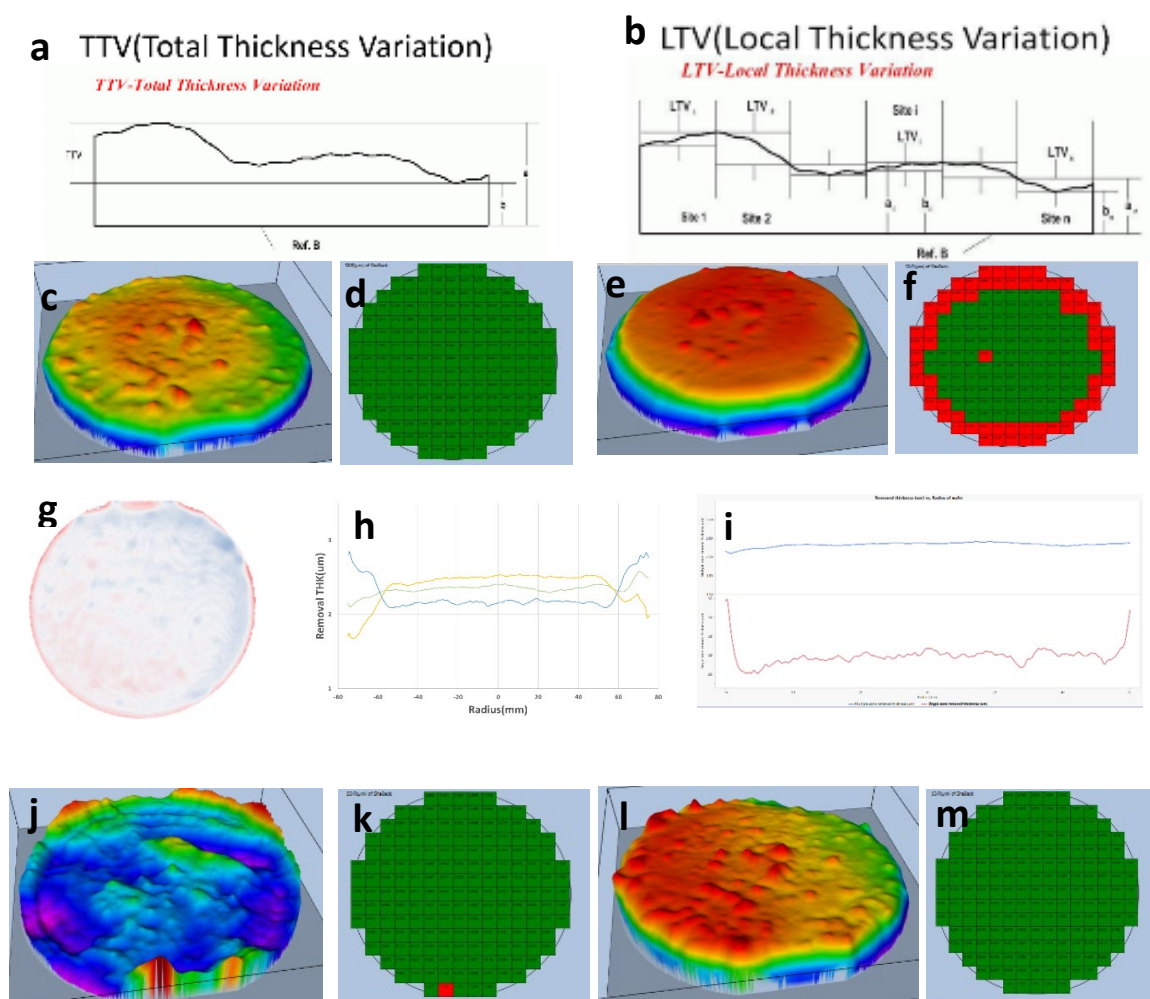
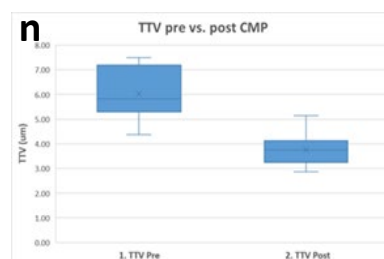


Fig. 3(a)(b). Definition of TTV and LTV, (c)-(f). Wafer thickness profile and LTV distribution comparison for a single zone membrane polishing head. (g). Removed thickness distribution map. Red area indicates larger amount of removal. (h). Illustration of removed thickness linescan for a multizone polishing head. (i) Linescan comparison between single zone and multiple zone polishing head. (j)-(m) Wafer thickness profile and LTV distribution comparison pre and post CMP for a multi-zone polishing head. (n) Post CMP shows 31% improvement in TTV with multizone polishing head for 2.5 μ m of total thickness removal.



2.3 Study of wafer surface roughness and defectivity

The developed CMP process has remarkable tolerance for incoming surface quality. Wafers with different initial surface conditions can be processed and the resulting surface roughness is not relevant. Wafer (30_07) was processed by a rough stock polishing process prior to CMP. Wafer (30_03) was polished by a so-called fine polishing process, as shown in Figure 4 (a)(b). Scratch-free wafer surfaces are observed on both wafers after CMP process. The roughness has been reduced to less than 0.1nm and 0.2nm for Si and C face, respectively, as shown in Figure 4(c). Post-CMP surface roughness remains consistent regardless of starting roughness. Micro-defects on the substrate surface influence SiC epilayer growth quality. Scratch type defects are generated in mechanical treatment

processes prior to CMP, Mirra Durum® single wafer CMP can achieve consistently the lowest levels of scratches and even eliminate scratches.

In this study, a SiC wafer processed by commercially available wafer lapping vendor (mechanical treatment) is compared to wafers polished by Mirra Durum® single wafer CMP. The wafers are characterized in a defect inspection tool by Lasertec. The measured defects are classified and presented in visual format for quantity and type. Bright field and dark field defectivity measurements of the lapping wafer are shown in Figure 4(d). The total scratch length was over 100 mm. Scratches are verified by AFM measurement at specific defect aggregative locations on wafer surface as shown in Figure 4 (e). Another SiC wafer was polished by Mirra Durum® single wafer CMP. Bright field and dark field defectivity measurements and AFM image are shown in Figure 4(f). A set of 10 wafers were measured for post-CMP scratches. As shown in Table 2, the maximum number of scratches is 5/wafer with the maximum total length of 6mm. 5 out of 10 wafers exhibited no scratches.

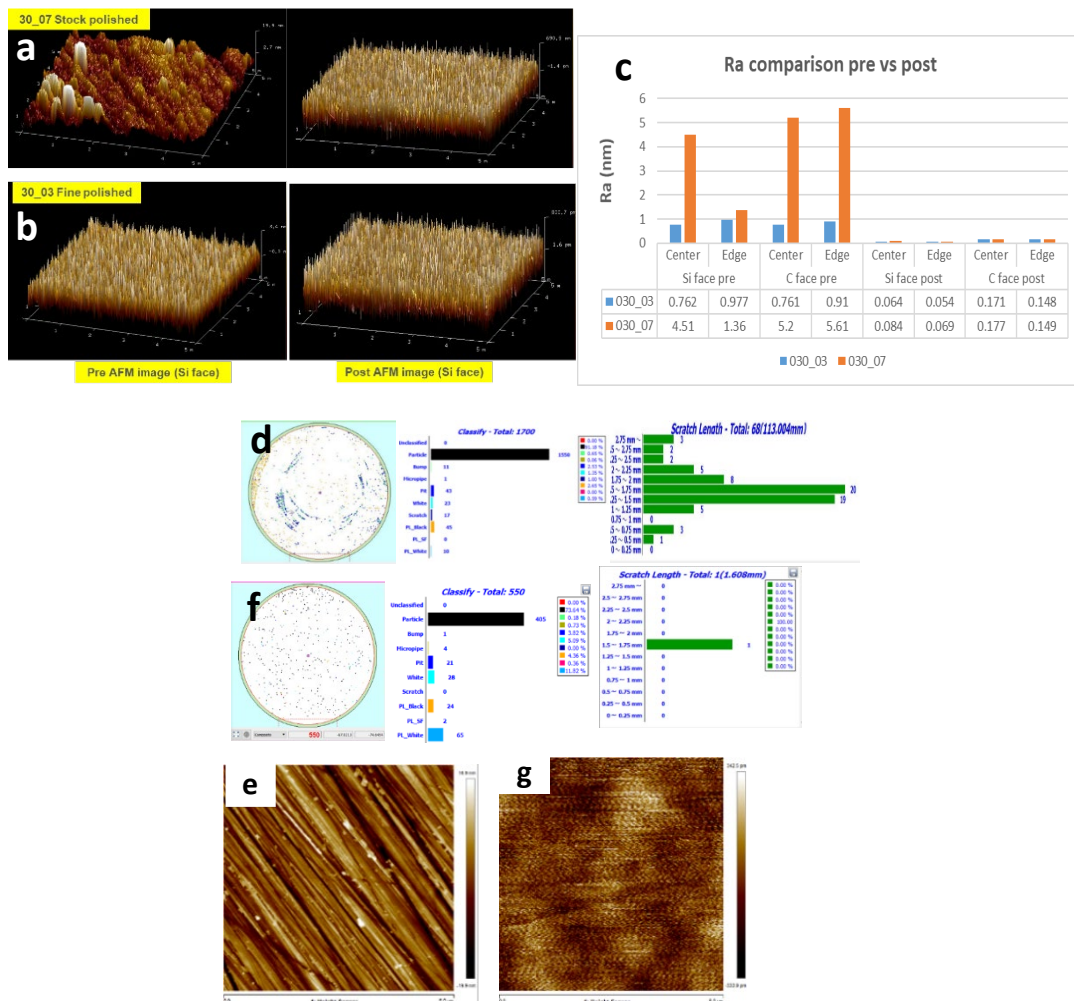


Fig. 4(a)-(b). AFM images of SiC wafers before and after CMP. The incoming surface finish does not affect the post-CMP surface quality. Fig. 4(c). Surface Ra data 0.08nm Si-face and 0.18nm C-face can be achieved. Fig. 4(d)-(e). Post-Lapping defectivity. Significant particle results for bright field and obvious scratching defect of dark field are typical. Fig. 4(f)-(g). Post-CMP defectivity. Very low defect results for bright field and dark field analysis are typical for Mirra Durum® single wafer CMP.

Table 2. Summary of scratches illustrates the excellent surface quality for high volume manufacturing.

Scratch	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10
Length (mm)	1.61	0	0	5.82	0	0	3.31	1.31	0.64	0
Number (#)	1	0	0	5	0	0	2	1	1	0

3. Conclusions

A novel single wafer chemical mechanical polishing (CMP) technique on n-doped, 4° off-axis, single crystal, 4H-SiC substrates wafers was developed. The effects of material removal rate (MRR) and wafer flatness by CMP parameter and polishing head design were investigated. The MRR is 3-4 times more efficient than that of conventional lapping or grinding process and overall wafer shape can be maintained or improved. The surface morphology and defect were studied by atomic force microscopy (AFM). A truly defect-free surface with atomic level surface roughness is achieved. Single wafer SiC CMP by Applied Materials Mirra Durum® demonstrated consistent performance and repeatability. This is ideal for 150mm high volume manufacturing and future substrate scaling.

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