

Evaluation of Defects in a SiC Substrate Using the Photoluminescence Measurement Method

Yoshitaka Nishihara^{1,a*}, Koji Kamei^{1,b}, Daisuke Shiomi^{1,c}
and Kenji Momose^{1,d}

¹SHOWA DENKO K.K., 1505 Shimokagemori, Chichibu, Saitama 369-1893, Japan

^anishihara.yoshitaka.xixlw@showadenko.com, ^bkamei.koji.xheuz@showadenko.com,

^cshiomi.daisuke.xhixv@showadenko.com, ^dmomose.kenji.xhipm@showadenko.com

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Abstract. Photoluminescence (PL) imaging provide defect and dislocation characteristics not only in a 4H silicon carbide (SiC) epilayer but also in a substrate. In this work, to detect a large-pit or a bar-shaped stacking fault (BSF) before epilayer growth, we employed PL under various detection conditions. A large-pit was detected as a dark spot on a 4H-SiC substrate due to dislocations orthogonal to a micropipe. The BSF was clearly observed as a bright rectangle by tuning the observation conditions. The finding indicates that device killing defects or dislocations should be detected as soon as possible and thus improve the yield.

Introduction

Silicon carbide (SiC) is a promising material that can provide high performance power devices owing to its high breakdown field and thermal conductivity. However, various crystal imperfections prevent SiC devices from fulfilling their potential. The impact of such crystal defect has been studied to allow us to understand which defects damage the device yield and reliability. As a result, crystal growth and detecting defects techniques have been developed to reduce the number of defects in an epitaxial wafer. Initially microscopy was used to observe the wafer surface and confirm for defects, however, it is too difficult to detect and classify various defects precisely with this method. Moreover, defects in an epilayer, such as basal plane dislocations (BPDs) and stacking faults, cannot be observed with microscopy.

Photoluminescence (PL) imaging is a powerful tool for detecting extended or in-grown defects in an epilayer [1]. The defects are detected through the energy band of near-infrared (NIR) or near-ultraviolet PL excited by ultraviolet light using a laser or lamp. In recent years, the PL technique has been employed at almost as a mass-production process. Although the defects on a SiC substrate should also be evaluated with PL observation, the method is rarely used because it is easily affected by the impurities included in a SiC crystal [2,3]. In this study, we observed large-pits (others (pits)) or bar-shaped stacking faults (BSFs, propagated stacking faults) [4] before growing an epilayer on the substrate due to using the improved PL measurement method.

Experimental

The samples used in this evaluation were commercially available n-type 4H-SiC (0001) substrates with a 4° off-cut angle toward in the [11-20] direction. These bare wafers were observed with a SICA88 (Lasertec Corp.), which provided confocal microscope images with differential interference contrast (CDIC) and PL. The PL imaging measurement was performed using various filters; the excitation source was extracted from a Hg-Xe lamp through a 313 nm band pass filter (BPF), and the emission from the SiC wafers was cut off with the BPF or a long pass filter (LPF) to allow us to observe the NIR region clearly. After this evaluation, 10 µm thick epilayers doped with nitrogen at $1 \times 10^{16} \text{ cm}^{-3}$ were grown on these substrates by chemical vapor deposition. Subsequently, cross-sectional scanning transmission electron microscopy (STEM) was performed on the epitaxial wafer to reveal the structural features of defects.

One sample was fabricated as a pin diode (PND) to evaluate the expansion of the basal plane dislocation caused by bipolar degradation. To design the PND with an acceptor box profile of $1 \times 10^{18} \text{ cm}^{-3}$, a p^+ -layer was formed by implanting Al ions to a depth of $1 \mu\text{m}$ below the epilayer surface at room temperature with performing the activation annealing at 1800°C for 10 min in Ar. For a package mounted on the PND chip diced at $3 \text{ mm} \times 3 \text{ mm}$, a forward DC was applied for over 1 hour to introduce bipolar degradation.

Results and Discussion

Large-pit Detection. Figures 1(a) and (b) show the CDIC and PL with LPF images of a large-pit detected in an epilayer. Both the pit structure and a bright spot at the same position were observed at the surface of the epilayer. This means that the pit was caused by a micropipe or a threading dislocation along with other dislocations formed in a direction parallel to the basal plane, which was introduced when the SiC substrate passed through the epilayer. Figure 1(c) shows a PL image observed at the same coordinates when using a 420 nm BPF with a PLIS-100 (PHOTON Design Corp.) after applying a direct current of 960 A/cm^2 for 1 hour to a PND fabricated on an epitaxial wafer. This image implies that extended SFs grown from the large-pit in the epilayer also contribute to bipolar degradation and need to be detected in an epitaxial wafer [5].

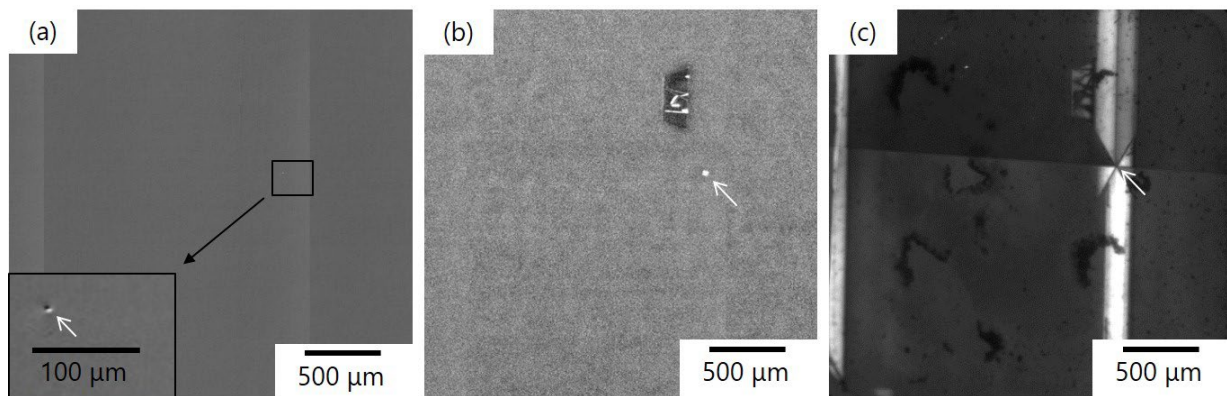


Fig. 1 (a)CDIC and (b)PL with LPF images on an epitaxial wafer. (c)PL in a 420 nm BPF image for the same region after applying DC stress to a PND fabricated using the wafer.

STEM image of a large-pit defect in an epitaxial wafer is shown in Fig. 2. A pit-shaped defect at the surface of the epitaxial wafer and a submicron size micropipe extending from the 4H-SiC substrate to the epilayer are observed; moreover, dislocations formed from the micropipe caused by spreading in the basal plane are also found. This means that the large-pit causes bipolar degradation due to the expanded SFs from the dislocations. Furthermore, BPDs in the epitaxial wafer extended to triangular SFs, however, dislocations with large-pits can form bar-shaped SFs, which cover larger area of the chip than in the former case. Thus, it is preferable that the large-pit is detected before the epilayer is grown.

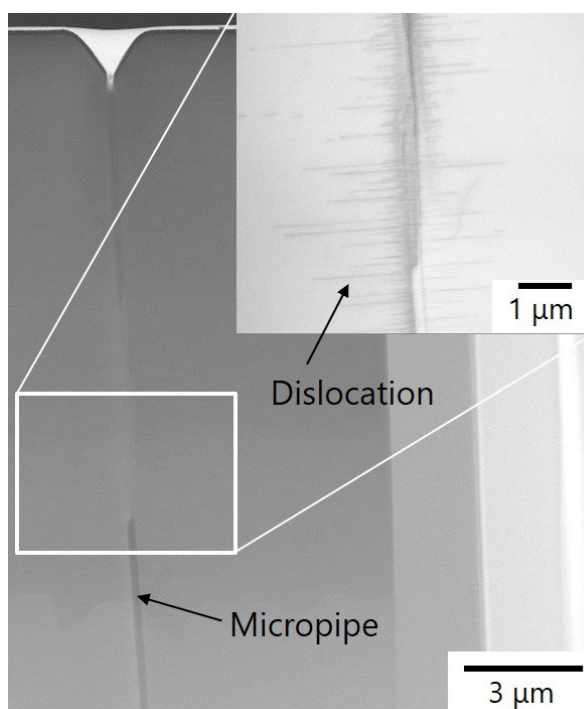


Fig. 2 Cross sectional STEM image of large-pit in a 4H-SiC wafer.

Figure 3 shows CDIC and PL with LPF images of a large-pit detected in a SiC substrate. The pit was found on the surface, which is the same as when it was measured in the epilayer, however, a dark spot was observed due to the different recombination paths in epilayers and substrates [2]. Thus, the large-pit on the substrate could be accurately examined by detecting pits on the surface with dark areas as nonradiative recombination centers in PL images.

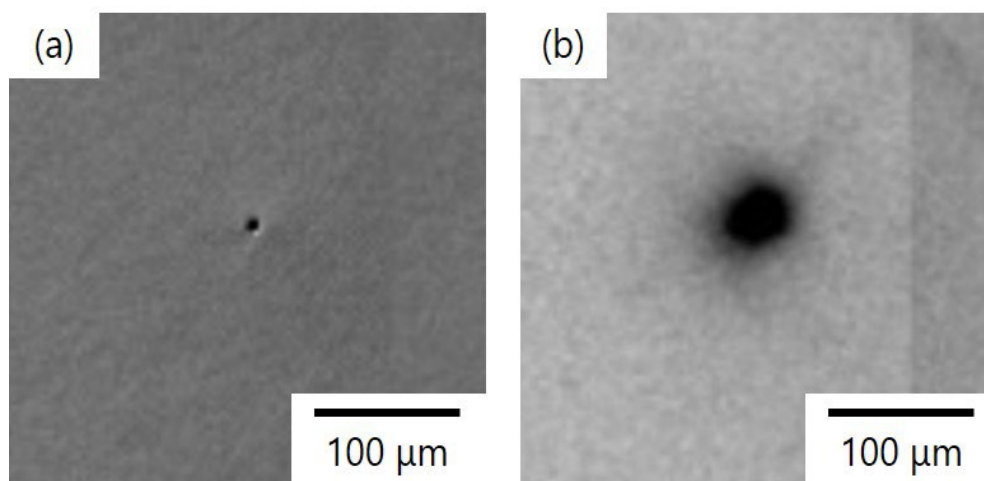


Fig. 3 (a)CDIC and (b)PL images observed on a SiC substrate.

BSF Detection. With other epitaxial wafers, PL imaging was used to detect BSFs, when no structures were found on the surface using CDIC mapping. Figure 4 shows several dark rectangles indicating BSFs that extended into the epilayer from the SiC substrate that were observed by using PL imaging with an LPF. Owing to all the BSFs extending to the epilayer from the SiC substrate, they should be detected before the epilayer is grown in order to reduce the number of fabricated epitaxial wafers that include many BSFs.

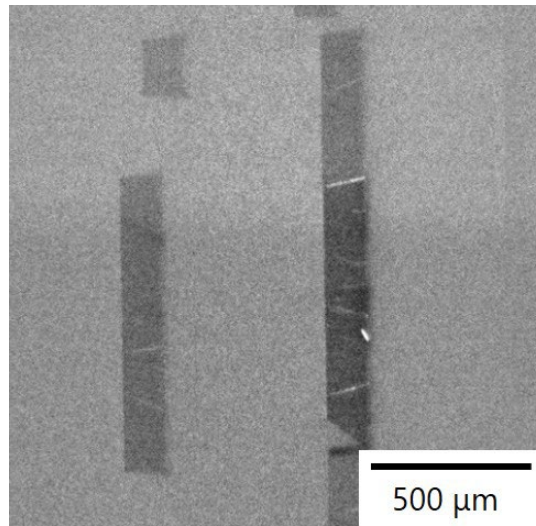


Fig. 4 PL image observed on an epilayer.

Figures 5(a) and (c) show PL images observed with the conventional PL measurement method. BSFs can be found in both images, however, there is a concern that some BSFs may be missed, because one exhibited a very weak contrast with the background and another exhibited a different degree of contrast. These BSFs found as bright contrast (Fig. 5(a)) and dark contrast (Fig. 5(c)) make difficult to detect automatically using various inspection tools. To make it possible to observe BSFs clearly, an improved PL measurement method with choosing suitable detection wavelength using the BPF was employed for the same region, and the results are shown in Figs. 5(b) and (d). The bright area of BSFs observed clearly in both PL images helped us calculate the BSF area or yield and determine whether an epilayer was grown on the substrate.

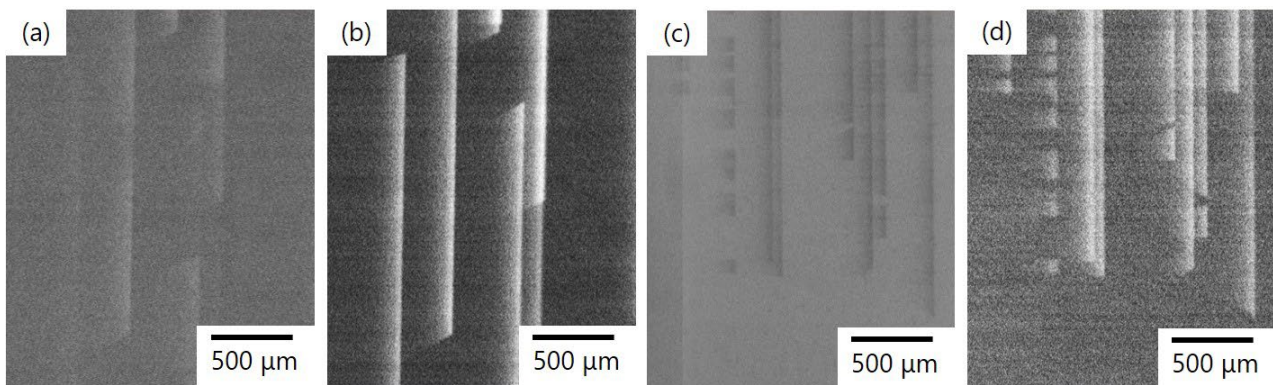


Fig.5 PL images observed same location (a)/(b) and (c)/(d) on a SiC substrate using (a), (c) the conventional measurement method, and (b), (d) the improved method.

Summary

The SiC wafer yield must be increased to reduce the total cost of the SiC device or module so that their use will become more widespread. Therefore, we have to know which wafers were grown the epilayer with priority while considering how many wafers include killer defects such as large-pits or BSFs. This study provides us selection methods for use SiC wafers before epitaxial growth that employ an improved PL evaluation technique.

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