

Observation of Fast Near-Interface Traps in 4H-SiC MOS Capacitors Using Capacitance Voltage Analysis at Cryogenic Temperatures

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Abstract. The inversion channel electron mobility in 4H-SiC MOSFETs with NO annealed gate oxides is still well below its theoretical limit. The physical reason behind the reduced mobility is not yet fully established but has for example been attributed to a high density of very fast interface traps close to the conduction band edge. These traps are not detected by high-low CV analysis at room temperature but are observed by conductance spectroscopy at low temperatures. In this study we demonstrate how conventional high-low CV analysis of MOS capacitors at cryogenic temperatures can be applied to detect and quantify these very fast traps.

Introduction

High power SiC MOSFETs are now commercially available. However, moderate inversion channel mobility has inhibited the development of low power devices (300 – 650 V) where the channel resistance is adversely affecting the power efficiency. The limited mobility is commonly attributed to large density of carbon-related interface defects [1-3].

Compared to the SiO₂/Si interface, the SiC/SiO₂ interface contains a rather high density of interface traps as well as near-interface traps that are located 1-2 nm inside the gate oxide. Currently the most successful method to neutralize these traps is to use post annealing in N₂O or pure NO at high temperatures (1150 – 1350°C) [4-7]. This process is able to suppress the density of interface traps by an order of magnitude with energy levels located 0.1-0.5 eV below the SiC conduction band edge as revealed by CV analysis [6]. However, the inversion channel mobility is still only about 25-35 cm²/Vs which suggests that there are still some interface defects hampering the electron mobility that cannot be detected at room temperature [7].

Recent studies using conductance spectroscopy at cryogenic temperatures have observed very fast interface traps labelled NI, that are detected both in dry thermal oxides and nitrided oxides [8-10]. Subsequent studies have showed that the NI signal is due to direct tunnelling in and out of near-interface traps located very close to the SiC conduction band edge [8]. Here we demonstrate that the NI traps are observed at cryogenic temperatures using conventional high-low CV analysis.

Experimental

In this study we use dry thermal oxide and dry oxide annealed in pure NO grown on 4° off-axis n-epitaxial 4H-SiC with a net doping of $\sim 10^{16} \text{ cm}^{-3}$. MOS capacitors were made with aluminium as the gate metal. The dry oxide (32 nm) was grown at 1240°C for 40 min. The NO annealed oxide (41 nm) was made by dry oxidation at 1250°C for 60 min followed by annealing in pure NO for 60 min at 1250°C.

Measurements were performed in a closed loop helium cryostat that is controlled using Lakeshore 331 temperature controller. Capacitance measurements were carried out using Agilent E4980A LRC meter and Keithley 6517B electrometer at fixed temperatures between 50 K and 300 K. High frequency measurements (1 kHz – 1 MHz) were conducted by sweeping the samples from -10 V to 10 V DC, using 10 mV AC test signal. Quasi static measurements were performed by sweeping the samples from -10 V to 10 V with 0.5 V/s ramp measuring the charge and the capacitance is calculated.

Results and Discussion

Figure 1 shows capacitance sweeps of both samples using quasi-static and high frequency signals at room temperature, 125 K and 75 K. Fig.1.a of the dry oxide sample at room temperature shows significant frequency dispersion, whereas the dispersion in the NO sample is much smaller (Fig.1.d). This well-known difference in the NO sample has been attributed to lower density of slow interface traps (labelled OX) with energy levels within the SiC bandgap [9]. At 125 K, a large portion of the slow traps in the dry oxide sample do not follow the high frequency signal, resulting in a stretch-out in accumulation due to electron trapping as seen in Fig.1.b [11]. As expected, this stretch-out is not observed in the NO sample due to the lack of OX traps, but frequency dispersion appears (Fig.1.e). At 75 K, a significant stretch-out in accumulation is observed in the dry oxide sample and the dispersion is enhanced (Fig.1.c) while a clear frequency dispersion is observed in the NO sample but no stretch-out in accumulation (Fig.1.f). Due to the stretch-out in the dry oxide sample the higher frequency curves asymptotically reach the accumulation capacitance at higher voltages (not shown). The dispersion starts in weak depletion at a similar surface potential as the NI signal is observed by

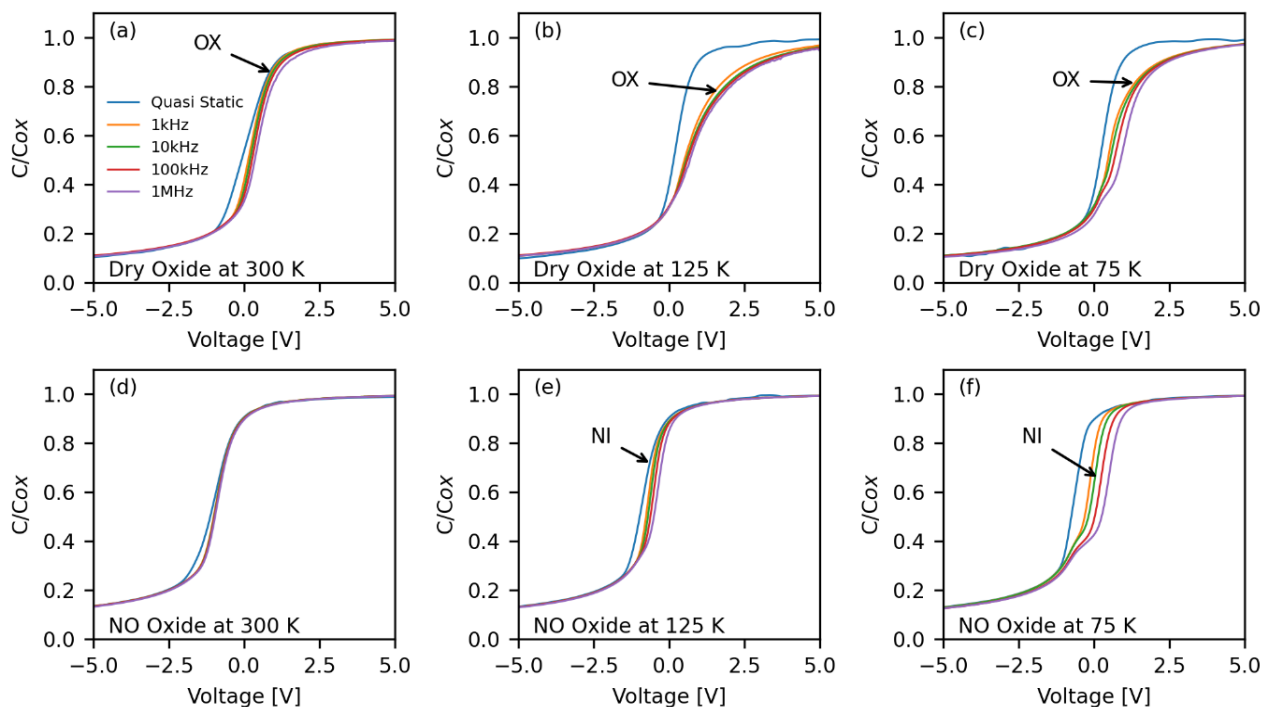


Fig. 1. Quasi-static and high frequency capacitance spectra of both samples at room temperature, 125 K and 75 K.

conductance spectroscopy [10]. At the onset of dispersion, the capacitance is at first influenced by traps that are responding near the test frequency and contribute to the capacitance. Then when the gate bias is increased further, the electron capture rate exceeds the test frequency and the traps remain filled and do not influence the CV curve. The dispersion behaviour versus voltage at 75 K is similar in both samples. Overall, the data suggests that the dispersion at 75 K is due to the NI traps [10]. It is evident that some of the NI traps have electron emission rate that is temperature dependent. The kink that is visible in weak depletion in figures 1 (c), (e) and (f) is assigned to the onset of electron trapping in NI traps.

For comparison, CV and conductance analysis was performed on sodium-enhanced oxides (SEO) samples. MOSFETs using such oxides exhibit about three times higher inversion channel mobility than NO annealed devices [12]. Neither the OX nor NI traps were observed in both types of measurements within the detection limit (not shown). This further indicates that the CV dispersion at low temperatures is due to NI traps.

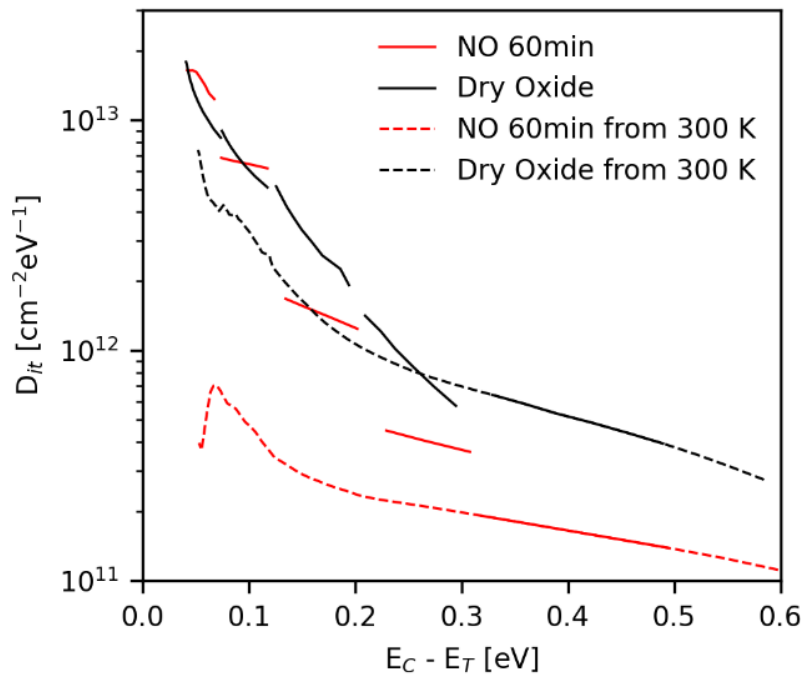


Fig. 2. Density of interface traps of both samples extracted from room temperature data (dashed lines) and at cryogenic temperatures (solid lines).

Figure 2 shows density of interface traps (D_{it}) from high-low CV analysis of both samples. The dashed lines show the D_{it} if only room temperature data is used and extended over a large energy range. The energy range extraction is based on thermal emission and using an electron capture cross section of $1.5 \times 10^{-15} \text{ cm}^2$. At low temperatures when the near-interface NI trap is the main contribution to the D_{it} such approach is not physically correct [10,12]. However, such simplification is justified when comparing relative differences in D_{it} between different gate oxides containing the NI trap. Solid lines show the D_{it} extracted using CV data at different temperatures, using a limited energy range for each temperature. The figure shows that using room temperature data results in an underestimation of D_{it} close to the conduction band edge, especially for the NO sample. At cryogenic temperatures, the NO sample shows similar or higher D_{it} than the dry oxide due the presence of a high density of NI traps that are too fast to be detected at room temperature. Measuring only at room temperature severely underestimates the density of traps closer to the conduction band edge. In addition, one should keep in mind that substantial surface potential fluctuations (the order of 100 mV) are present

at the SiC/SiO₂ interface [13,14] which makes definitive energy level localization of the interface traps questionable. Nevertheless we can compare the extracted D_{it} from the cryogenic capacitance measurements for differently prepared gate oxides. Similar trend can be seen from the conductance spectroscopy analysis where the D_{it} of the NI peak increases as we probe closer to the conduction band edge [9]. The CV analysis provides the total number of D_{it} (the sum of NI and OX traps) while the conductance spectroscopy can separate between the NI and OX traps. The high density of NI traps in NO annealed samples suggests that they are the main cause of limited inversion channel electron mobility in SiC MOSFETs.

Summary

Very fast near-interface traps (NI) are observed in 4H-SiC MOS capacitors using high-low CV analysis at cryogenic temperatures in both dry oxides and NO annealed oxides. Comparison between differently prepared gate oxides suggests that electron trapping and scattering due to these traps is responsible for the rather low inversion channel electron mobility in NO annealed SiC MOSFETs.

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