

## Depth-Resolved Study of the SiO<sub>2</sub>-SiC Interface Using Low-Energy Muon Spin Rotation Spectroscopy

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**Keywords:** Muon spin rotation spectroscopy, thermal oxidation, post-oxidation annealing, interface defects.

**Abstract.** In this work, the interface between 4H-SiC and thermally grown SiO<sub>2</sub> is studied using low energy muon spin rotation (LE-μSR) spectroscopy. Samples oxidized at 1300 °C were annealed in NO or Ar ambience and the effect of the ambience and the annealing temperature on the near interface region is studied in a depth resolved manner. NO-annealing is expected to passivate the defects, resulting in reduction of interface traps, which is confirmed by electrical characterization. Introduction of N during annealing to the SiC matrix results in a thin, carrier- rich region close to the interface leading to an increase in the diamagnetic asymmetry. Annealing in an inert environment (Ar) seems to have much less impact on the electrical signal, however, the μSR signal shows a reduced paramagnetic asymmetry, indicating a narrow region of low mobility at the interface.

### Introduction

The interface between SiC and thermally grown SiO<sub>2</sub> has large number of interface defects, resulting in low channel mobility and limited device performance. Although NO-annealing has shown to reduce the density of interface states ( $D_{it}$ ), the resulting changes at the interface and the interplay between N and the SiC crystal are not completely understood [1,2]. Low energy muon spin rotation (LE-μSR) spectroscopy is a powerful tool to study thin films and multi-layered structures. The implanted positive muons ( $\mu^+$ ) act as local probes in the material and enable the extraction of electrical information about the sample in a depth-resolved manner. Herein, we study the effect of thermal oxidation and post-oxidation annealing on the interface of the grown oxide and 4H-SiC using LE- μSR.

### Working Principle of μSR

The μSR measurements were performed at the low-energy muon (LEM) facility at the Paul Scherrer Institute (PSI), Switzerland [3]. During the experiment, the implanted  $\mu^+$  has the possibility to bind with an electron ( $e^-$ ) in the semiconductor and form a neutral hydrogen-like paramagnetic state known as Muonium ( $Mu^0$ ). In regions with large carrier concentration,  $Mu^0$  can capture an electron to form  $Mu^-$  or capture a hole to form  $Mu^+$ . Both  $Mu^+$  and  $Mu^-$  are referred to as the diamagnetic states. The paramagnetic and diamagnetic states can be distinguished by their different muon spin precession frequencies in an externally applied magnetic field. The recorded decay asymmetries (diamagnetic:  $A_D$ , paramagnetic:  $A_{Mu}$ ) and the calculated diamagnetic fraction ( $F_D$ ) provide information about the local environment of the implanted  $\mu^+$ .

At LEM,  $\mu^+$  with tunable energy between 1-30 keV are implanted at mean depths between  $\sim 10$  nm and  $\sim 200$  nm. During slowing down, the  $\mu^+$  produces an ionization track of  $e^-$ . Below a few keV, the  $\mu^+$  does not generate  $e^-$  by ionization but loses energy by charge-exchange processes [4]. If the  $\mu^+$  leaves the charge-exchange regime as neutral  $Mu^0$ , it is known as '*prompt Muonium*'. If the  $\mu^+$  does not form  $Mu^0$  and the final charge state of the muon is positive, it can capture an electron from its ionization track and form what is known as '*delayed Muonium*' [5]. Therefore, in order for the delayed  $Mu^0$  to be formed, the electron at the end of the ionization track has to travel to the  $\mu^+$  under the influence of its electric field. The time taken by the electron to reach the  $\mu^+$  depends on the distance traveled and its mobility in that nanoscale of the semiconductor. Therefore, for a low-doped semiconductor and at low temperature where the only available electrons for delayed  $Mu^0$  formation are from the muons' ionization track, a measure of  $Mu^0$  asymmetry ( $A_{Mu}$ ) is directly proportional to the mobility of electrons around the implantation depth of  $\mu^+$  in the semiconductor [6]. Further details on the measurement procedure are described elsewhere [7].

## Experimental Details

We study n-type, 4H-SiC samples having a 30  $\mu m$  thick epitaxial layer, and a doping density (Nitrogen) of  $2.8 \times 10^{15} \text{ cm}^{-3}$ . Thermal oxidation was performed at 1300 °C in  $O_2$  atmosphere and the samples underwent a post-oxidation anneal (POA) in NO and Ar atmosphere at 1300 °C for 70 minutes. A thin layer of  $SiO_2$  was deposited on top of the thermal oxide using PECVD to reach a total thickness of 100 nm, such that the distance between the surface and the  $SiO_2$ -SiC interface is equivalent for the three samples. An overview of the sample processing parameters is presented in Table 1.

## Results and Discussion

Fig. 1(a) shows the diamagnetic asymmetry measured. At 10 K, the  $Mu^0$  is expected to stay in the neutral charge state, due to lack of free carriers to form  $Mu^+/Mu^-$ . Therefore, the  $A_D$  recorded is similar across the three samples and independent of the POA. The paramagnetic signal as seen in Fig. 1(b) indicates the ease for the last ionization track electron to reach the implanted  $\mu^+$  to form delayed  $Mu^0$ . The paramagnetic asymmetry recorded for the NO-annealed sample is very close to the non-annealed sample indicating that for the two samples, the mobility of electrons perpendicular to the  $SiO_2$ -SiC interface is similar. However, the Ar-annealed sample has a smaller  $A_{Mu}$  indicating a hindrance to the carriers flow in the first 20 nm, beyond which the  $Mu^0$  signal for the three samples is similar. This suggests that the annealing at 1300 °C in Ar ambience affects the first 20 nm of the semiconductor. The  $A_{Mu}$  recorded for the Ar and NO-annealed samples also show that  $Mu^0$  formation is suppressed in the thermal  $SiO_2$  layer.  $A_{Mu}$  rises sharply as the SiC region of the sample is reached, showing clearly that the  $\mu SR$  signal is very sensitive to the  $SiO_2$ -SiC interface.

Table 1. Description of sample processing steps and resulting oxide layer thicknesses.

Name	Thermal $SiO_2$ thickness [nm]	Post-oxidation anneal (POA)	PECVD $SiO_2$ thickness [nm]
1300x	48	Not annealed	52
1300NO1300	56	NO at 1300 °C for 70 minutes.	44
1300Ar1300	48	Ar at 1300 °C for 70 minutes.	52

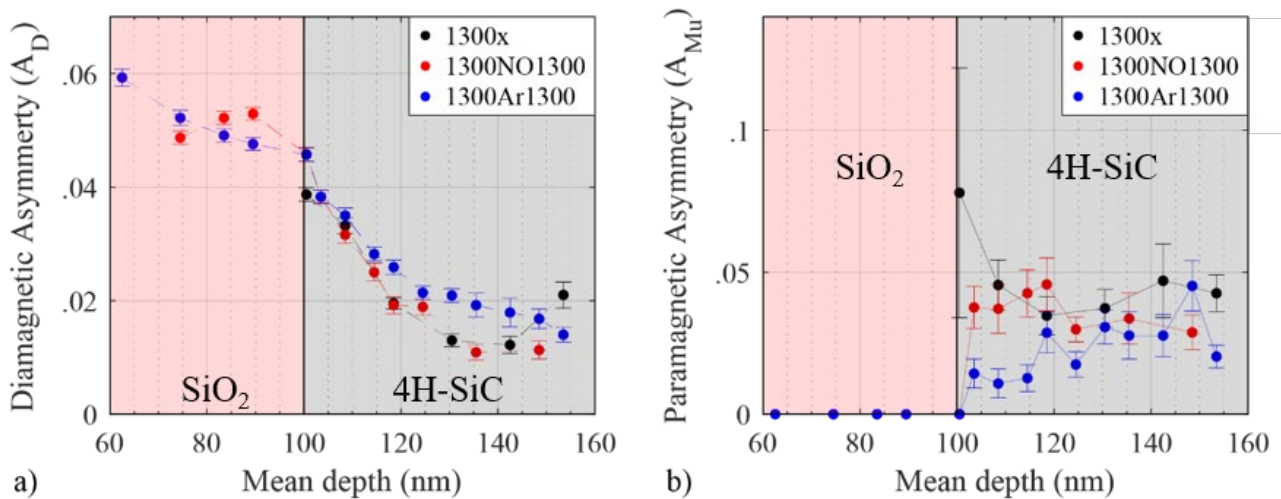


Figure 1:  $\mu$ SR data recorded at  $T = 10$  K and  $B = 0.5$  mT. (a) At low temperatures, due to freeze out of carriers, the  $\text{Mu}^-$  formation is suppressed and  $A_D$  is similar for the three samples. (b) The  $A_{Mu}$  signal indicates a higher mobility in the NO-annealed sample when compared to the Ar-annealed sample in the first  $\sim 20$  nm of SiC.

The experiments performed at 260 K and 0.5 mT (Fig. 2) show again a drop in the  $A_D$  signals for the non-annealed and the Ar-annealed sample, reaching quickly the bulk level [8]. However, the Ar-annealed sample exhibits a slightly smaller  $A_D$  signal,  $\sim 20$  nm into SiC from the interface compared to the non-annealed sample. The drop in diamagnetic signal is likely due to the reduction in carrier concentration. This argument is also supported by an increase in the  $A_{Mu}$  signal for the Ar-annealed sample compared to the non-annealed sample beyond 20 nm into the SiC. In contrast, the NO-annealed sample has a much higher  $A_D$  signal compared to the non-annealed and Ar-annealed samples. The  $A_{Mu}$  signal for the NO-annealed sample is almost zero whereas it is significantly higher for the other two. Low  $A_{Mu}$ , together with the increased  $A_D$  suggests a region of large carrier concentration, which supports the formation of  $\text{Mu}^-$ .

The three samples were characterized electrically and the results of the capacitance-voltage (CV) measurements are shown in Fig. 3 a). Annealing in an Ar environment has very little effect on  $D_{it}$ , whereas with NO-annealing, the  $D_{it}$  is reduced significantly as shown in Fig 3 b). It has been suggested that the silicon vacancies ( $V_{Si}$ ) are formed during thermal oxidation by the emission of silicon, contributing to the large  $D_{it}$  at the SiO<sub>2</sub>-SiC interface [9]. Recently,  $\mu$ SR was shown to be sensitive to the presence of  $V_{Si}$  in 4H-SiC, with  $V_{Si}$  enhancing the formation of  $\text{Mu}^0$ , resulting in the reduction of the  $A_D$  [8]. In our experiment, nitrogen, released during NO-annealing, could passivate the  $D_{it}$  and more specifically  $V_{Si}$ , explaining the increase of  $A_D$ . The N on the substitutional Si site could act as a donor and result in a region of large carrier concentration. The  $A_D$  for the 1300NO1300 sample gradually reduces as we move farther away from the interface due to a decreasing N-concentration in the SiC. This trend suggests that the  $A_D$  for the NO-annealed sample would merge with that of the non-annealed sample beyond 70-80 nm into the SiC.

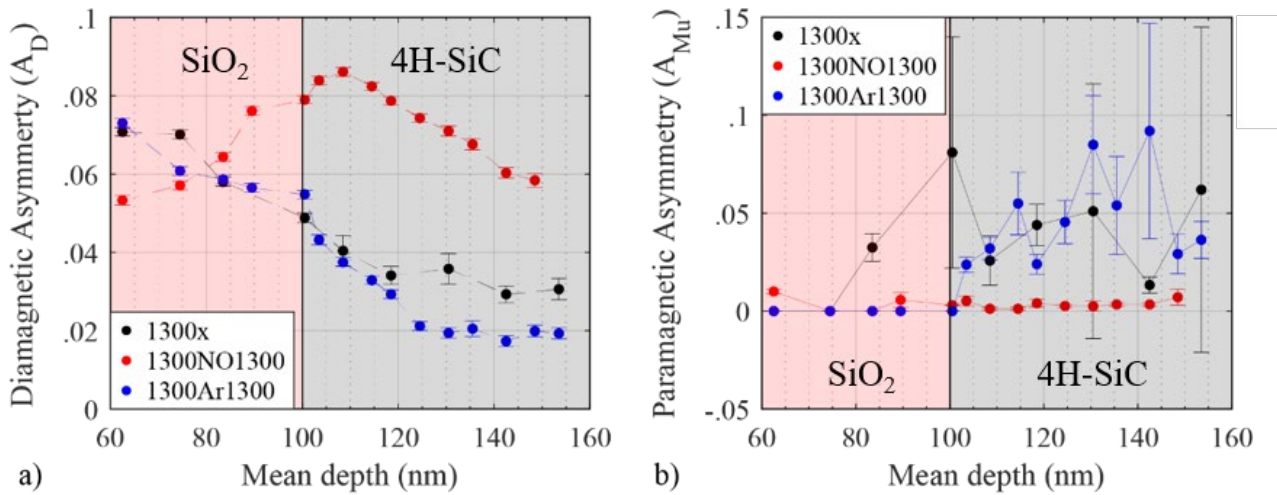


Figure 2:  $\mu$ SR data recorded at 260 K and 0.5 mT. (a). The  $A_D$  for the NO-annealed sample is significantly higher than Ar and non-annealed samples. (b)  $A_{Mu}$  for the NO-annealed sample is suppressed, whereas it is significantly higher for the other two samples.

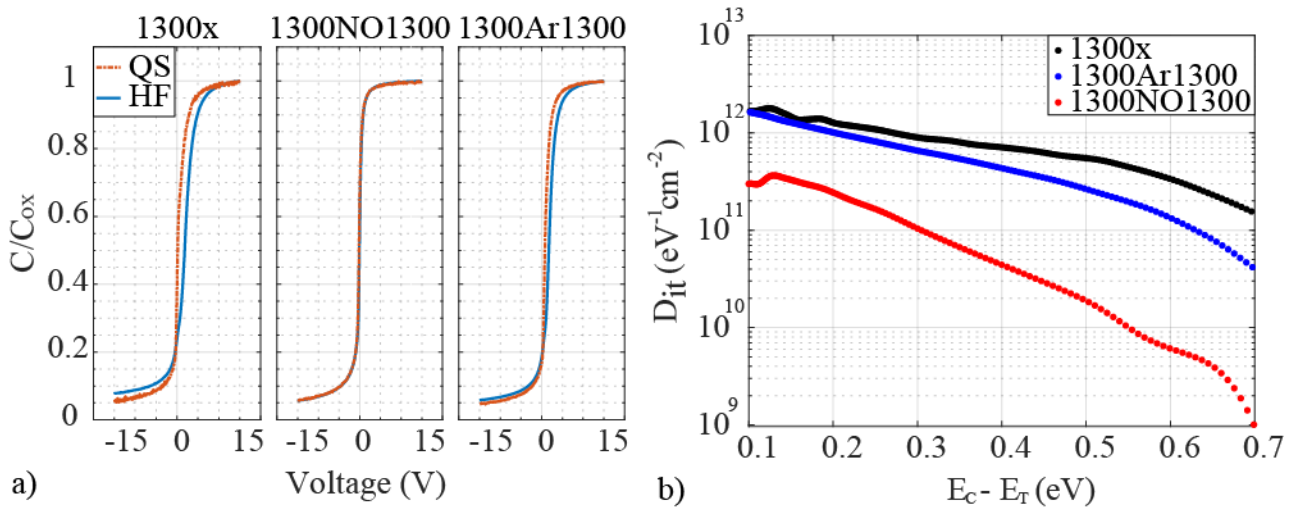


Figure 3: a) Quasi-static (QS) and high frequency (HF) measurement for the three samples. b)  $D_{it}$  calculated using quasi-static and high-frequency capacitance measurements. The  $D_{it}$  for the NO-annealed sample is significantly smaller than for the Ar and non-annealed samples.

## Summary

The effect of oxidation and annealing on 4H-SiC has been studied with LE- $\mu$ SR. NO-annealing results in a region of high carrier concentration near the interface extending up to 70 nm into the SiC region but no appreciable effect on the carrier transport is observed, when compared to the non-annealed sample. Ar annealing has a very slight effect on the  $D_{it}$  (confirmed by CV measurements) and on the  $A_D$  signals. However, a reduction in  $A_{Mu}$  is observed which could suggest a narrow interface region ( $\sim 20$  nm) of reduced mobility.

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