

The Improved Reliability Performance of Post-Deposition Annealed ALD-SiO₂

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Abstract. A systematic capacitance-voltage (C-V) and time-dependent dielectric breakdown (TDDB) study on silicon carbide (SiC) metal-oxide-semiconductor capacitors (MOSCAPs) that use silicon dioxide (SiO₂) is shown in this paper. Oxides were formed using atomic layer deposition (ALD), low-pressure chemical vapour deposition (LPCVD) or direct thermal growth in nitrous oxide (N₂O) ambient, where both deposited oxides were post-deposition annealed in N₂O ambient, too. The electrical characterisation results reveal that the ALD-deposited and N₂O-annealed oxides show the best capacitance-voltage (C-V) characteristics, with flatband and hysteresis voltages (V_{FB}) averaging 1.44 V and 0.41 V, respectively. When measuring the leakage current levels at 175°C, the ALD-deposited MOSCAPs' breakdown electric fields are averaging similar to their counterparts at 9.71 MV/cm. MOSCAPs which utilized ALD-deposited SiO₂ also showed 29% and 345% increased average injected charge-to 63% failure (Q_{BD,63%}) at 9 MV/cm and 9.6 MV/cm, respectively, when comparing these devices to their direct thermally grown SiO₂ counterparts.

Introduction

Reliability aspects in 4H-silicon carbide (4H-SiC) gate dielectrics, such as an insulator lifetime, threshold voltage (V_{TH}) stability and high leakage currents, remain an issue of paramount importance, which hamper the further development of 4H-SiC power MOSFETs [1]. Most of the SiO₂/SiC interface problems, such as carbon clusters, hydrogen (H) and oxygen (O) vacancies, are directly related to the thermal oxidation process [2] and can be bypassed by using deposition processes. Among deposition techniques, atomic layer deposition (ALD) offers specific advantages, such as very low deposition temperature, excellent process control [3] and suitability for conformal deposition of gate oxides in trench structures [4]. Deposition of oxide layers is then usually followed by a post-deposition anneal (PDA) in a nitrogen-containing ambient [5], such as nitrous oxide (N₂O) or nitric oxide (NO) [2], to overcome the as-deposited layer's poor electrical quality.

In this investigation, we present the excellent reliability performance of ALD-deposited SiO₂ layers on SiC, specifically time-dependent dielectric breakdown (TDDB) characterisation of metal-oxide-semiconductor capacitors (MOSCAPs). The results will be shown for N₂O post-deposition annealed samples. Here, the distribution of interface parameters, as well as the results from TDDB, will be investigated as metrics of improvement following the PDA process. For benchmarking, processes will be compared to LPCVD-deposited devices, which have undergone the same PDA, and direct thermally grown oxides [5], to demonstrate the superior process quality.

Experimental

The active 10 μm thick epitaxial layer of $4 \times 10^{15} \text{ cm}^{-3}$ n-type doping was grown in house on 100 mm diameter, 4° off-axis 4H-SiC wafers. Growth was performed using a 30 $\mu\text{m/hr}$ growth rate and nitrogen (N_2) as a dopant, in an LPE ACiS M8 chemical vapour deposition (CVD) reactor. After an initial clean, a 1 μm thick field oxide was deposited and a window was opened via photolithography and reactive ion etching (RIE). Then, quarter wafers underwent one of the three oxidation routines: 1. SiO_2 plasma deposition at 200°C using bis(diethylamino)silane (BDEAS) and O_2 plasma precursors in an Ultratech Fiji G2 Plasma-Enhanced ALD system. 2. SiO_2 deposition at 750°C using tetraethyl orthosilicate (TEOS) as a precursor in a Thermco LPCVD system. 3. Direct thermal growth of SiO_2 in a HiTech furnace at 1300°C for 5 hrs in N_2O ambient. Samples from the first two routines then underwent a PDA in the HiTech furnace, in N_2O at 1300°C for 2 hrs. All oxidation measurements resulted in oxide thicknesses between 50 and 60 nm, which were verified using cross-sectional transmission electron microscopy (TEM) measurements. Finally, 500 nm aluminium (Al) backside contacts were deposited, before a 1 μm Al layer was deposited on the topside of the samples by means of a liftoff process. A cross-sectional diagram of the fabricated final device structure is shown in Fig. 1 (a).

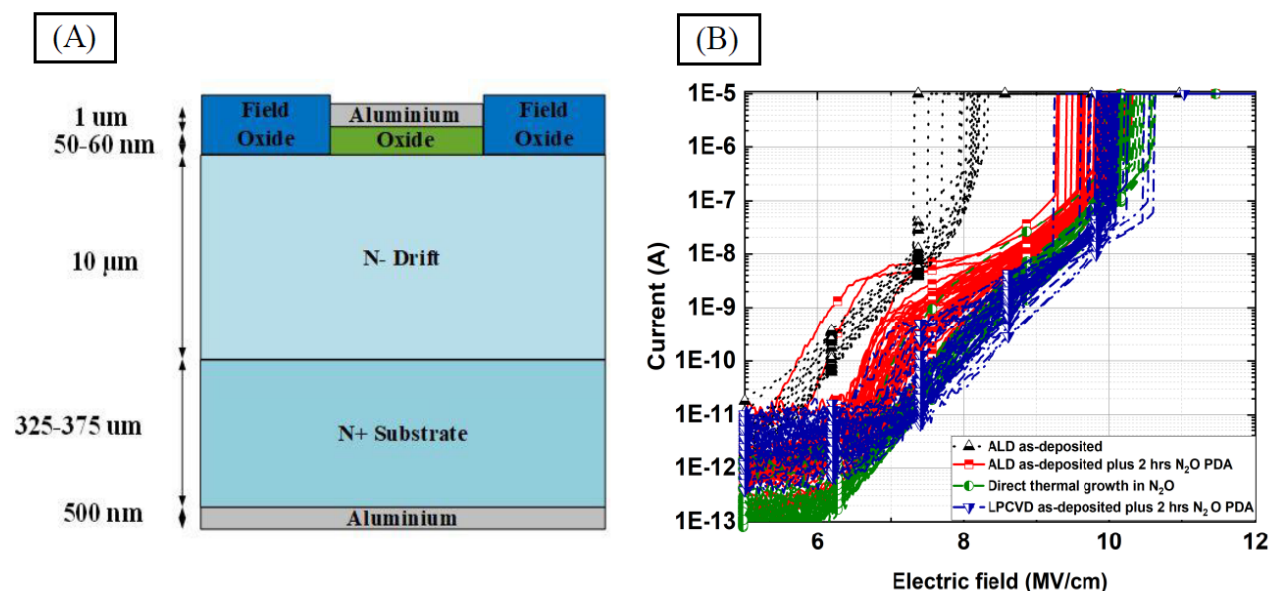


Figure 1: (a) Cross-section of the fabricated device structures. (b) Leakage current distribution of the measured devices at 175°C , with a device area of $7.86 \times 10^{-5} \text{ cm}^2$.

Results

Table 1 shows the key electrical parameters, extracted using room temperature capacitance-voltage (C-V) measurements, combined with current-voltage (I-V) and constant field TDDB measurements at 175°C . C-V measurements reveal the already poor quality of ALD as-deposited SiO_2 layers, with flatband voltages averaging 13.94 V and high frequency dispersion in accumulation. All MOSCAPs utilising oxides which were formed in a N_2O ambient showed significant improvements. V_{FB} is greatly improved for all N_2O -processed samples, with the ALD oxide with PDA offering the lowest flatband voltage, at 1.44 V. Frequency dispersion was greatly reduced for all N_2O -processed samples, down to a negligible level of $<0.2\%$ per decade. Although the ALD as-deposited sample shows the lowest hysteresis, the other two deposited layers still showed hysteresis values of 0.41 V, lower than the 0.60 V of the thermally-grown oxide. These results indicate a good general quality of the thermal oxide and of the deposited oxides after PDA.

Figure 1 (b) shows the leakage current distribution of the MOSCAPs at 175°C, analysed as a precursor to TDDB, and table 1 shows the extracted breakdown electric field (E_{BD}) values. The ALD as-deposited samples showed high leakage current at low voltage and premature breakdown at 8.58 MV/cm and were therefore excluded from the TDDB study. The remaining samples, all formed in a N_2O ambient, showed significant improvement, with E_{BD} averaging in a similar range, between 9.71 MV/cm (ALD SiO_2 with PDA) and 10.04 MV/cm (direct thermal growth). TDDB measurements were then performed for constant field values of 9 MV/cm and 9.6 MV/cm, and both the time to 63% failure ($T_{fail,63\%}$) and injected charge to 63% failure ($Q_{BD,63\%}$) were extracted.

Table 1: Key electric parameters of the different MOSCAPs. For flatband voltage, hysteresis and frequency dispersion values, at least 20 devices were measured for each annealing condition at room temperature and all values are given with standard deviations. For I-V analysis and TDDB analysis, at least 50 devices were measured for each split, at 175°C.

Sample	E_{BD} (MV/cm)	V_{FB} (V)	Hysteresis (V)	Freq. disp. (% per decade)	9 MV/cm		9.6 MV/cm	
					$T_{fail,63\%}$ (s)	$Q_{BD,63\%}$ (C/cm ²)	$T_{fail,63\%}$ (s)	$Q_{BD,63\%}$ (C/cm ²)
ALD As-dep. SiO_2	8.58 ± 0.87	13.94 ± 0.71	0.31 ± 0.08	12.27 ± 14.10	-	-	-	-
ALD SiO_2 plus N_2O PDA	9.71 ± 1.38	1.44 ± 0.20	0.41 ± 0.03	0.18 ± 0.06	4786	7.79	120	0.76
LPCVD SiO_2 plus N_2O PDA	9.83 ± 1.09	1.77 ± 0.23	0.41 ± 0.15	0.13 ± 0.06	3715	5.40	65	0.13
Direct thermal growth	10.04 ± 1.38	2.20 ± 0.12	0.60 ± 0.26	0.16 ± 0.03	3020	5.86	75	0.22

Weibull plots and I-t graphs are shown in Fig. 2, panel (a) and (b) respectively. The ALD oxide with PDA showed the best reliability for all 4 metrics, whereas the LPCVD and thermal oxides gave similar, lower values. For the lower field value of 9 MV/cm, the ALD oxide improves $T_{fail,63\%}$ by 29%, compared to the LPCVD oxide, and $Q_{BD,63\%}$ by 33%, compared to the thermal oxide. For the higher field value of 9.6 MV/cm, the ALD oxide offers a larger improvement, increasing $T_{fail,63\%}$ by 60% and $Q_{BD,63\%}$ by 345%, compared to the thermal oxide. Fig. 2 (b) shows that the breakdown mechanism has changed for the ALD oxide with PDA, showing buildup of positive charge in the MOSCAPs before negative charge triggers breakdown.

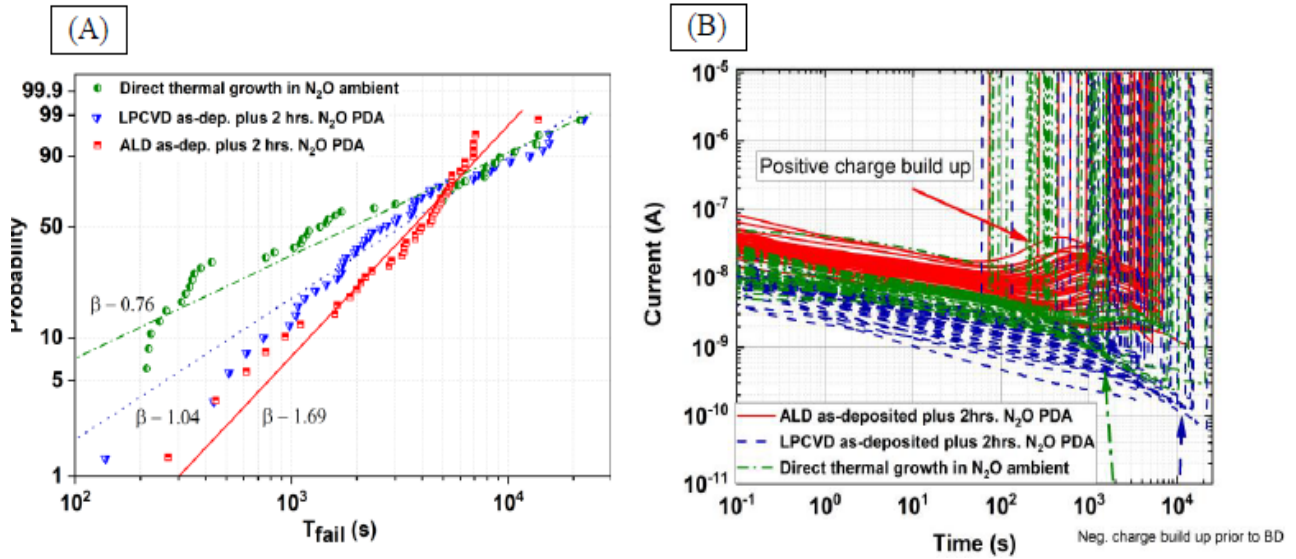


Figure 2: (a) Weibull probability distribution and shape factors of more than 50 MOSCAPs for each fabrication process, when stressed at a constant field of 9 MV/cm at $T=175^\circ\text{C}$. (b) Current over time for the same devices which were stressed at 9 MV/cm, $T = 175^\circ\text{C}$. ALD N_2O samples showed distinct positive charge build up prior to negative charge build up and breakdown, which could be seen for the whole dataset.

Conclusion

High-quality, high-reliability SiO_2 layers, formed by ALD and post-deposition anneal (PDA), have been demonstrated. Flatband voltage and hysteresis are reduced, compared to thermally grown oxide, and frequency dispersion in accumulation is negligible. At 175°C , the oxide critical electric field is in line with thermally grown oxide and LPCVD oxide with PDA. The ALD oxide with PDA has demonstrated higher reliability than LPCVD and thermal oxide in TDDDB, offering 29% to 345% improvement. The ALD oxide shows different degradation mechanisms to the LPCVD and thermal oxides, with positive charge building up before breakdown.

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