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Surface Potential Fluctuations of SiO_2/SiC Interfaces Investigated by Local Capacitance-Voltage Profiling Based on Time-Resolved Scanning Nonlinear Dielectric Microscopy

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Abstract. We investigate surface potential fluctuations on SiO_2/SiC interfaces by local capacitance-voltage profiling based on time-resolved scanning nonlinear dielectric microscopy. As experimental indicators of surface potential fluctuations, we measured the spatial fluctuations of local capacitance-voltage and its first derivative profiles through the detection of the voltages at the infection points of the profiles. We show that, even for a sample with a nitrided interface with low interface defect density, the fluctuations of the measured voltages are much higher than the thermal energy at room temperature. This indicates the existence of high potential fluctuations, which can give a significant impact on the carrier transport at the SiO_2/SiC interface of SiC metal-oxide-semiconductor field effect transistors.

Introduction

SiO_2/SiC interfaces have been extensively studied because of their significant impact on the performance of the SiC metal-oxide-semiconductor field effect transistors (MOSFETs) such as channel mobility and threshold voltage [1, 2]. Si-face 4H-SiC MOSFETs with an as-oxidized MOS interface typically show a peak field effect mobility (μ_{FE}) of ~10 cm^2/Vs or less. As a standard treatment, post oxidation annealing (POA) in nitrogen rich environments has been established for the reduction of interface defect density (D_{it}) [3-7]. Although the POA treatment improves the peak of μ_{FE} (e.g. POA in NO achieves about 40 cm^2/Vs), the achievable mobility is still much lower than the bulk mobility in SiC. In order to understand the cause of the observed low mobility, possible mechanisms have been suggested so far [8, 9]. In addition, recently, the formation of the interface by hydrogen etching pretreatment of a SiC surface followed by SiO_2 deposition instead of thermal oxidation has been proposed and paid considerable attention as a key to further drastic reduction of interface defects including those at shallow levels [10]. It has been demonstrated that this new technique allows the fabrication of normally-off transistors with μ_{FE} of ~80 cm^2/Vs at the peak [11]. However, the record value is still one order magnitude lower than bulk carrier mobility of SiC (1000 cm^2/Vs).

For deeper understanding of the interface properties, we focus on surface potential fluctuations on SiO_2/SiC interfaces. An early study using the conductance method by Bano *et al*. has shown that, unlike SiO_2/Si, SiO_2/SiC interfaces have surface potential fluctuations largely exceeding the thermal energy at room temperature (~ 26 mV) [12]. It has been pointed out that the high surface potential fluctuations can give a significant impact on the carrier transport at the SiO_2/SiC interfaces [12, 13]. Thus, here we investigate the surface potential fluctuations at the SiO_2/SiC interfaces by scanning nonlinear dielectric microscopy (SNDM) [14]. SNDM is a scanning probe microscopy method that has exceptionally high sensitivity to the variation in the microscopic capacitance. So far, the imaging the first voltage derivative of capacitance (dC/dV) by the conventional SNDM was performed on various SiO_2/SiC samples. It has been shown that the dC/dV images for the samples with different macroscopic D_{it} levels have commensurate levels of spatial fluctuations [15]. The fluctuations of dC/dV reflect those of local CV profiles in part. If the local CV profiling is enabled, we are able to give real-space microscopic insights on the surface potential fluctuations of the SiO_2/SiC interfaces.

In this paper, we perform local CV profiling on SiO_2/SiC based on recently developed time-resolved SNDM (tr-SNDM). We discuss the spatial fluctuation of local CV profiles in real-space by extracting the voltages giving particular features of the profiles. We show that the fluctuations of the extracted voltages are much higher than the thermal energy at room temperature.

Local CV and d*C*/d*V*-*V* Profiling

Local CV profiling was here performed using tr-SNDM [16]. A tr-SNDM setup was implemented to a commercial atomic force microscopy (AFM) system (Bruker, Dimension Icon) operated in air at room temperature. We mounted a lab-made SNDM probe on the AFM head; the SNDM probe is made of an LC self-oscillator and detects the variation in the microscopic capacitance below the conductive tip of an AFM cantilever attached to the oscillator. The center frequency of the oscillator is modulated by the capacitance variation caused by a voltage pulse applied between the tip and sample. Unlike the conventional SNDM using classical analog signal processing, tr-SNDM demodulates the capacitance response to the voltage pulse by the high-speed direct digitization and offline software signal processing. This permits wide measurement bandwidth and flexible signal treatments. The more details of the technique and setup can be found in Ref. [16].

We can perform point-by-point local CV and dC/dV-V profiling by sweeping the voltage at each measurement point on the sample [17, 18]. When a triangular voltage pulse is used for the voltage sweep, the resulting capacitance response can be converted to backward and forward local CV profiles over the sweep range [17]. In addition, the first derivative of the local CV profile, or a dC/dV-V profile, can be simultaneously taken by adding a small high frequency voltage to the triangular pulse [18]. The dC/dV-V profile can be obtained from a high frequency component arising in the capacitance response, because it has a higher amplitude as the slope of the local CV profile increases. The local CV profiling performed here differs from the standard macroscopic CV profiling based quasi-static voltage sweep. The sweep rate in the local CV profiling is typically equivalent to the frequency in the order of 10 kHz and thus the profiles reflect deep depletion in the depletion region, since an inversion layer is not formed during the fast voltage sweep.

In order to discuss the spatial fluctuations of the local CV profiles, here we focus on the fluctuations of the voltages at the infection points of the individual local CV and dC/dV-V profiles. As shown in Fig. 1, these voltages are here denoted V_1 and V_2. V_1 and V_2 respectively denote the voltage at the infection point of a local CV profile and that of the corresponding dC/dV-V profile. We extract V_1 and V_2 to estimate the voltage shifts of the local CV profiles. V_1 and V_2 are numerically detected by finding the voltage at the negative peak of a local dC/dV-V profile and that at the positive peak of a local d^2C/dV^2-V profile, respectively. Local d^2C/dV^2-V profiles are numerically derived from the dC/dV-V profiles. The fluctuations of V_1 and V_2 are experimental indicators for surface potential fluctuations, because the fluctuations of a built-in potetial at the interface causes the shift of the local CV profiles. The fluctuations can be caused by the spatially non-uniform distribution of D_{it} and fixed oxide charge density at the interface. V_1 and V_2 can have different spatial distributions, because they reflect the different spatial distributions of charge states at the different energy levels in general. Since V_2 is located closer to the deep depletion region, the spatial fluctuations of V_2 are dominated by those of the static charge states with no significant dependence on the applied voltage such as fixed oxide charges and deep level defects. The fluctuations of V_1 located near the accumulation region are further affected by those of voltage-dependent charge states such as defects at shallower levels. This implies that V_1 is expected to be higher than V_2, as the fluctuations of V_1 are cumulatively affected from the shallower levels as well as the static interface charge states.

It is noted that similar local CV analysis, called scanning capacitance spectroscopy [19], has also been performed for SiO_2/4H-SiC samples by scanning capacitance microscopy [20]. In Ref. [20], local CV profiles were obtained by integrating dC/dV-V profiles to discuss the spatial fluctuations of V_1, while the sweep rate was much smaller than that in this study.

Results and Discussions

Here we measured local CV and d*C*/d*V*-*V* profiles on two different n-type 4H-SiC(0001) samples with a 10 nm-thick thermal oxide layer and 10^{16} cm^{-3} dopant concentration. One of the samples was as-oxidized but the other was further treated by POA in NO gas for 60 min. at 1250 deg. C. The oxide layers of the measured samples were thinner than those of typical SiC wafers for power device applications in order to obtain higher spatial resolution in local CV profiling. We think that even the samples with such a thin oxide layer are worth investigating. This is because, as reported in Refs. [21, 22], electric defects such as interface defects, oxide charges, and near interface traps have been detected even for SiC with thin oxide layer thickness, while their density depends on the thickness. In addition, it has been considered that nitrogen atoms are localized at the SiO_2/SiC interface treated by POA in NO gas [23, 24].

We used a Pt-Ir coated microcantilever with a 100 nm radius tip (NanoWorld, EFM-100). For local CV profiling, we applied a 1.5 cycle triangular voltage pulse with an amplitude of 20 V_{pp} and a slew rate of 0.4 V/μs. In addition, a 1 MHz and 2 V_{pp} high frequency sinusoidal voltage was added to the triangular pulse for the simultaneous d*C*/d*V*-*V* profiling. The voltage was applied to the sample relative to the grounded tip. For the reduction of noise, a local CV profile was obtained by averaging the capacitance responses to repetitive 160 voltage pulses at each measurement point. The scan size was 1 μm×1 μm for both samples.

Figure 2 shows typical local CV [Fig. 2(a)] and d*C*/d*V*-*V* [Fig. 2(b)] profiles for the as-oxidized sample. It is confirmed that the local CV profiles showed typical n-type characteristics with a negative slope. As shown in Fig. 3, the nitrided sample had local CV and d*C*/d*V*-*V* profiles less stretched out than the as-oxidized one, which was expected from the significant reduction of D_{it} by the POA treatment. Figures 4 and 5 show V_1 and V_2 images for the as-oxidized and nitrided samples, respectively. The images were reconstructed by extracting V_1 and V_2 values from the backward and forward local CV and d*C*/d*V*-*V* profiles. We found that V_1 and V_2 had spatially non-uniform clustered distributions as similar to d*C*/d*V* reported in the previous study [15]. The standard deviations (SDs) of V_1 and V_2 were summarized in Table I for the comparison of fluctuations. For obtaining V_1 values, outliers were excluded, because V_1 was not detected within the measurement range on some measurement points especially for the as-oxidized sample. The SDs of V_1 were as high as 1 V for the as-oxidized sample but decreased by 80 % for the nitrided sample, which indicates the POA treatment significantly reduces D_{it} contributing surface potential fluctuations. V_2 less fluctuated than V_1 for both samples, as expected from the location of V_2 closer to the deep depletion region with lower interface charge density. The SDs of V_2 also decreased by 40 % through the POA treatment and became lowest but still several times higher than the thermal energy at room temperature. This suggest that the elimination of the static interface charges and their fluctuations is at least necessary to suppress surface potential fluctuations within the thermal energy level.

Conclusion

We performed local CV profiling on the as-oxdized and nitrided SiO_2/SiC samples for investigating the surface potential fluctuations, which may give a significant impact on the carrier transport properties of SiC MOSFETs. The SDs of V_1 and V_2 largely exceeded the thermal energy at room temperature even for the nitrided sample. Our results indicate that surface potential fluctuations remain high even after the significant reduction of D_{it} by the POA treatment. It seems that the surface potential fluctuations are already higher than the thermal enegy due to the contribution of the static interface charge states such as fixed charges and deep level defects and they further increase with the charge trapping to shallower levels.

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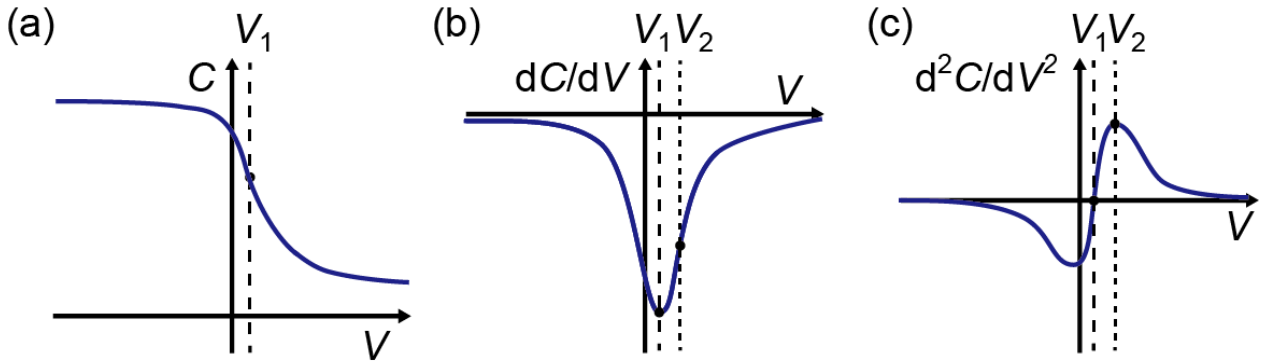

Fig. 1. Schematic illustration of local CV [(a)], dC/dV-V [(b)], and d^2C/dV^2-V profile [(c)] for an n-type local metal-insulator-semiconductor capacitor. V_1 and V_2 respectively denote the voltage at the infection point in (a) and that in (b).

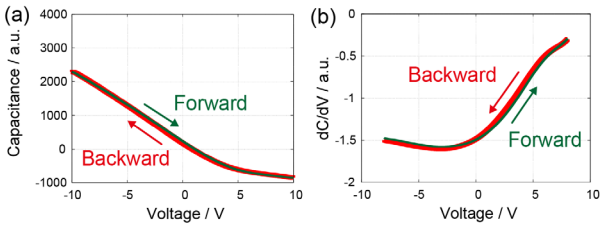

Fig. 2. Typical local (a) CV and (b) dC/dV-V profiles of the as-oxidized SiO_2/SiC sample

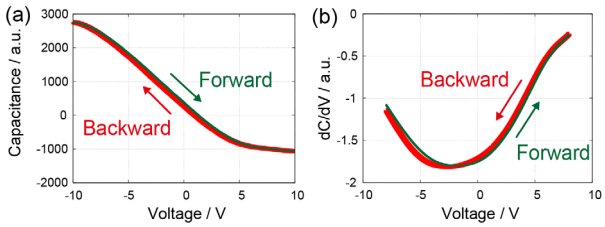

Fig. 3. Typical local (a) CV and (b) dC/dV-V profiles of the nitrided SiO_2/SiC sample

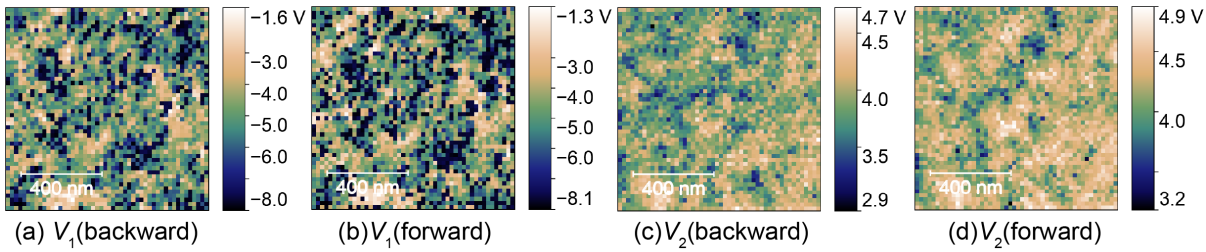

Fig. 4. V_1 and V_2 images of the as-oxidized sample.

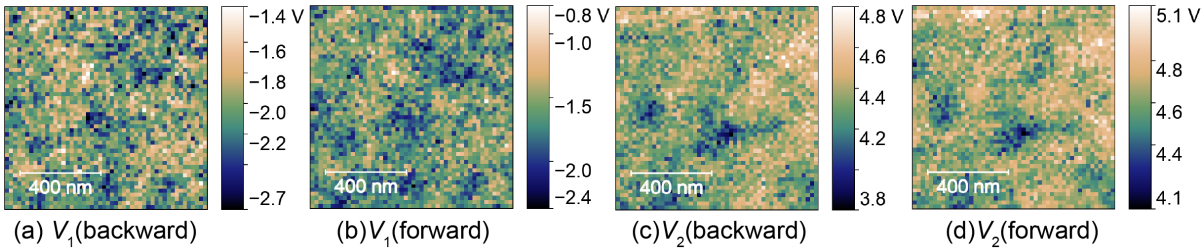

Fig. 5. V_1 and V_2 images of the nitrided sample.

Table I. Standard deviations of fluctuations in V_1 and V_2

Sample	V_1 (backward) / V	V_1 (forward) / V	V_2 (backward) / V	V_2 (forward) / V
As-oxidized	1.01	1.12	0.25	0.24
Nitrided	0.22	0.22	0.14	0.13

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