Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 346-350
doi:10.4028/p-fnktjf

Submitted: 2021-10-22
Revised: 2022-02-21
Accepted: 2022-03-07
Online: 2022-05-31

Sensitivity of D_{it} Extraction at the SiO_2/SiC Interface Using Quasi-Static Capacitance-Voltage Measurements

Manuel Belanche[1,a*], Piyush Kumar[1,b], Judith Woerle[1,c], Roger Stark[1,d] and Ulrike Grossner[1,e]

[1]Advanced Power Semiconductor Laboratory, ETH Zurich, Physikstrasse 3, 8092 Zurich, Switzerland

[a]belanche@aps.ee.ethz.ch, [b]kumar@aps.ee.ethz.ch, [c]woerle@aps.ee.ethz.ch, [d]stark@aps.ee.ethz.ch, [e]ulrike.grossner@ethz.ch

Keywords: interface characterization, quasi-static capacitance, capacitance-voltage measurements, MOS capacitors.

Abstract. In this work, we compare different quasi-static capacitance-voltage measurement systems by analyzing 4H-SiC n-type MOS capacitors and studying the influence of systematic errors when extracting the interface trap density (D_{it}). We show that the extracted D_{it} strongly depends on the calculation of the surface potential due to variations of the integration constant Δ. In addition, the ramp-rate during the quasi-static measurement is identified as a sensitive measurement parameter whose noise level is amplified in the D_{it} extraction.

Introduction

Owing to its beneficial electrical and thermal properties, silicon carbide (SiC) is a well-established material for power electronic devices. However, the widespread use of SiC MOSFETs in power applications results in increasingly demanding requirements regarding their performance and reliability. Despite the commercial success of SiC MOSFETs, there are still unsolved reliability issues related to the number of defects and near-interface traps situated at the interface between silicon carbide and silicon dioxide (SiO_2) that are generated during thermal oxidation [1]. Therefore, a careful analysis of the density of interface traps (D_{it}) and their effect on the device performance is crucial for process development and monitoring.

Different methods have been used to study the D_{it} at the SiO_2/SiC interface [2], among which capacitance-voltage (CV) measurements are the most established technique due to their apparent simplicity in both execution and interpretation of results. The D_{it} can be extracted as a function of the energy position in the bandgap by comparing a low-frequency or quasi-static capacitance curve with a high-frequency measurement [3] or a theoretical CV curve [4].

However, in quasi-static capacitance measurements, the values obtained for low capacitances are very sensitive to the setup parameters used in the analysis of D_{it}. This can lead to inaccuracies that are difficult to detect but strongly influence the final result. Here we present a study of the systematic errors encountered when performing quasi-static capacitance-voltage measurements and the subsequent extraction of D_{it} for the analysis of the SiO_2/SiC interface.

Experimental Details

The devices tested are 4H-SiC n-type MOS capacitors. For the results in Fig. 1, the analyzed MOS capacitors have a doping concentration of $N_D = 4.7 \times 10^{15}$ cm^{-3} and 48 nm of thermal oxide grown at 1300 °C. The high-frequency capacitance was measured using the *Keithley 4200A-SCS*.

The quasi-static measurements shown in Fig. 2 and Fig. 3, were performed on MOS capacitors with a 23 nm thick thermal oxide using three systems: *Keithley 595 QS CV Meter*, *Keysight B1500A* and *Keithley 4200A-SCS*. The gate electrode used for all MOS capacitors was a 100 nm layer of nickel deposited with e-beam evaporation.

Extraction of Surface Potential

For the study of the D_{it}, we use the C-ψ_s method [4]. In this method, the relationship between the applied gate bias (V_g) and the surface potential (ψ_s) is calculated with the quasi-static (C_{QS}) and oxide capacitance (C_{ox}) by solving the Berglund integral [5]:

$$\psi_s(V_g) = \int \left(1 - \frac{C_{QS}}{C_{ox}}\right) dV_g + \Delta, \tag{1}$$

where:

$$\psi_s' = \int \left(1 - \frac{C_{QS}}{C_{ox}}\right) dV_g = \psi_s(V_g) - \Delta. \tag{2}$$

Following the C-ψ_s method [4], the constant Δ is determined from the extrapolation of a linear fit of ψ_s' vs $1/C_{dep}^2$, where the depletion capacitance (C_{dep}) is obtained from a high-frequency CV measurement, i.e. assuming there is no influence from traps. Here we observe that the ψ_s' range used to perform the linear fitting influences the value of Δ. Even though the shift in Δ seems small, it can have a strong impact on the D_{it} along the energy axis [6], causing a wrong evaluation of the defect density at the SiO_2/SiC interface. In order to extract Δ, it is crucial to limit the linear fit to the range where the MOS capacitor is in depletion, i.e. were ψ_s' decays linearly with $1/C_{dep}^2$, and to not include the voltage range of deep depletion, where the relation ψ_s' vs. $1/C_{dep}^2$ is not linear anymore. The depletion region boundaries can be identified by considering that the slope of $1/C_{dep}^2$ is inversely proportional to the doping concentration of the epitaxial layer [3].

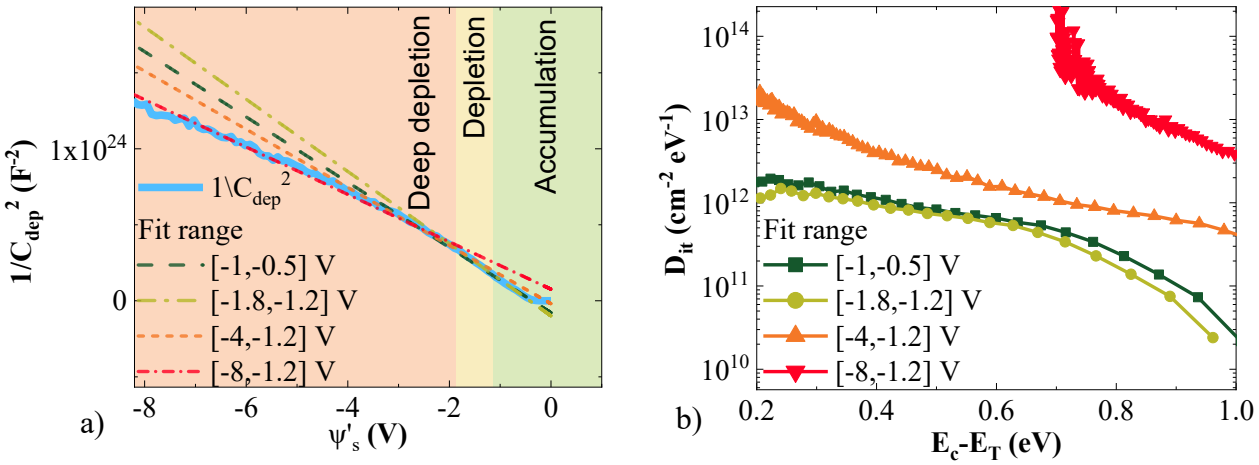

Figure 1. Impact of the linear fitting range on the D_{it} analysis of the SiC/SiO_2 interface. a) Linear fitting of $1/C_{dep}^2$ (blue) for four different voltage ranges and their extrapolation (fit (Δ) = 0) to obtain the integration constant Δ. b) Impact of the small variations in Δ on the D_{it} extraction. Different fitting regions are shown: from depletion to weak accumulation (dark green), only the depletion region (light green), different ranges in the deep depletion regime (red and orange).

In Fig. 1a, the results of the CV analysis are shown, where the blue curve was obtained at a measurement frequency of 2 MHz. The red and orange curves are obtained by fitting in a ψ_s' range that leads the MOS capacitor into deep depletion and depletion. The dark green curve is evaluated using ψ_s' = [-1 V, -0.5 V] where the MOSCAP is in accumulation; whereas the light green is obtained by applying the fitting only in depletion. The distance between the intersection point, $1/C_{dep}^2 = 0$, for each of the fit ranges is small; from 0.1 V for the smallest to 0.9 V for the largest. The impact of such voltage shifts on the D_{it} profile is shown in Fig. 1b. These apparently small voltage shifts of Δ can translate to a wide shift of the D_{it} curve, resulting in a wrong estimation of the interface quality.

Therefore, for obtaining the constant Δ, the fitting of ψ_s' vs $1/C_{dep}^2$ must be performed in the depletion region only, which requires a precise selection of the fit range for each device under test.

Analysis of Quasi-Static Capacitance-Voltage Setup Parameters

In order to calculate $\psi_s(V_g)$ and proceed with the C-ψ_s method, a quasi-static capacitance-voltage measurement is required. We have studied the sensitivity of the measurement with respect to the selected ramp-rate (V/s), which is one of the main setup parameters in a quasi-static measurement system. Moreover, we have investigated the impact of using three different setups for the C_{QS} measurements on the D_{it} extraction.

The ramp-rate (V/s) in a quasi-static measurement represents a trade-off between the resolution of the voltage sweep and the noise in the capacitance value [7]. This is illustrated in Fig. 2a showing the quasi-static capacitance (C_{QS}) measurements with three different ramp-rates: 0.1, 0.5 and 1 V/s, respectively. Applying the C-ψ_s method for each of the ramp-rates, we observe that closer to the conduction band, there is a deviation of the D_{it} extracted for the 0.1 V/s ramp when compared to the other two values. This originates from the increasing noise in the measured discharge capacitance that becomes more prominent at low ramp-rates.

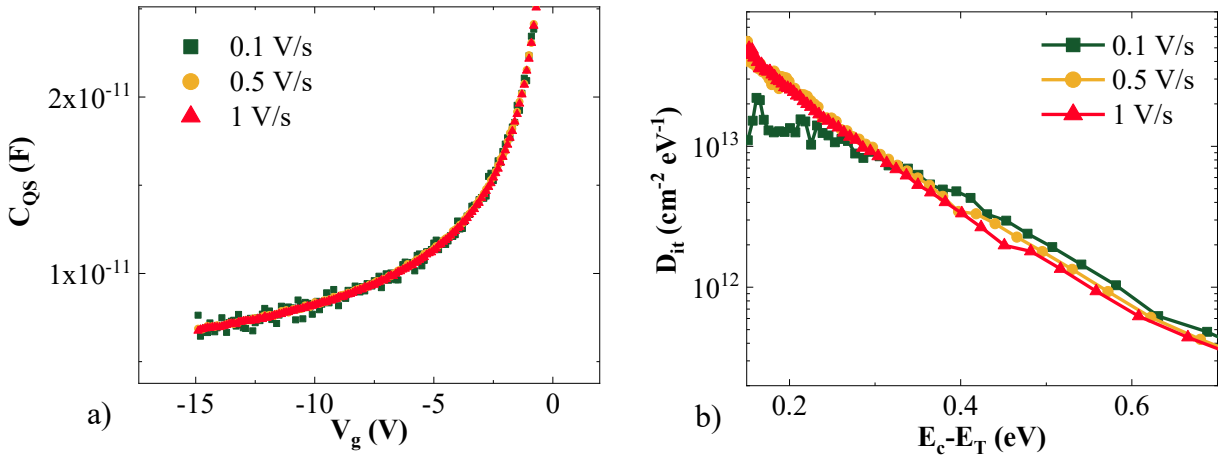

Figure 2. Influence of ramp-rate on capacitance analysis of the SiC/SiO_2 interface, measured with the *Keysight B1500A*. a) Quasi-static capacitance measured with different ramp-rates: 0.1 (V/s) (dark green), 0.5 (V/s) (ochre) and 1 (V/s) (red). b) D_{it} extraction from the measurements with different ramp-rates in a).

We acquired the QS measurement of the capacitance with three different systems: *Keithley 595 QS CV Meter*, *Keysight B1500A* and *Keithley 4200A-SCS*. Fig. 3a illustrates the different quasi-static curves measured by the different setups. The results obtained with the different setups show small variations over the entire voltage sweep from deep depletion to accumulation attributable to the slight differences in the quasi-static principles used by each system. Also shown are 1 MHz and 1 Hz

capacitance curves measured with the MFIA Zurich Instruments system that were analyzed using the high-low capacitance method [8].

Taking into consideration the sensitivity of the surface potential calculation as well as the ramp-rate effect previously discussed, we applied the C-ψ_s method and compared the D_{it} distribution from the measurements performed with the three quasi-static systems, Fig. 3b. We observe that for energies higher than E_C-0.25 eV, the results of the three quasi-static setups are matching. However, due to the small differences in lower capacitance, and lower voltage values, the D_{it} distribution shows a different behaviour in the energy below 0.25 (eV) for the the *Keysight B1500A* compared to the results from the *Keithley 595 QS CV Meter* and the *Keithley 4200A-SCS*. Moreover, Fig. 3b includes the D_{it} results obtained with the high-low technique [8], which, as expected [4], underestimates the density of interface traps.

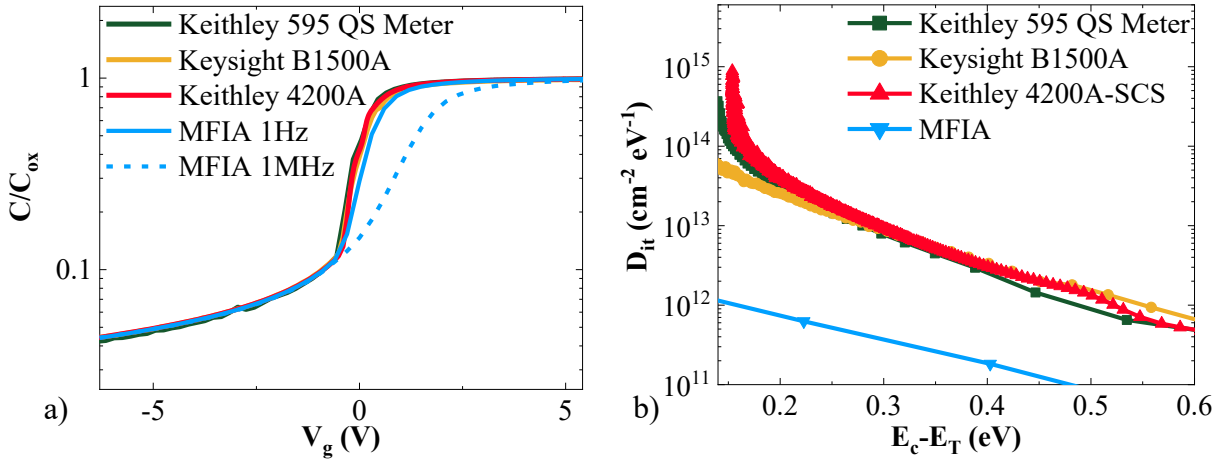

Figure 3. a) Quasi-static capacitance measured with the different setups. b) D_{it} extraction from the different quasi-static setups with the C-ψ_s method (dark green, ochre, red) and simultaneous high-low method (blue).

Summary

In this work, we have studied how the choice of the quasi-static CV setup and selected parameters for applying the C-ψ_s method influence the evaluation of D_{it}. Capacitance-voltage measurements of 4H-SiC n-type MOS capacitors show that the calculation of the surface potential can be a strong source of error if the depletion region is not well identified during the extraction of the integral constant Δ. We assessed the influence of ramp-rate in the quasi-static measurements and observed that its impact is more prominent for lower values of energy due to the increasing relative noise. Finally, we compared three commonly used quasi-static systems, finding differences in their D_{it} distribution, more noticeable for lower energies. Further studies are needed to ascertain the optimal system and setup for the application of quasi-static methods.

References

[1] V. V. Afanasev, M. Bassler, G. Pensl, M. Schulz, Intrinsic SiC/SiO_2 Interface States, Phys. Stat. Sol. (a), 162(1), 321-337 (1997).

[2] J. A. Cooper, Advances in SiC MOS Technology, Phys. Stat. Sol. (a) 162, 305-319 (1997).

[3] E. H. Nicollian, J. R. Brews, MOS Physics and Technology, Wiley, New York (1982).

[4] H. Yoshioka, T. Nakamura, T. Kimoto, Accurate evaluation of interface state density in SiC metal-oxide-semiconductor structures using surface potential based on depletion capacitance, J. Appl. Phys. 111, 014502 (2012).

[5] C.N. Berglund, Surface States at Steam-Grown Silicon-Silicon Dioxide Interfaces, IEEE Trans. Electron Dev. ED-13, 701–705 (1966).

[6] D. K. Schroeder, Oxide and interface trapped charges, oxide thickness, in Semiconductor material and device characterization, John Wiley & Sons (2006).

[7] A. Wadsworth, Keysight technologies: The parametric measurement handbook (2014).

[8] R. Castagne, A. Vapaille, Description of the SiO2-Si interface properties by means of very low frequency MOS capacitance measurements, Surf. Sci. 28, 157–193 (1971).