

## Synchrotron X-Ray Topography Characterization of Power Electronic GaN Materials

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**Abstract.** Synchrotron X-ray topography techniques are used to characterize the microstructures in gallium nitride materials being developed for selective area doping for power electronic applications. Bulk substrates grown by different methods, epitaxial layers that are subject to ion implantation, annealing, etching and regrowth are characterized by X-ray topography in grazing incidence geometry and X-ray rocking curve topography. Strain and tilt maps of ion implanted epitaxial layers and etched and regrown wafers are generated. From the X-ray topographs, it is concluded that ammonothermal grown substrates show the highest quality among other types and most suitable for high-end electronic applications. It is also revealed that epitaxial growth, ion implantation and the annealing process do not change the dislocation distribution, but ion implantation introduces damage, strain and lattice bending effect, which are removed after annealing. Inductively coupled plasma (ICP) etching gives rise to strain variations in the wafer, while using tertiary butyl chloride (TBCl) to etch the wafer does not affect the strain distribution and can remove some damage from a preceding ICP etching process.

### Introduction

Gallium nitride (GaN) is one of the most promising wide band gap semiconductor materials that can replace silicon (Si) in the applications of power electronic devices as the latter has nearly reached its performance limits. However, the performance of the GaN based power devices is limited by the availability of high-quality GaN substrates and reliable selective area doping techniques.

Several bulk growth techniques for GaN have been developed including ammonothermal growth [1] and hydride vapor phase epitaxy (HVPE) [2]. A patterned HVPE method [3] has also been developed to lower the dislocation density. Selective area doping techniques are critical to the fabrication of vertical GaN-based power electronic devices. Ion implantation is a very common

doping technique that can be used for selective area doping. To remove the damage induced by ion implantation and activate the implanted atoms, several annealing methods have been developed for GaN materials, including AlN capped annealing [4], high pressure annealing [5] and a combination of both under non-equilibrium annealing conditions [6]. Selective area etching and regrowth is another method to realize the device structures on GaN materials. Different etching methods have been deployed including inductively coupled plasma (ICP) etching [7] and tertiary butyl chloride (TBCl) etching [8].

## Experiments

Table 1 lists the samples that are characterized by synchrotron X-ray topography. Synchrotron monochromatic beam X-ray topography (SMBXT) [9] ( $E=9.37$  KeV) and synchrotron X-ray rocking curve topography (SXRCT) [10] ( $E=8.05$  KeV) are both conducted at beamline 1-BM of Advanced Photon Source (APS) in Argonne National Laboratory (ANL).

Table 1. Sample list and descriptions

Sample type	#	Description
GaN substrates	1	Ammonothermal grown substrate
	2	Patterned HVPE grown substrate
	3	Regular HVPE grown substrate
Epitaxial growth, implantation and annealing	4	Sequentially studied at substrate (grown by ammonothermal method), MOCVD grown epitaxial layer ( $1\ \mu\text{m}$ ), Mg ion implanted, and high pressure annealed (1 GPa, $1440^\circ\text{C}$ , 10 min)
	5	Mg/N co-implanted epitaxial layer on ammonothermal grown substrate
	6	AlN capped, annealed $1225^\circ\text{C}$ , 2 min, same implantation process as sample 5
Etching and regrowth	7	Continuously grown without etching process on HVPE wafer
	8	ICP etched and regrown on HVPE wafer
	9	TBCl etched and regrown on HVPE wafer
	10	ICP and TBCl etched and regrown on HVPE wafer

## Results and Discussions

**GaN Substrates.** SMBXT characterization of different types of GaN substrates has been conducted [11-13]. Figure 1 includes the magnified topographs of the GaN substrates grown by ammonothermal method, patterned HVPE method and regular HVPE method. The contrast of white dots in the topographs is identified as threading dislocations, while the curved line contrast represents basal plane dislocations (BPDs). For the ammonothermal grown substrate shown in Figure 1 (a), the overall dislocation density is calculated as  $1.1 \times 10^4\ \text{cm}^{-2}$ , which indicated a very high quality of the GaN substrate. No BPDs are observed in the ammonothermal GaN substrate. In the patterned HVPE GaN substrate shown in Figure 1 (b), large areas with low dislocation densities below  $10^2\ \text{cm}^{-2}$  are observed between a grid of strain centers with relatively higher threading dislocation densities larger than  $10^4\ \text{cm}^{-2}$ . BPDs are also observed around strain centers, with a density larger than  $10^5\ \text{cm}^{-2}$ . In Figure 1 (c), it is noted that not many individual dislocations can be resolved, which means that the dislocation density is in the range of  $10^5$  -  $10^6\ \text{cm}^{-2}$ . The threading dislocations, especially screw types, are found responsible in degradation of reverse bias current leakage [14, 15], which can be challenging for high-end power electronic device fabrication.

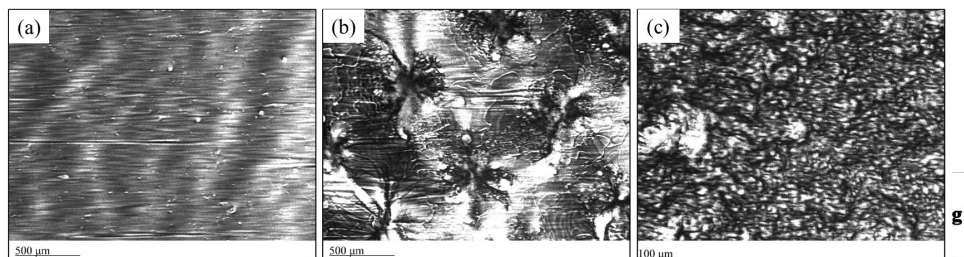


Figure 1. SMBXT images ( $g = 11\bar{2}4$ ; 9.37 KeV) of bulk GaN substrate grown by (a) ammonothermal method, (b) patterned HVPE method, and (c) regular HVPE method.

### Epitaxial Growth, Ion Implantation, and Annealing.

SMBXT and SXRCT analysis of changes in microstructures during epitaxial growth, ion implantation and different annealing techniques has been conducted [16, 17]. Figure 2 shows the overall SMBXT images of sample 4 at different processing stages. Both the overall topography

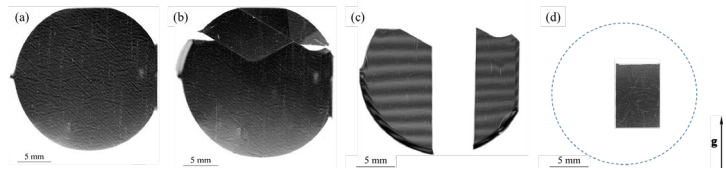


Figure 2. SMBXT images ( $g = 11\bar{2}4$ ; 9.37 KeV) of sample 4 in the stage of (a) bare substrate, (b) epitaxial wafer, (c) as-implanted wafer, and (d) annealed wafer.

images of the bare substrate and epitaxial wafer have only one contour, which indicates very low lattice bending levels. The estimated radius of curvature is larger than 97 m. However, in Figure 2 (c), consisting of pieces of the as-implanted wafer, multiple contours obtained by rocking the sample are needed to cover the wafer area, and the radius of curvature of the wafer is calculated as only 9.7 m. This is due to the insertion of the implanted atoms during the ion implantation process, which causes higher lattice distortions. After high pressure annealing for the piece of the GaN wafer in the middle, it is revealed that the lattice bending level is restored to the original level due to appearance of single contour in the image. This result indicates that the high-pressure annealing process can successfully remove the lattice bending effect by incorporation of the dopant atoms from interstitial sites to substitutional sites in the crystal. Enlarged SMBXT images in Figure 4 show that the threading dislocation distribution remains the same during epitaxial growth, ion implantation, and the subsequent high pressure annealing process ((a), (b), and (c) are from the same region on the wafer, but (d) shows another area of the wafer). The enlargement of dislocation contrast after epitaxial growth is due to the interaction between threading dislocations and the vacancies, by which helical dislocations are formed [18].

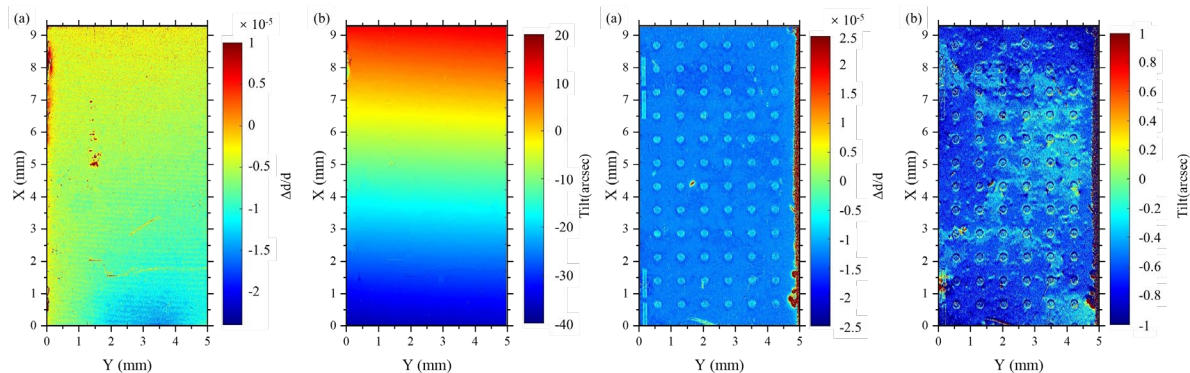


Figure 3. (a) Strain map of sample 5; (b) Tilt map sample 5; (c) Strain map of sample 6; (d) Tilt map of sample 6. Note: The pattern of round shapes is for the testing purpose and not microstructure related.

Figure 4 shows the strain and tilt maps of sample 5 and sample 6 extracted from 0004 rocking curve topographs recorded in 0 and 180 positions. The strain values on the as-implanted wafer ranges from  $-1.5 \times 10^{-5}$  to 0, and the tilt ranges from  $-30''$  to  $15''$ . For the annealed sample, the strain ranges from  $-1 \times 10^{-5}$  to  $-5 \times 10^{-6}$ , which is similar to the as-implanted wafer. However, the tilt range of the annealed wafer is only from -1 arcsecond to 0.5 arcsecond, which is significantly decreased compared to that of the as-implanted wafer. This means that the capped annealing process modifies the lattice strain uniformly across the wafer. The lattice bending effect is also lowered by the annealing process.

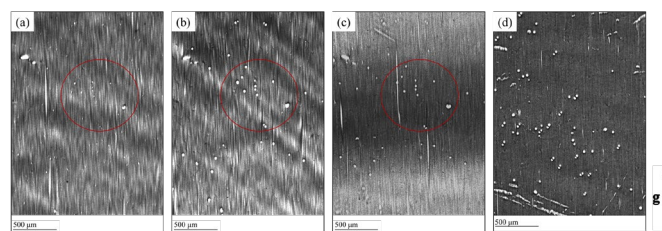


Figure 4. Magnified SMBXT images of sample 4.

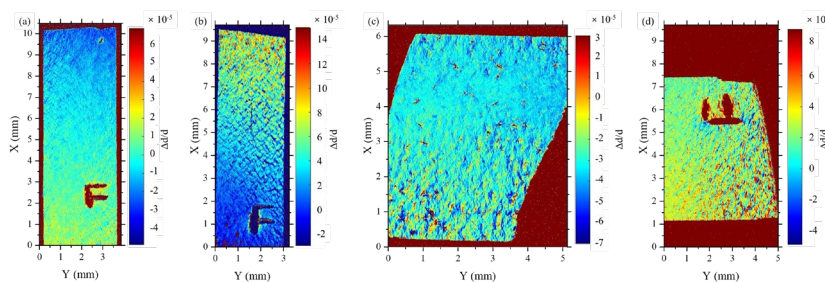


Figure 5. (a)-(d) Strain maps of sample 7 to sample 10.

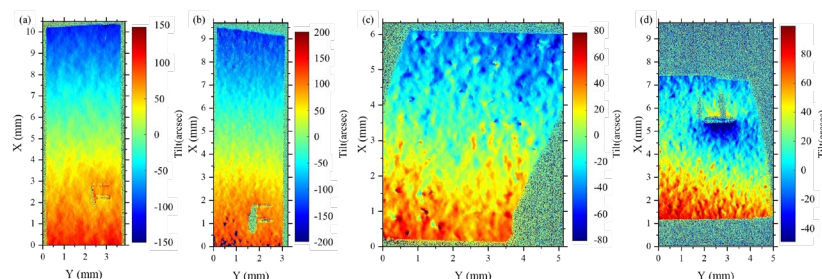


Figure 6. (a)-(d) Tilt maps of sample 7 to sample 10.

Table 2. Strain and tilt ranges of sample 7 to sample 10 from the strain and tilt maps.

#	Description	Strain range	Tilt range
7	Continuously grown	$4 \times 10^{-5}$	230''
8	ICP etched	$1.6 \times 10^{-4}$	300''
9	TBCl etched	$2.5 \times 10^{-5}$	160''
10	ICP and TBCl etched	$6 \times 10^{-5}$	115''

**Etching and regrowth.** Strain and tilt maps of the etched and regrown samples are plotted out of the SXRCT data. Table 2 summarizes the strain and tilt ranges in the maps in Figure 5 and Figure 6. It can be noted that the ICP etched and regrown sample has a strain range of  $1.6 \times 10^{-4}$ , while that of the other samples are in the order of  $10^{-5}$ . This indicates that the ICP etching process can cause some non-uniform lattice damage to the wafer due to the ion bombardment. The TBCl etched sample, on the other hand, has the smallest strain range. This is because the TBCl etching process does not involve reactive ion bombardment on to the sample. By comparing the strain ranges of ICP etched wafer and the ICP + TBCl etched wafer, it can also be noted that the TBCl etching can recover some of the damage from the ICP process by removing some of the severely damaged layers from the surface. For the tilt ranges of the samples, it should be noted that the imaged regions for sample 9 and sample 10 are smaller. Therefore, the tilt ranges of all the samples are similar, which means that the tilt level is not affected by the different etching processes adopted.

## Summary

Synchrotron X-ray topography techniques including SMBXT and SXRCT are adopted to characterize the microstructure of GaN materials for power electronic applications. Ammonothermal grown substrate is found to have the best quality and most promising in high-end power electronic applications. Epitaxial growth, ion implantation and subsequent annealing do not change the dislocation distribution in the wafer, but lattice damage and strain is induced by ion implantation and removed by both high-pressure annealing and capped annealing as revealed by both SMBXT and SXRCT. Furthermore, different etching techniques including ICP, TBCl, and a combination of ICP and TBCl are compared by SXRCT. It is concluded that ICP etching gives rise to enhanced strain by ion bombardment, while using TBCl does not cause damage to the material and can actually recover some damage from a preceding ICP etching process.

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## References

- [1] R. Dwiliński, et al., *Journal of Crystal Growth* 311 (2009) 3015-3018.
- [2] H.P. Maruska, et al., *Applied Physics Letters* 15 (1969) 327-329.
- [3] T. Nakamura, et al., *GaN substrate technologies for optical devices*, IEEE, vol 101, 2013, p. 2221.
- [4] V. Meyers, et al., *Journal of Applied Physics* 128 (2020) 085701.
- [5] M.H. Breckenridge, et al., *Applied Physics Letters* 118 (2021) 022101.
- [6] J.D. Greenlee, et al., *ECS Journal of Solid State Science and Technology* 4 (2015) P382.
- [7] R. Shul, et al., *Applied physics letters* 69 (1996) 1119-1121.
- [8] B. Li, et al., *Applied Physics Letters* 115 (2019) 162101.
- [9] B. Raghothamachar, et al., in: G. Dhanaraj, K. Byrappa, V. Prasad, M. Dudley (Eds.), *Springer handbook of crystal growth*, Springer, 2010, p. 1425.
- [10] J. Guo, et al., *Journal of Electronic Materials* 47 (2018) 903-909.
- [11] Y. Yao, et al., *Journal of Electronic Materials* 47 (2018) 5007-5012.
- [12] B. Raghothamachar, et al., *Journal of Crystal Growth* 544 (2020) 125709.
- [13] Y. Liu, et al., *Journal of Crystal Growth* 551 (2020) 125903.
- [14] J. Hsu, et al., *Applied Physics Letters* 78 (2001) 1685-1687.
- [15] E. Miller, et al., *Applied physics letters* 84 (2004) 535-537.
- [16] Y. Liu, et al., *MRS Advances* (2021) 1-6.
- [17] Y. Liu, et al., *ECS Transactions* 104 (2021) 113-122.
- [18] K. Horibuchi, et al., *Semiconductor Science and Technology* 31 (2016) 034002.