Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 383-388
doi:10.4028/p-kc5309

Submitted: 2021-12-23
Revised: 2022-03-04
Accepted: 2022-03-10
Online: 2022-05-31

Latest Advances in the Implementation and Characterization of High-K Gate Dielectrics in SiC Power MOSFETs

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Keywords: SiC power MOSFET, high-k gate dielectrics, SiC MOSFET reliability, high temperature gate bias test, threshold voltage stability.

Abstract. Recently high-k gate dielectrics for SiC power MOSFETs attracted increasing research interest thanks to promising results related to improved specific channel resistances and threshold voltage stability. We investigated high-k gate stacks for 1.2kV and 3.3kV SiC power MOSFETs regarding on-state performance and stability during high temperature gate bias tests. Furthermore, we studied the high-k/SiC interface quality and the effect of burn-in pulses using SiC MOSCAPs. High-k SiC power MOSFETs show significant improvement in on-state performance and threshold voltage stability. We found that the burn-in pulses can be shorter for high-k gate dielectrics compared to SiO_2-based devices.

Introduction

Nowadays, power electronics is undergoing an exciting and profound technology shift driven by the steadily growing demand for energy of our digital society and the urgent requirement for low carbon emission transport infrastructures. Si based power electronics reaches its performance limits regarding high energy-efficient power converters for e-mobility and renewable energy applications. SiC MOSFETs have entered the power devices arena and are the frontrunners to replace traditional Si IGBT technology due to their higher breakdown voltage and thermal conductivity. Despite their successful market entry, several challenges that are strongly connected to the state-of-the-art gate stack technology are still to be solved though in order to fully exploit the enormous potential of SiC power MOSFETs. Conventional SiO_2 gate oxides for example suffer from highly defective oxide/SiC interfaces with interface state densities (D_{IT}) of in the order of $\sim 10^{13}$ eV^{-1} cm^{-2} [1-3]. These defect levels are significantly higher than what it is typically found in SiO_2/Si systems ($\sim 10^{10}$ eV^{-1} cm^{-2}) [4]. Thus, the field-effect mobility of SiC MOSFET, which is strongly related to the D_{it}, is limited by the carrier trapping effect of the interface states, even after nitridation [5]. The origin of such high D_{IT} is not yet fully understood, but there is a general consensus that it might originate from the presence of C in the SiO_2 or at the interface [6]. Additionally, the threshold voltage stability and drift are unsolved problems in SiC MOS technology. We have developed a novel MOS gate stack technology based on high-k dielectrics for power electronic devices between 1.2kV and 3.3kV. The concept of integrating high-k dielectrics in SiC power devices has been investigated since the late 1990s, however, it is only recently that the rather low temperature processes needed for high-k have been successfully combined with the high thermal budgets required for SiC. It is becoming increasingly evident that the predicted device performance gain has not only been experimentally confirmed, but is also featured by other concomitant phenomena, which, for instance, impact on burn-in behavior and other effects caused by defects. In this paper, we review the performance gain and threshold voltage stability in low and medium voltage SiC power MOSFETs, while focusing on the key features of an improved dielectric interface.

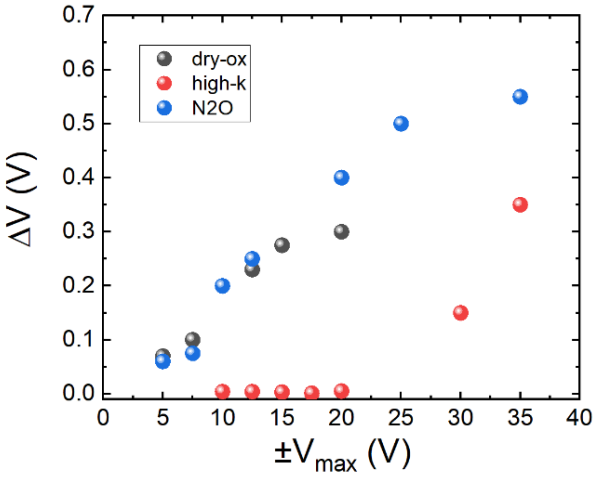

Figure 1: Extracted hysteresis for various sweep amplitudes from +/- 5V to +/- 40V for high-k and SiO_2 dielectrics with and without post oxidation nitridation

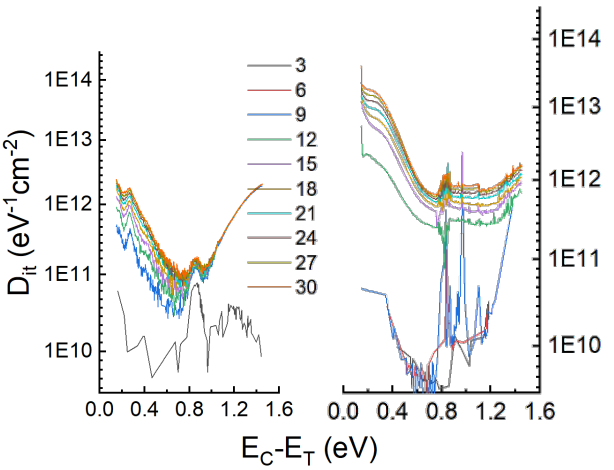

Figure 2: D_{it} extraction from CC-DLTS for various V for high-k (left) and SiO_2 (right) for various pulse voltage from 3V to 30V (inset).

Experimental Details

Thermally oxidized and high-k MOS capacitors were fabricated by thermal oxidation in O_2 ambient and state-of-the-art dielectric deposition technique without oxidizing the underlaying SiC interface, respectively. Electrically characterization by C-V and deep level transient spectroscopy was performed. C-V measurements were performed at RT (1 MHz), whereas deep level transient spectroscopy, in constant capacitance mode (CC-DLTS), was performed in the 77-750 K temperature range. CC-DLTS measurements were carried out at a fixed frequency of 1 MHz, by using a reverse bias (V_R) of -15 V and by keeping a constant pulse height (V_H) value, with a filling pulse of 1 ms. Another set of measurements was done by replacing the electrical pulse with an UV optical pulse of 100 ms (30 mW, 365 nm), e.g. minority carrier transient spectroscopy (MCTS).

The CC-DLTS/MCTS signal was then converted into an energy distribution of the density of interface traps (D_{IT}). This was done assuming that the D_{IT} is weakly dependent of the energy and that the capture cross section does not depend on the temperature and energy [5].

A gate stress bias (burn-in) of 20 V was applied to either thermal oxide and high-k MOS capacitors, at 150, 175 and 200 °C, for different time durations. The flat band voltage (V_{FB}) was extracted from the C-V measurements, by using the second derivative of the relation between the capacitance C and the gate voltage V_G [7].

Finally, we fabricated planar high-k SiC power MOSFETs for repetitive switching experiments to investigate the threshold voltage stability under harsh dynamic conditions. These devices were soldered on copper substrates, wire bonded and measured in a double pulse tester with a stray inductance of 60nH.

Results and Discussion

Figure 1 shows the static gate voltage hysteresis comparing both dielectric layers, also indicating the effect of N_2O annealing on the SiO_2/SiC interface. Apparently, the N_2O process does not improve the hysteresis effect of the device. The high-k, however, shows no hysteresis up to 20V that underlines the improved threshold stability still representing one of the greatest challenges for SiC devices and applications. Figure 2 indicates the comparison of the extracted density of interface states (D_{it}) using CC-DLTS of high-k (left) and SiO_2 (right) gate stacks. Here, voltage pulses at different start voltages (3-30V) for the CV characteristics of the MOS capacitor samples were studied. Higher trap densities

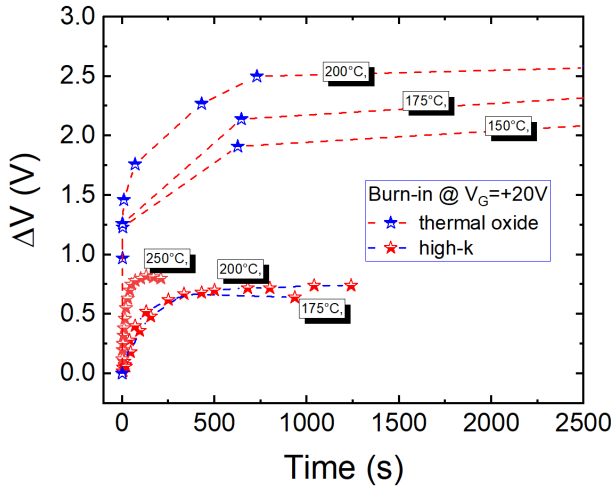

Figure 3: Burn-in over time for different temperatures comparing high-k and SiO_2 gate dielectrics.

are associated to larger voltage sweeps in both cases. However, the trap density for the high-k gate stacks is more than one order of lower compared to the SiO_2-based stack. Notably, the pulse voltage dependence drops significantly towards mid gap. We also investigated whether the improved high-k/SiC interface quality does also affect the burn-in behavior.

Figure 3 shows the flat band voltage shift (ΔV) as function of the burn-in time at various temperatures. The voltage shift saturates at approx. +2.5V for all temperatures for the SiO_2 stack. This saturation level is reached faster, i.e. at shorter burn-in times, with increasing temperature. Similar behavior was observed for the high-k dielectric, although the saturation voltage is lower.

Figure 4 and 5 display the interface density extracted using CC-DLTS and MCTS for a wide range of the bandgap. We examined as deposited devices and samples after burn-in pulses at 200°C, for thermal oxide and high-k dielectrics. As it can be seen, the D_{IT} close to the conduction band is considerably higher for the thermal oxide compared to the high-k dielectric. This might be due to the fact that in the thermal oxide MOS capacitor, the presence of defects in the SiO_2 that give rise to a D_{IT} distribution close to the conduction band [8] has to be taken into consideration. Close to midgap the two dielectrics show a broad D_{IT} distribution. Despite the superior high-k/SiC interface quality, this peak was not influenced by the choice of dielectric and its corresponding process. Thus, we assume that the defect traps are in the SiC epi layer rather than at the interface. After the burn-in stress, it can be noted that the D_{IT} close to the conduction band was not affected (Figure 4 and 5). On

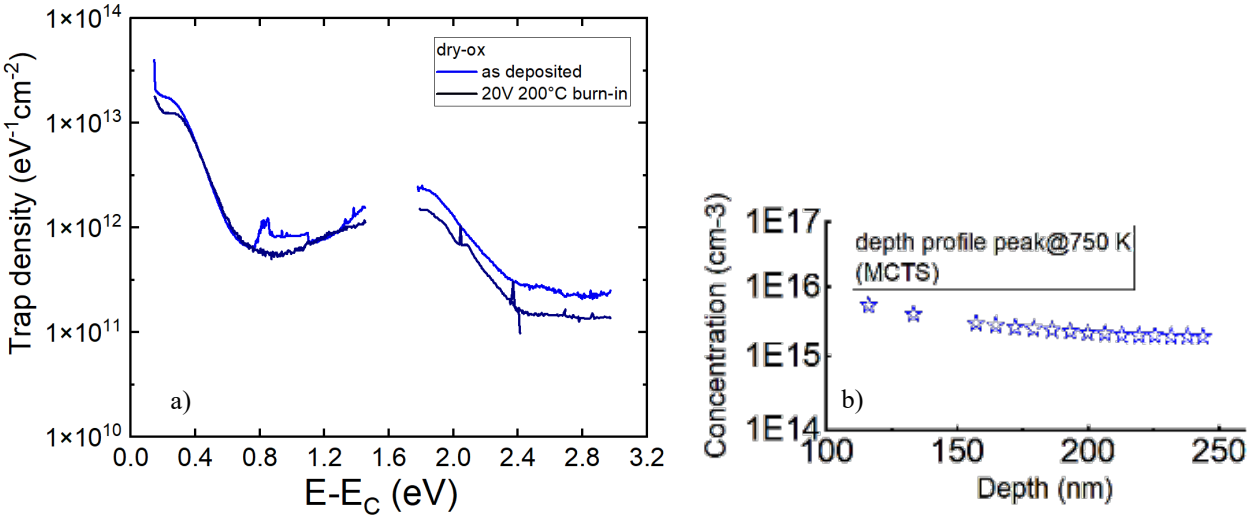

Figure 4: a) D_{it} extraction using CC-DLTS and MCTS over the full bandgap for as deposited and burned-in thermal oxide, for a V_H=30V. b) Depth profile of the CC-MCTS signal taken at 750 K, corresponding to the D_{IT} distribution at $E-E_C$ ~1.9 eV.

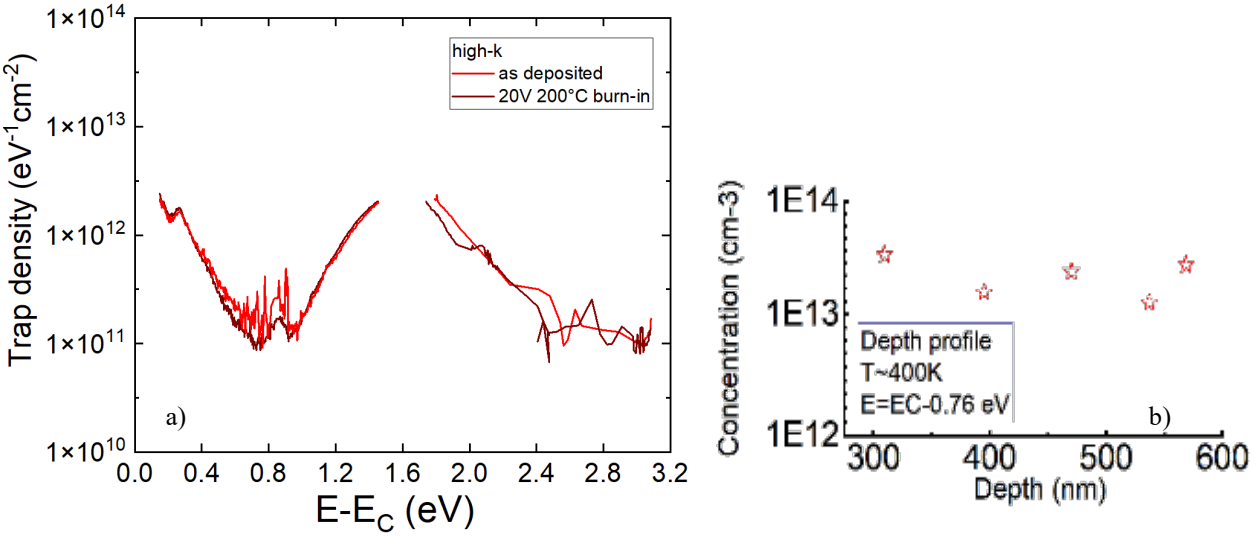

Figure 5: a) D_{it} extraction using CC-DLTS and MCTS over the full bandgap for as deposited and burned-in high-k dielectrics, for a V_H=30V. b) Depth profile of the CC-DLTS peak at $E\text{-}E_C$~0.8 eV.

the other hand, we observe a slight decrease in D_{IT} for the thermal oxide samples. The burn-in pulses do not show any effect on the D_{IT} for the high-k samples.

In the following we will provide a short discussion about the microscopic origin of such mid-gap defect distribution. First, it should be noted, that no final conclusions can be drawn based on the presented results and that further investigations are needed. Nonetheless, some hypotheses can be put forward to explain such broad distributions. In their study, Kobayashi et al.[9] have analyzed different defects, e.g., carbon dimers in the SiO_2, at the interface and in SiC, in a SiO_2/SiC system, by means of density functional theory. Among the investigated defects, the most promising might be the dicarbon antisite ($(C_2)_{Si}$), located in the SiC crystal giving rise to several electrical active levels in the band gap. As a matter of fact, $(C_2)_{Si}$ is responsible for two very close electrically active levels at midgap, at E_C-1.6 eV and E_C-1.7 eV [9]. Since DLTS is generally not suitable for separating two (or more) similar emission rates, it can be suggested that such broad D_{IT} might originate from these two closely spaced levels. Possibly, a Laplace DLTS investigation might be useful to separate both contributions.

In the insets of Figure 4 and 5, we report the extracted depth profiles of the CC-DLTS signals at ~750K (thermal oxide) and ~400K (high-k). The depth distribution of both signals is located at least within the first hundreds of nanometers of the epitaxial layer, meaning that the defects responsible

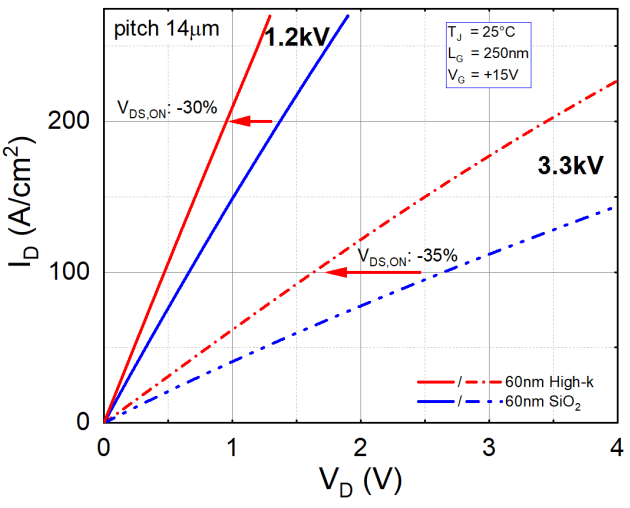

Figure 6: Static on-state comparison of 1.2kV and 3.3kV SiC MOSFETs with high-k and SiO_2 dielectric.

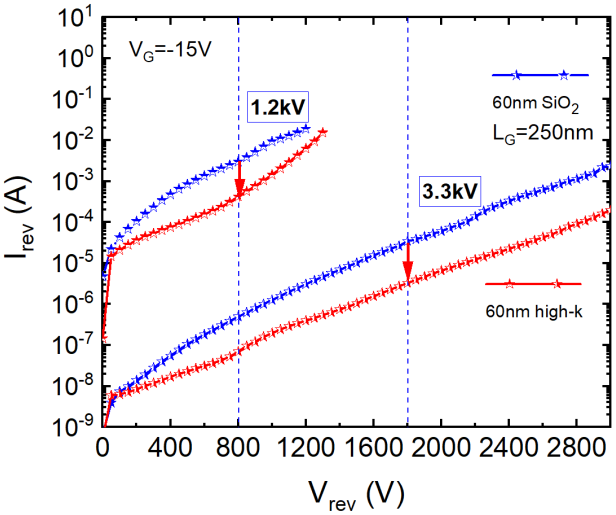

Figure 7: Static blocking comparison of 1.2kV and 3.3kV SiC MOSFETs with high-k and SiO_2. dielectric.

for this D_{IT} are rather close to the surface. The concentration, however, is in the range of the drift doping. Thus, it must be assumed that a change due to burn in, as we have seen, has a significant effect on the threshold and flatband voltage of the device.

Figure 6 shows the static on-state characteristics of 3.3kV and 1.2kV SiC power MOSFETs with high-k and standard silicon dioxide gate stacks and pitches of 14um. The channel length amounts to 250nm. While the high-k gate stack was deposited by a state-of-the-art deposition technique commonly used for example in CMOS technology, the silicon dioxide was formed by high temperature thermal oxidation of a deposited CVD layer and a high temperature post oxidation nitridation (PON) in N_2O ambient. As can be seen in the graph, both voltage classes gain significantly in performance. Although the performance of higher voltage devices depends substantially on the epi

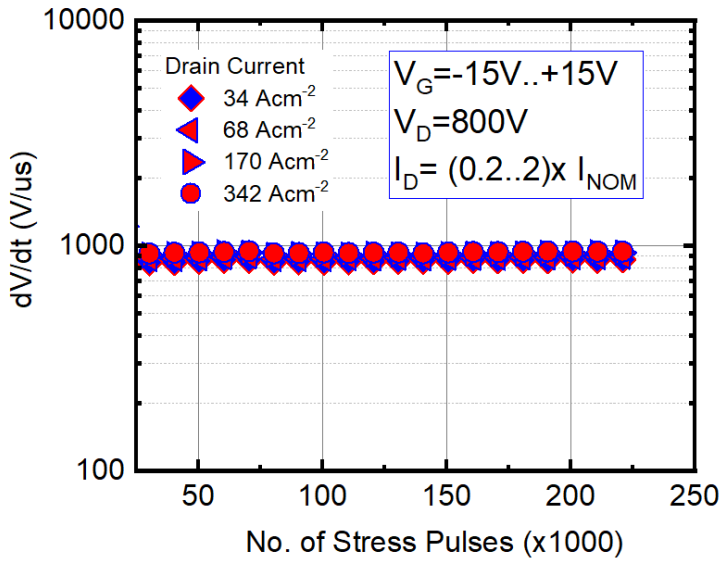

Figure 8: Extracted dV/dt from repetitive dynamic turn-on waves of high-k MOSFET switching V_{DS}=800V and I_D=2xI_{NOM} and V_{GS}=-15V to +15V at 150°C.

resistance, the implementation of high-k leads to a reduction of the on-state by more than 35%. Figure 7 shows the blocking characteristics of the same representative devices from Figure 6. In both voltage classes the high-k dielectric efficiently reduces the reverse leakage by approx. one order of magnitude. Apparently, the channel suffers from drain induced barrier lowering effects which can be suppressed by the larger permittivity and thus electric field in the SiC. Moreover, the V_{th} stability extracted from dynamic characterization is depicted in in Fig. 8. The extracted dV/dt of the turn-on

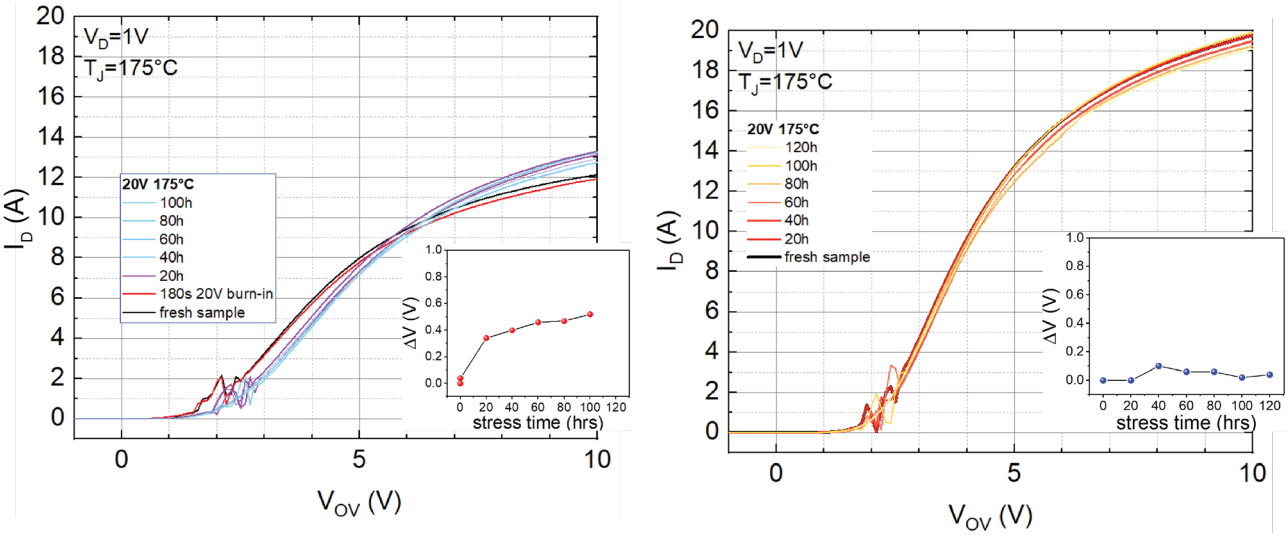

Figure 9: Transfer curves of 1.2kV SiC power MOSFETs with (left) SiO_2-based and (right) high-k gate stacks after each 20 hours HTGB stress cycle. The insets show the extracted threshold voltage drift as function of stress time.

wave forms up to 200k stress cycles at 2x I_{NOM} using a wide gate voltage swing of V_{GS}= +/- 15V does not show any signs of degradation. Finally, we performed high temperature gate bias (HTGB) tests on 1.2kV SiC power MOSFETs with high-k and SiO_2-based gate stacks. The devices were tested for 100-120 hours at 175°C using a gate voltage of V_{GS} = 20V. After each 20 hours gate voltage stress phase we measured the transfer curves, as can be seen in Figure 9, and extracted the threshold voltage drift (c.f. insets of Figure 9). The threshold voltage drift of the high-k devices is considerably lower, i.e. below 100mV, compared to the SiO_2-based devices. For the latter we observed a maximum threshold voltage drift of 500mV after an accumulated HTGB stress of 100 hours.

Summary

In this paper we presented the latest advances of our high-k gate stack technology for vertical SiC power MOSFETs including a thorough study of the SiC/dielectric interface quality using CV, DLTS and MCTS measurements. Additionally, we studied the effect of burn-in voltage pulse on the flatband voltage stability of high-k SiC MOSCAPs. We found that the flatband voltage saturates at lower burn-in times for increasing temperature. This saturation is reached even earlier for the high-k gate stacks. 1.2kV and 3.3kV SiC power MOSFETs show a significantly improved on-state performance compared to SiO_2-based control devices and indicate a lower threshold voltage drift. Furthermore, it was demonstrated that the influence of the stress voltage results in a change of the defect concentration.

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