

## Fast Defect Mapping at the SiO<sub>2</sub>/SiC Interface Using Confocal Photoluminescence

Judith Woerle<sup>1,a\*</sup>, Brett C. Johnson<sup>2,b</sup>, Roger Stark<sup>1,c</sup>, Massimo Camarda<sup>3,d</sup>  
and Ulrike Grossner<sup>1,e</sup>

<sup>1</sup>Advanced Power Semiconductor Laboratory, ETH Zurich, Physikstrasse 3, 8092 Zurich, Switzerland

<sup>2</sup>School of Physics, University of Melbourne, Victoria 3010, Australia

<sup>3</sup>Paul Scherrer Institute, Forschungsstrasse 111, 5232 Villigen, Switzerland

\*a<sup>woerle@aps.ee.ethz.ch</sup>, b<sup>brett.johnson2@rmit.edu.au</sup>, c<sup>stark@aps.ee.ethz.ch</sup>,  
d<sup>massimo.camarda@psi.ch</sup>, e<sup>ulrike.grossner@ethz.ch</sup>

**Keywords:** interface defect density, photoluminescence, capacitance-voltage

**Abstract.** Electrically active defects at the SiO<sub>2</sub>/SiC interface can have detrimental effects on the device performance of SiC MOSFETs. Capacitance- or conductance-based analysis techniques are commonly used to extract the density of interface defects, despite having the disadvantage of requiring dedicated test structures for the analysis. Here, we discuss confocal sub-bandgap photoluminescence (PL) microscopy as a fast and reliable alternative to conventional electrical characterization techniques. For this purpose, the quality of the SiO<sub>2</sub>/SiC interface after post-oxidation annealing in N<sub>2</sub>O is studied both by confocal imaging as well as by the high-low and C-Ψ capacitance technique. We find excellent agreement between the optical and electrical analysis and observe a significant increase of the interface defect density for annealing temperatures below 1050 °C.

### Introduction

For the fabrication of commercially viable SiC metal-oxide-semiconductor field-effect transistors (MOSFETs), the growth of a high-quality gate oxide layer in combination with an abrupt silicon dioxide (SiO<sub>2</sub>)/SiC interface and a low density of defects is vital. Although conventional dry or wet oxidation techniques - similar to what is used for Si - can be used to grow SiO<sub>2</sub> insulation layers on SiC, the termination of the SiC surface has proven insufficient using these processes alone as they lead to a high density of both interface defects ( $D_{it}$ ) and near-interface oxide traps. This has been linked to very low channel mobilities and thus high channel resistances in SiC MOSFETs [1].

For the characterization of interface and bulk properties of a dielectric layer on a semiconductor, capacitance-voltage (CV) and conductance-voltage (GV) measurements on MOS capacitors are routinely used. One major advantage of these well-established techniques is their selective sensitivity to electrically active defects, facilitating a correlation of measurement results with the device performance of the final MOSFET. However, the inherently wide bandgap of SiC causes a broad variation of interface trap response times, setting strict limits to the energy window that can be investigated at room temperature [2]. In addition, much higher frequencies are required for a correct evaluation of the  $D_{it}$  close to the conduction band compared to, e.g., silicon devices [3]. Another disadvantage of CV and GV techniques is that they require dedicated test structures, which can be cumbersome during process development or for process monitoring purposes. Recently, confocal photoluminescence (PL) microscopy was shown to present an attractive alternative for a non-destructive characterization of the SiO<sub>2</sub>/SiC interface [4], allowing for a quick estimation of the interface defect density between individual fabrication steps.

In order to improve the low channel mobility in SiC MOSFETs, a variety of oxidation and post-oxidation annealing (POA) treatments have been suggested [5,6], among which nitridation was shown to be particularly promising [7-10]. Both direct growth as well as post-oxidation annealing (POA) in NO or N<sub>2</sub>O ambients have been intensively studied and are now commonly used for the fabrication

of commercial power MOSFETs [6]. During nitridation, nitrogen accumulates at the SiO<sub>2</sub>/SiC interface and although the detailed mechanisms are still not fully understood, there seem to be similarities with Si, where a passivation of the interface defect states via Si-N bonds is responsible for the observed improvement [11].

In particular, NO was shown to be very effective in improving the channel mobility for all crystal faces [1,10,12], although its high toxicity sets clear constraints to a widespread implementation. N<sub>2</sub>O is less of a safety concern but in order to prove beneficial, careful optimization of the nitridation temperature is required as high temperatures are necessary for N<sub>2</sub>O to dissociate into NO, O<sub>2</sub> and N<sub>2</sub> which then lead to a simultaneous nitration and oxidation [9,13,14].

The upper temperature limit for nitridation in N<sub>2</sub>O is set around 1300 °C where NO dissociates into N<sub>2</sub> and O<sub>2</sub> [15]. The low-temperature limit, on the other hand, is less clearly defined and experimental reports on the beneficial effect of N<sub>2</sub>O treatments to efficiently passivate interface defects range from 900 °C to 1150 °C [9,16,17]. A clear understanding of the low-temperature nitridation regime, however, may be essential for applications where very thin oxides are required or where the thermal budget of the samples is limited. Furthermore, a large number of academic and industrial research facilities are restricted both in oxidation temperatures as well as in the choice of processing gases, emphasizing the need for a dedicated low-temperature study.

Hence, the aim of this work is to explore the effects of POA processes in N<sub>2</sub>O on the quality of the SiO<sub>2</sub>/SiC interface in the temperature range between 750 °C and 1050 °C. The interface defect density is extracted both by conventional capacitance-voltage techniques (i.e. the high-low and C-Ψ method) as well as sub-bandgap confocal photoluminescence (PL) spectroscopy and results are discussed in light of temperature-dependent N<sub>2</sub>O dissociation processes.

## Method

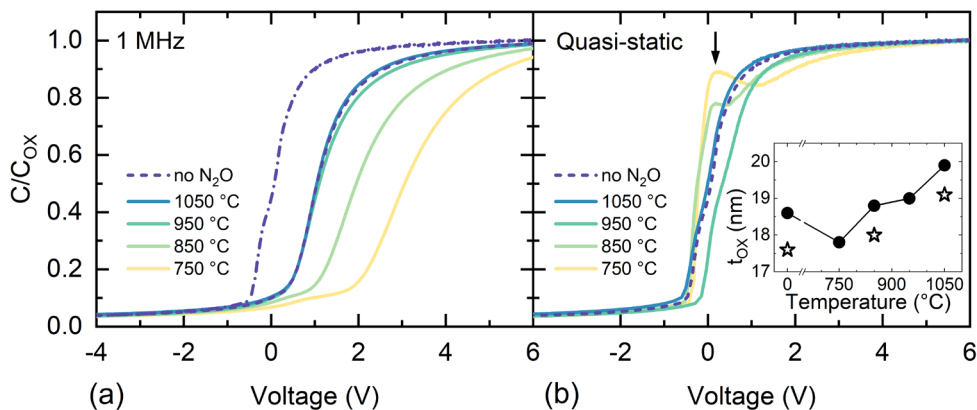
Samples cut from Wolfspeed 4H-SiC wafers with a 4° off-axis orientation and an epi-layer doping concentration of  $N_D = 4 \times 10^{15} \text{ cm}^{-3}$  were used in this study. All samples were wet-chemically cleaned and an oxidation was performed for 11 h at 1050 °C in an O<sub>2</sub> atmosphere, resulting in an oxide thickness ( $t_{\text{ox}}$ ) of 18.5 nm. Post-oxidation annealing in N<sub>2</sub>O was carried out in the same oxidation furnace for 3 h at temperatures ranging from 750 °C to 1050 °C. After the nitridation, aluminum was deposited on the front side to define contacts with a radius of 300 μm. Finally, the oxide on the backside was removed and 100 nm Ni was deposited for the Ohmic back contact.

High-frequency (HF) and quasi-static (QS) CV measurements were performed on a wafer probe station with a Keithley 4200A-SCS parameter analyzer. For the high-frequency measurements, an AC frequency of 1 MHz and an AC amplitude of 25 mV were used. Quasi-static CV curves were obtained by measuring the displacement current in response to a slowly varying DC gate voltage. The ramp rate was fixed to 0.1 V s<sup>-1</sup>. For each nitridation process, several MOS capacitors were analyzed and a negligible variability between different devices was found. All CV measurements presented here were performed at room temperature. In addition to the capacitance measurements, the oxide thickness of three of the samples were also measured by X-ray reflectometry (XRR) using a Bruker D8 micro-source X-ray diffractometer.

The confocal PL setup used in this study consisted of a 532 nm continuous wave Nd:YAG laser, a dichroic mirror, a high numerical aperture (0.95) 100x air objective, a 560 nm long pass filter and a fiber-coupled single photon counting module. The theoretical diffraction-limited spatial resolution was 280 nm for emission wavelengths of 600 nm. The samples were mounted onto a piezoelectric XYZ scanning stage allowing for scan sizes of up to 100 μm × 100 μm. All confocal images presented here were collected at room temperature. More details on the setup and the PL analysis are given in Ref. [4].

## Results & Discussion

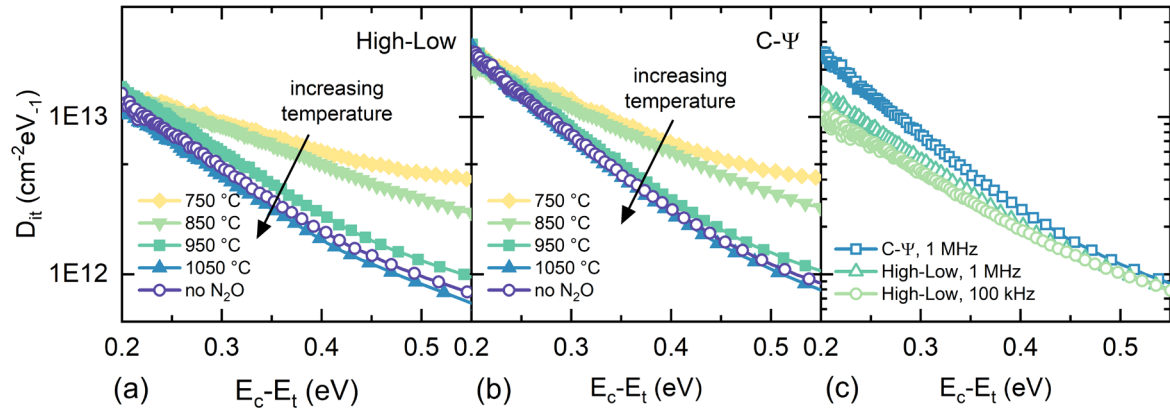
For the electrical extraction of the  $D_{it}$ , quasi-static and HF capacitance-voltage measurements were performed and results are presented in Fig. 1. The high-frequency CV curves in Fig. 1a show an increasing stretch-out of the capacitance for decreasing annealing temperatures as expected for increasingly large interface defect densities. For the two lowest annealing temperatures, a small bump is observed in depletion, which is even more pronounced for the quasi-static measurements in Fig. 1b (indicated by the arrow). From the oxide capacitance, the oxide thickness was then extracted and results are presented in the inset of Fig. 1b. With increasing temperature, more and more  $O_2$  from the  $N_2O$  dissociation is available, giving rise to additional oxide growth and hence to an increase of the overall oxide thickness to 20 nm. The sample annealed at 750 °C, on the other hand, showed a slightly reduced  $SiO_2$  thickness which might be connected to the very large defect density and hence a larger error of the electrically determined oxide thickness.



**Figure 1.** Normalized capacitance-voltage curves for different  $N_2O$  annealing temperatures. (a) High-frequency measurements at 1 MHz. The quasi-static curve for the non-annealed sample is also shown (dash-dotted line). (b) Quasi-static CV curves. The inset shows the oxide thickness as function of the  $N_2O$  annealing temperature as extracted from CV (filled symbols) and XRR (open symbols) measurements. Additional oxide growth is only observed for temperatures  $> 950$  °C.

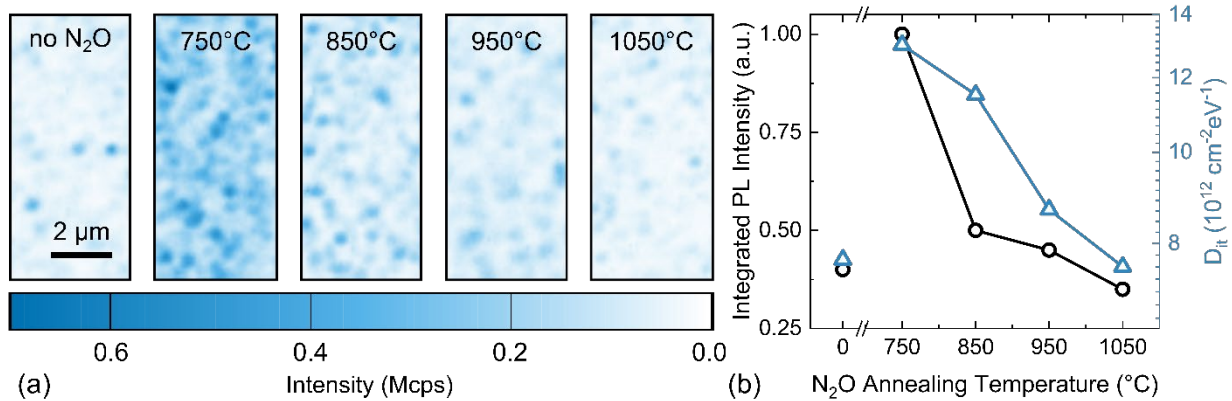
Also indicated in the inset of Fig. 1b are the results of thickness measurements using X-ray reflectometry (XRR) performed on three of the five samples, which show a similar trend as the electrical analysis. Similar to earlier reports [18], the systematic overestimation of  $t_{ox}$  from the CV data may be explained by a smaller relative permittivity for thermal oxides grown on SiC compared to Si, i.e.  $\epsilon_{SiO_2} \approx 3.7$  instead of  $\epsilon_{SiO_2} = 3.9$ . A variation of the oxide density for different annealing temperatures was not observed during the XRR measurements.

Using both the C- $\Psi$  [3] and high-low [19] CV method, the interface trap density  $D_{it}$  was extracted. A comparison of the two methods is presented in Fig. 2. As previously reported, the high-low method is not sensitive to very fast states, which still respond to the probing frequency of 1 MHz, hence leading to an underestimation of the interface defect density close to the conduction band [3]. Apart from the absolute offset between the two methods, a very similar trend is observed for the  $N_2O$ -annealed samples shown in Fig. 2: a strong increase in  $D_{it}$  is detected for the samples annealed at 750 °C, indicating a deterioration of the interface caused by the POA in  $N_2O$  as also observed previously [11,20]. With increasing temperature, the  $D_{it}$  decreases again and only for the samples annealed at 1050 °C, a small but consistent improvement to the non-annealed samples is observed.



**Figure 2.** Density of interface defects as a function of the trap energy position. (a) Trap distribution extracted from the CV measurements in Fig. 1 using the high-low method. (b) Trap distribution according to the C-Ψ method. (c) Comparison of the high-low and C-Ψ method for the non-annealed sample.

In addition to the electrical characterization of the defect states generated during the low-temperature nitridation, confocal PL microscopy was deployed for optical analysis. While this technique is already extensively used for the analysis of bulk defects using above band-gap light excitation [21,22], it is gaining increasing attention as defect mapping tool for the  $\text{SiO}_2/\text{SiC}$  interface [4,23,24].



**Figure 3.** (a) Confocal PL maps of thermally oxidized 4H-SiC. (b) Comparison of the emission center intensity median (*left*) and the  $D_{it}$  as extracted by the C-Ψ method (*right*) as a function of the annealing temperature. Presented  $D_{it}$  values refer to a bandgap energy of  $E_c - E_t = 0.35\text{ eV}$ .

Figure 3a shows confocal PL maps of the nitrided samples after excitation with a sub-bandgap 532 nm laser. Diffraction-limited spots can be observed which are associated with single defects residing at or near the  $\text{SiC}/\text{SiO}_2$  interface. In accordance with the electrical analysis, the integrated intensity of these single defects is observed to decrease as the  $\text{N}_2\text{O}$  annealing temperature increases while the density of defects remains around  $1\text{ }\mu\text{m}^{-2}$  (equivalent to  $10^8\text{ cm}^{-2}$ ) in each map. These values are much lower than the defect densities discussed above since only a small energy window is probed with the sub-bandgap energy laser. The decrease in intensity is assumed to be due to modification of the radiative recombination rate due to the presence of nitrogen at the interface [4]. An increased number of defect centers is also observed in vicinity to crystal defects or surface damage (e.g., scratches) of the epitaxial layer. After removal of the  $\text{SiO}_2$  layer from the samples, the PL intensity and hence defect density is significantly decreased. The corresponding room-temperature ensemble PL spectra for the studied samples exhibit a large spectral variability, leading to a broad PL peak centered at 750 nm (not shown here).

A direct comparison of the two analysis methods is shown in Fig. 3b where both the integrated PL intensity of the presented confocal PL maps and the electrically extracted  $D_{it}$  as a function of the  $N_2O$  annealing temperature are presented. Very good agreement between the two analysis methods is found. With both methods, a small improvement of the interface quality compared to the non-annealed sample could be observed for the highest annealing temperature. A further decrease of the  $D_{it}$  is expected as the annealing temperature is further increased [13,17].

In order to explain the observed degradation of the interface at low annealing temperatures, it is valuable to consider the nitridation process in more detail: for efficient nitridation of the interface, the dissociation of  $N_2O$  into  $NO$ ,  $N_2$  and  $O_2$  is essential, which only occurs at temperatures well above 1000 °C. This is also apparent in our measurements where a reduction of  $D_{it}$  is only detected at an annealing temperature of 1050 °C. The significant increase of interface defects at lower temperatures is less intuitive, especially when considering that the diffusion of  $N_2O$  in  $SiO_2$  should be very slow due to their large molecular size [13]. However, several studies confirm this observation: slow-trap profiling of  $N_2O$ -annealed SiC revealed increased densities of slow interface traps, (whereas  $NO$  annealing led to a significant decrease of the slow traps) and in experiments with diluted  $N_2O$  an improvement was only achieved when the carbon removal rate from the interface exceeded the carbon accumulation rate [7-9,25]. The strong increase in  $D_{it}$  observed in the CV and PL measurements may be an indication for a hampered out-diffusion of carbon away from the interface and emphasizes the need for careful optimization of the  $N_2O$  annealing process.

## Conclusion

In this work, a comparison between capacitance-voltage methods and sub-bandgap confocal photoluminescence microscopy for the characterization of oxidation-induced defects at the  $SiO_2/SiC$  interface was presented. The samples, annealed in  $N_2O$  at different temperatures, exhibited an increasing density of interface defects for decreasing annealing temperatures. At an annealing temperature around 1050 °C, the nitridation had beneficial effects on the  $D_{it}$ . Although confocal PL does not allow for a quantitative analysis, already small variations of the defect density at the  $SiO_2/SiC$  interface are detectable and a similar trend for increasing annealing temperatures is clearly observed. This study emphasizes the great potential of confocal PL as a quick and reliable characterization method for a variety of oxide/semiconductor systems without the need of fabricating a full device. Although this work has been performed on smaller sample sizes, an extension of confocal PL to full-wafer mapping is feasible. As the measurement does not require surface contacts, very thin oxides (a few monolayers) can also be accurately measured. Furthermore, measurements can be performed directly on the oxidized wafer and at room temperature, making it an attractive tool for a quick and reliable interface analysis during device fabrication.

## Acknowledgments

Laura Maurel is gratefully acknowledged for performing the XRR measurements. This work was supported by the Australian Research Council Centre of Excellence for Quantum Computation and Communication Technology (No. CE110001027).

## References

- [1] T. Kimoto and J. A. Cooper, Fundamentals of Silicon Carbide Technology. Wiley (2014).
- [2] J. A. Cooper, Phys. Status Solidi A 162, 305 (1997).
- [3] H. Yoshioka, T. Nakamura, and T. Kimoto, J. Appl. Phys. 111, 014502 (2012).
- [4] B. C. Johnson et al., Phys. Rev. Applied 12, 044024 (2019).
- [5] G. Liu, B. R. Tuttle, and S. Dhar, Appl. Phys. Rev. 2, 021307 (2015).
- [6] M. Cabello et al., Mater. Sci. Semicond. Process. 78, 22 (2018).
- [7] S. Dimitrijević et al., IEEE Electron Device Lett. 18, 175 (1999).
- [8] H.-F. Li et al., Appl. Phys. Lett. 70, 2028 (1997).

- 
- [9] P. Jamet and S. Dimitrijević, Appl. Phys. Lett. 79, 323 (2001).
  - [10] G. Y. Chung et al., Appl. Phys. Lett. 76, 1713 (2000).
  - [11] S. Dimitrijević et al., Properties of Nitrided Oxides on SiC, Springer Berlin Heidelberg (2004).
  - [12] Y. Nanen et al., IEEE Trans. Electron Devices 60, 1260 (2013).
  - [13] T. Kimoto et al., Jpn. J. Appl. Phys. 44, 1213 (2005).
  - [14] V. V. Afanas'ev et al., Appl. Phys. Lett. 82, 568 (2003).
  - [15] T. Suzuki et al., Mater. Sci. Forum 615-617, 557 (2009).
  - [16] L. A. Lipkin, M. K. Das, and J. W. Palmour, Mater. Sci. Forum 389-393, 985 (2002).
  - [17] K. Fujihira et al., Solid State Electron. 49, 896 (2005).
  - [18] T. Hosoi et al., Mater. Sci. Forum 740-742, 605 (2013).
  - [19] D. K. Schroder. Semiconductor Material and Device Characterization. John Wiley & Sons, (2005).
  - [20] R. C. De Meo et al., J. Electrochem. Soc. 141, 150 (1994).
  - [21] G. Feng, J. Suda, and T. Kimoto, Appl. Phys. Lett. 92, 221906 (2008).
  - [22] J. Camassel and S. Juillaguet, Phys. Status Solidi B 245, 1337 (2008).
  - [23] A. Lohrmann et al., Appl. Phys. Lett. 108, 021107 (2016).
  - [24] J. Woerle et al., Phys. Rev. Materials 3, 084602 (2019).
  - [25] K. Y. Cheong et al., J. Appl. Phys. 93, 5682 (2003).