

Electrical Scanning Probe Microscopy Investigation of Schottky and Metal-Oxide Junctions on Hetero-Epitaxial 3C-SiC on Silicon

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Abstract. This paper presents a macro- and nanoscale electrical investigation of Schottky and metal-oxide junctions with hetero-epitaxial 3C-SiC layers grown on Si. Statistical current-density-voltage (J-V) characterization of Pt/3C-SiC Schottky diodes showed an increase of the reverse leakage current with increasing the devices diameters. Furthermore, C-V and J-V analyses of SiO₂/3C-SiC capacitors revealed non-idealities of the thermal oxide, such as a high trapped positive charge ($3 \times 10^{12} \text{ cm}^{-2}$) and a reduced breakdown field ($E_{BD}=6.5 \text{ MV/cm}$) compared to ideal SiO₂. Nanoscale electrical characterizations by conductive atomic force microscopy (CAFM) and scanning capacitance microscopy (SCM) allowed to shed light on the origin of non-ideal behavior of Schottky and thermal oxide junctions, by correlating the morphological features associated to 3C-SiC crystalline defects with local current transport and carrier density.

Introduction

The cubic polytype of silicon carbide (3C-SiC) has been studied since a long time, as it could give some advantages with respect to 4H-SiC in MOSFET devices, i.e. a high inversion channel mobility [1,2]. Hence, it is considered a good candidate for power electronics applications in the voltage range 600-900V [3]. However, the large density of defects in hetero-epitaxial 3C-SiC on Si currently limits the performances of both Schottky and MOS devices based on this material. In particular, the impact of stacking faults (SF) and anti-phase-boundaries (APBs) on the reverse leakage current and on the forward turn-on voltage of Schottky diodes is debated [4,5]. Furthermore, the origin of the extrinsic mechanisms responsible for the observed degradation and premature breakdown of 3C-SiC MOS capacitors [6] is still unclear. Considering the detrimental effect of crystalline defect (such as the threading dislocation) in 4H-SiC MOSFETs reliability under high temperature reverse bias stress[7], it is mandatory to fully investigate the role of crystalline defects in 3C-SiC MOS-based structures to address the real intrinsic reliability for future power electronics application.

In this paper, Schottky contacts and thermal oxide (SiO₂) insulators on hetero-epitaxial 3C-SiC/Si layers have been investigated by means of nanoscale electrical characterizations [8,9], i.e. conductive atomic force microscopy (CAFM) and scanning capacitance microscopy (SCM), with the aim to correlate the morphological features associated to 3C-SiC crystalline defects with local current transport and carrier density.

Experimental

Unintentionally doped 10.2 μm thick 3C-SiC layers were grown on on-axis Si(100) substrates by chemical vapor deposition (CVD) using silane (SiH_4) and propane (C_3H_8) as silicon and carbon precursors [10]. After the growth, a chemical mechanical polishing of the surface was carried out to reduce the roughness.

On a first sample, Pt Schottky diodes were fabricated by formation of a Ni_2Si Ohmic front contact (by Ni lift-off and thermal annealing at 950 $^\circ\text{C}$), followed by lift-off of circular Pt contacts with different radius (from 5 to 25 μm) [8]. On a second 3C-SiC sample, a ~ 40 nm thermal oxide (SiO_2) was grown at 1150 $^\circ\text{C}$, 1 hour, in dry O_2 . Lateral metal–oxide semiconductor (MOS) capacitors were obtained by lift-off of Ni/Au metal electrodes, consisting of a circular inner gate (radius 50 μm), surrounded by a large-area electrode. Electrical characterization (I-V and/or C-V) of the Schottky diodes and MOS capacitors were carried out in a CASCADE Microtech probe station, using a Keysight B1505A parameter analyzer. Nanoscale electrical characterizations, namely Conductive Atomic Force Microscopy (CAFM) and Scanning Capacitance Microscopy (SCM), have been performed using a DI3100 system by Bruker with a Nanoscope V controller, using conductive (Pt or diamond coated) tips. Current maps were acquired on the bare 3C-SiC surface and after the growth of a thin (~ 10 nm) thermal oxide, properly chosen to apply an electric field up to 10 MV/cm with the tip using the maximum bias (10 V) allowed by our CAFM setup. Furthermore, the same CAFM tip was used to contact the Pt diodes with different areas and perform current–voltage measurements.

Results and Discussion

Fig. 1(a) and (b) show two sets of J-V curves collected on arrays of Pt/3C-SiC Schottky diodes with 5 and 25 μm radius. Noteworthy, the curves collected on the larger diodes showed a significantly higher leakage current density at negative bias, with a larger spread between different devices. Fig.1(c) shows the “yield” of working devices, defined as the percentage of analyzed diodes with a leakage below a threshold current density of 10 $\mu\text{A}/\text{cm}^2$. The red line is the fit of the data with the function reported in the insert of Fig.1(c), commonly employed to describe the yield of electronic devices, where A is the contact area and D is the areal density of defects responsible for devices failure [4]. The evaluated density ($D=2\times 10^5 \text{ cm}^{-2}$) from the fit can be associated with the extended defects responsible for a leakage current exceeding the fixed threshold. This areal density corresponds to a typical average distance $L=D^{-1/2}\approx 20 \mu\text{m}$ between the defects.

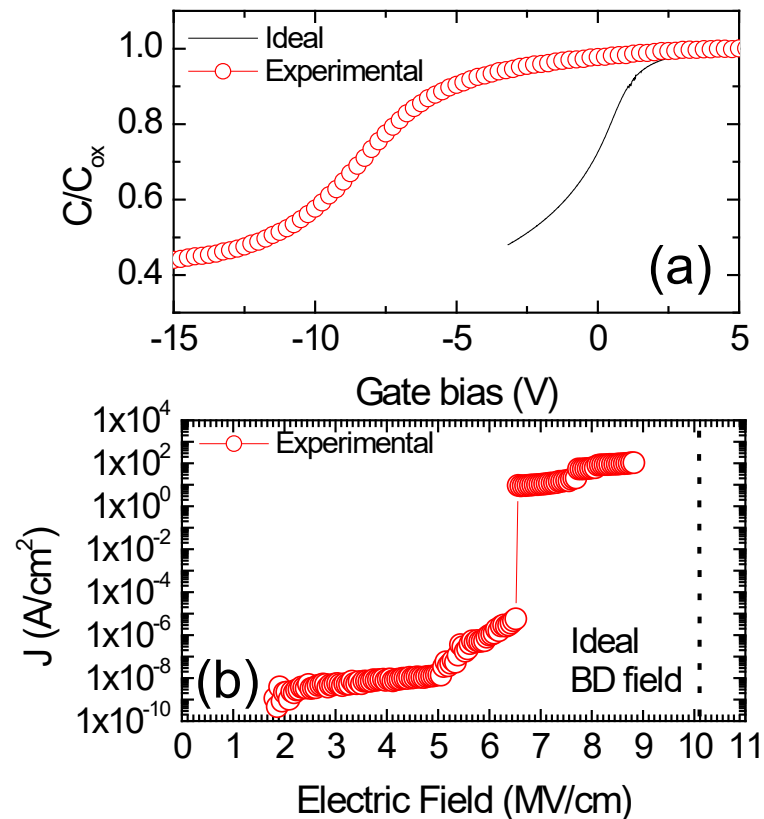


Fig.2 (a) C-V curve measured at 1 kHz on a 3C-SiC MOS capacitor compared with the calculated curve; (b) Current density vs voltage (J-V) curve of a 3C-SiC MOS capacitor. The value of the ideal SiO₂ breakdown electric field is indicated by the dashed line.

In the following, the nanoscale electrical characterization of the bare 3C-SiC surface and after the growth of a thin (~ 10 nm) thermal oxide are reported. The CAFM metal tip (working as local Schottky contact) was preliminarily employed to probe the conduction on the 3C-SiC bare surface, as illustrated in Fig. 3(a). Fig. 3(b) and (c) show the surface morphology and the current map, collected simultaneously with a tip bias $V_{tip}=0.5$ V. Under this forward polarization, preferential conductive paths are visible on the 3C-SiC bare material, such as the anti-phase boundaries (APBs), indicated as dotted curved lines, and stacking faults (SFs), indicated as straight dashed lines [8]. Furthermore, current maps collected at negative tip bias (not shown) revealed that APBs are the main conductive defects under reverse polarization. Interestingly, their distance ($10\text{--}20\ \mu\text{m}$) is similar to the average value obtained from statistical analysis of macroscopic diodes.

Fig. 3(d) shows a schematic illustration of the CAFM setup on the SiO₂/3C-SiC system [9]. The morphology of the as-grown oxide (Fig. 3(e)) resembles the one of the bare 3C-SiC material, i.e., characterized by terraces separated by darker lines associated with the APBs. The SiO₂ surface roughness (RMS) was in the order of 5 nm, a value comparable to those measured directly on 3C-SiC layer before oxidation, demonstrating the conformal growth of the oxide onto the substrate, confirmed also by cross-section TEM analyses [9].

Fig. 3(f) reports the simultaneously collected current map by the positively biased conductive tip with $V_{tip}=8$ V. It can be considered as a breakdown map of an array of nano-MOS capacitors simultaneously stressed at 8 MV/cm. The BD events are not randomly distributed but there are some regions with a larger density, located in correspondence with some APBs. Noteworthy, the SFs were not visible in the case of 3C-SiC covered by thermal SiO₂. The SCM experimental setup is illustrated in Fig. 3(g), whereas Fig. 3(h) and (i) show two representative images of the SCM signal amplitude $|\Delta C|$ and of the phase signal. In particular, both straight line features resembling SFs (dashed lines) and curved line features resembling APBs can be distinguished in the SCM amplitude image in Fig. 3(h), whereas only APBs features can be observed in the phase map in Fig. 3(i). The spatial variations in the SCM amplitude are related to local changes in the carrier density in the 3C-SiC layer.

Interestingly, Fig. 3(i) shows a strong change of the SCM phase signal from 180° on APBs to -180° on the surrounding regions indicating a local increase of the minority carriers (holes) concentration in the 3C-SiC material. Thus, the APBs may act also as a preferential sites for positive charges trapping. On the other hand, the presence of positively charged APBs can cause an enhanced electron injection from the semiconductor into the insulator and the preferential dielectric breakdown close to these extended defects. This can explain the reduced E_{BD} observed in large area MOS capacitors.

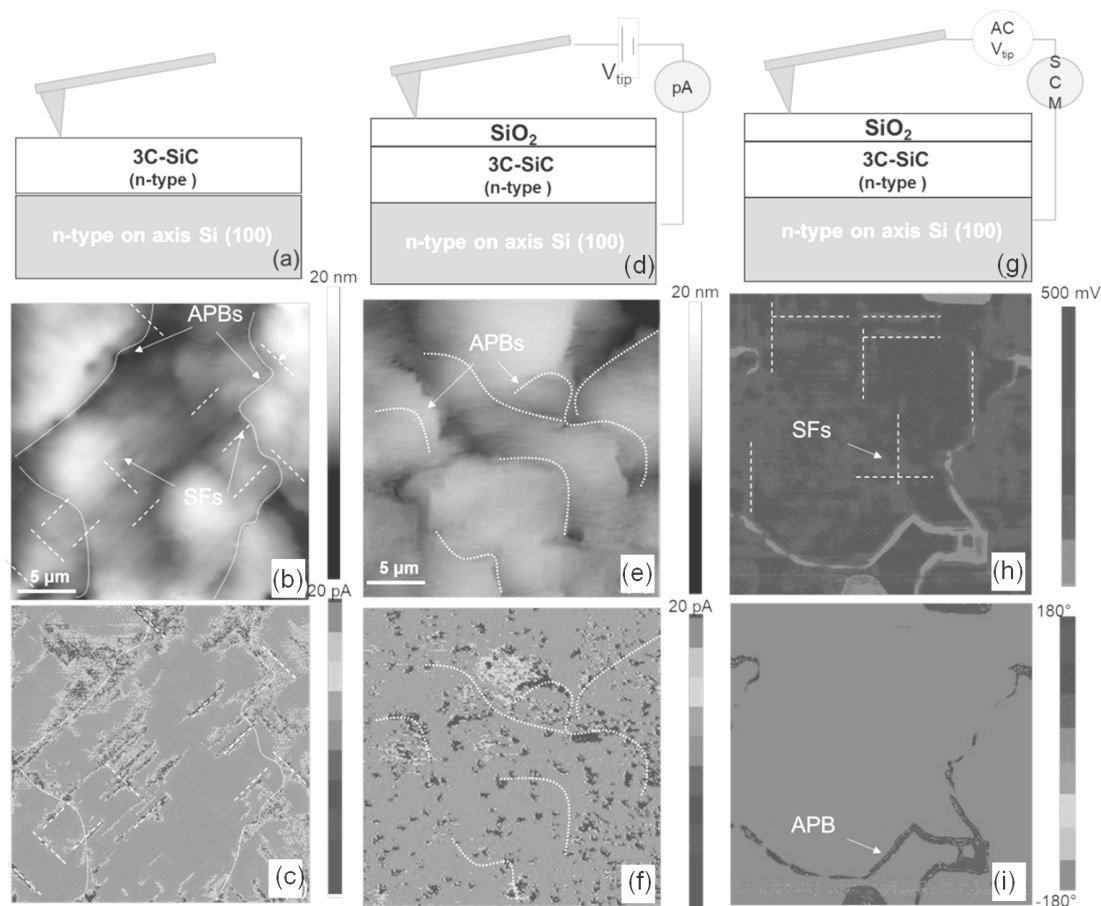


Fig.3 (a) C-AFM setup for current mapping of 3C-SiC/Si, (b) surface morphology and (c) current map. (d) CAFM setup for current mapping of SiO₂/3C-SiC, (e) surface morphology and (f) current map. (g) SCM setup for surface carrier profiling of SiO₂/3C-SiC, maps of SCM amplitude (h) and phase (i) signal.

Conclusion

Electrical characterization of Schottky and thermal-oxide junctions with 3C-SiC showed non-idealities in the device behavior, e.g. high reverse leakage current in Schottky diodes and premature dielectric breakdown of MOS capacitors. Nanoscale electrical characterizations by CAFM and SCM allowed to shed light on the microscopic origin of these phenomena, by correlating the morphological features associated to 3C-SiC crystalline defects with local current transport and carrier density.

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