

A Deeper Look into the Effects of Extended Defects in SiC Epitaxial Layers on Device Performance and Reliability

Hrishikesh Das^{1,a*}, Swapna Sunkari^{1,b}, Joshua Justice^{1,c}
and Danielle Hamann^{1,d}

¹ON Semiconductor, South Portland, Maine, USA

^ahrishikesh.das@onsemi.com, ^bswapna.sunkari@onsemi.com, ^cjoshua.justice@onsemi.com,
^ddanielle.hamann@onsemi.com

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Abstract. The detection and classification of SiC Epitaxial extended defects was refined to separate out defective areas that influence device characteristics. Die level defect localization along with defect area calculations were performed on millions of die across product groups. A clear impact of non-killer defects was observed, especially with increasing density and defective area in the die. Specifically, all types of stacking faults caused higher leakage, lower blocking voltage, and increases in ON resistance and threshold leakage. Furthermore, MOSFET devices were affected to a much larger extent than diode devices. Testing die with higher numbers of defects provides insight on device reliability. Analyzing devices with specific counts of BPDs let us quantify the amount of bipolar degradation caused drift by product/voltage classes.

Introduction

Silicon Carbide is gaining rapid traction in the power electronics space. The highest volume drivers require high power density and efficiency, while maintaining ever increasing requirements on reliability, robustness, and stability over the system life. Concurrently, SiC substrates used to build these devices have over $1 \times 10^4 \text{ cm}^{-2}$ crystal defects even in good production-quality wafers. These substrate crystal defects further nucleate extended defects and crystal defects in the epitaxial layers. Squaring the requirements of reliability with the reality of the material quality, requires a very deep understanding of the SiC material and the fabrication process, as well as the influence these aspects have on the electrical performance including lifetime, stability, or drift. It is no longer sufficient to analyze defects and metrics on a wafer level [1,2]. Attributes need to be analyzed on the die level, with sufficiently large volumes, to remove process variations. This work presents a framework to determine relevant attributes of die and assess the impact of various defects on electrical performance. This is done on a massive level of tens of millions of die to remove variations coming from the various processes steps.

Experimental

N-type epitaxial layers with a doping range between $1 \times 10^{16} \text{ cm}^{-3}$ and $1 \times 10^{18} \text{ cm}^{-3}$ were grown on 4° off-cut 4H-SiC 150 mm substrates in a warm-wall multi-wafer CVD reactor. The epitaxial layers were characterized by a confocal microscope, the Lasertec SICA88, using a 313 nm excitation lamp. Defects were detected and classified using machine learning algorithms with surface topographic channels along with photoluminescence (PL) channels in the near infrared (700 nm+). With the ability to now detect and classify the numerous non-killer crystal defects (NKDs) in SiC epitaxial layers with greater than 95%-99% purity, each defect can be traced to the corresponding fabricated die. Purity here is defined by the accuracy of the automatic defect classification and is determined by review. Each defect category was further split into defect areas that caused an effect on the devices and areas that do not cause any influence, iteratively. Additionally, the affected defective area caused by each defect was calculated for each die. These enhanced attributes were localized and aligned to the

affected die and such statistics were collected on 3 million die for each product (Diodes and MOSFETs). The effect of these attributes on electrical properties and reliability were analyzed.

Results

In our previous work [3], we explored statistically the consequence of defect presence in a die; the results on killer defects were very clear. The defect classified as killer defects had kill-rates of ~90% or more, as expected. In contrast, NKDs, including V-type defects/Partials and Stacking faults, had a minimal increase in the base kill-rate. Furthermore, an improved localization was developed, where the “dangerous” areas of each defect were identified. As a result, both the count of such defects and the corresponding defective area in each die were determined as shown in Fig. 1. ONSEMI’s advanced manufacturing infra-structure seamlessly integrates datasets collected at crystal growth, epitaxy, and device fabrication as well as electrical test results from front-end and back-end stages. In addition, all information related to individual defects like classification, size, contrast, and exact coordinate are collected and stored. This eventually enables the analysis of devices with exact knowledge about type, location, and quantity of specific NKDs. In addition, due to run rates of MOSFETs and Diodes in mass production, large statistical quantities of >3 million devices were analyzed, which provides excellent signal to noise ratio.

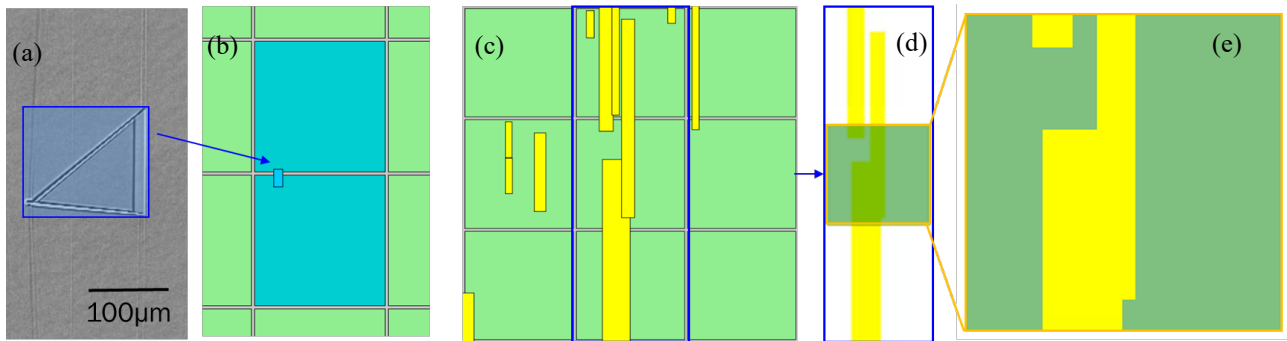


Figure 1. Shows the defect identification and then localization within a device die. Fig. 1a shows the identification of the relevant areas of a defect and Fig. 1b shows the localization/alignment of the defect on product die. Fig. 1c-1e shows how actual defective area is calculated when there are multiple and overlapping defects.

Fig. 2 shows the relationship between the kill-rate of the die (i.e. percentage of the die failing with the trend shown as a dashed line) and the number of the defects localized in that die. The secondary axis shows the absolute quantity of die that have those number of defects. The number of affected die decrease by orders of magnitude as the defect densities increase. Diodes and MOSFETs show vastly different sensitivity to NKDs, with MOSFETs being more susceptible to higher densities of Stacking faults. The kill-rate climbs slightly for the diodes to ~20%, while for the MOSFETs this rises to 90%+. This is attributed to additional yield failure modes like channel leakage. The combination of the distribution density and the effect on the die explains the relatively benign influence these defects have at low quantities but become harmful or “killer” at higher densities. The concept of a die failing depends on a variety of other factors, like process variations of the epi and fabrication and how close to the test specifications the die falls. The true gauge of the effect of the defects is the shift in the parametric test values.

Fig. 3 demonstrates the effect of the density of one NKD type, pure Stacking Faults, has on the electrical leakage and blocking characteristics of both diodes and MOSFETs. These stacking faults are classified as having no surface signatures or features. While the diodes are affected, the impact on the MOSFETs is more severe. There are also more modes of failure in MOSFETs [4]. While killer defects typically lead to hard shorts or excess forward or reverse leakage currents, devices which are affected by multiple NKD demonstrate wider parametric distributions of critical device parameters like breakdown voltages (BVD_{ss}), forward voltage (V_F) or threshold voltage (V_{TH}).

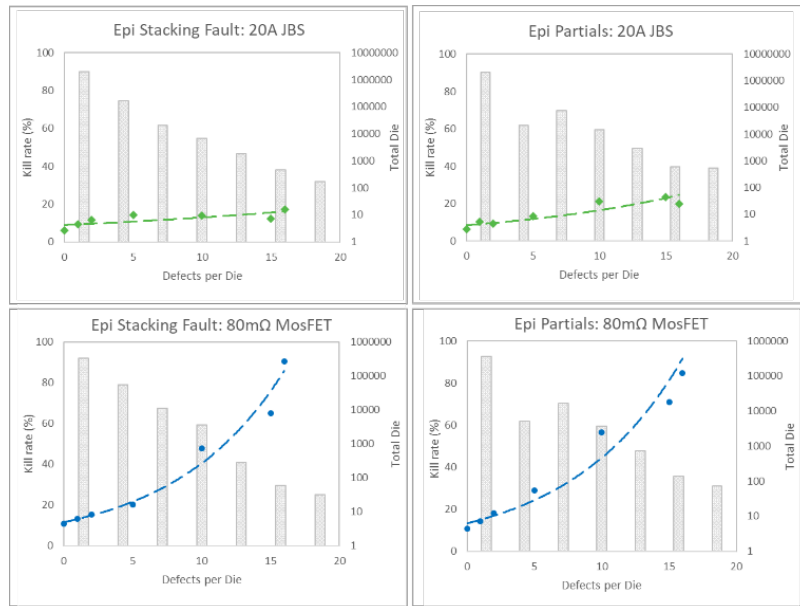


Figure 2. Shows the effect of different densities of non-killer defects on 3 million each of 1200V Diode and MOSFET die. The MOSFETs are much more sensitive and the kill-rate approaches 90%+ at higher densities.

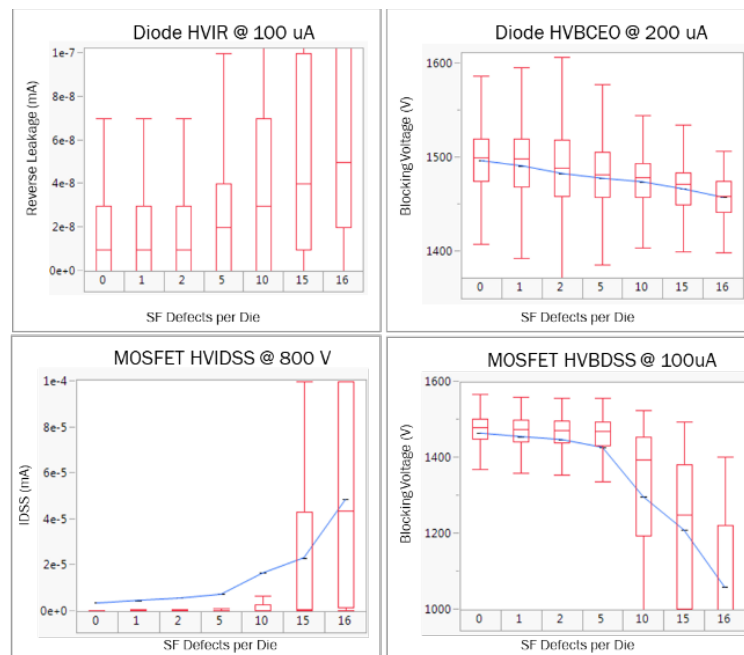


Figure 3. Shows the degradation of performance as the number of SF per die increase. This eventually causes the die to fail the test limits. The x-axis denotes the bin grouping by defect count.

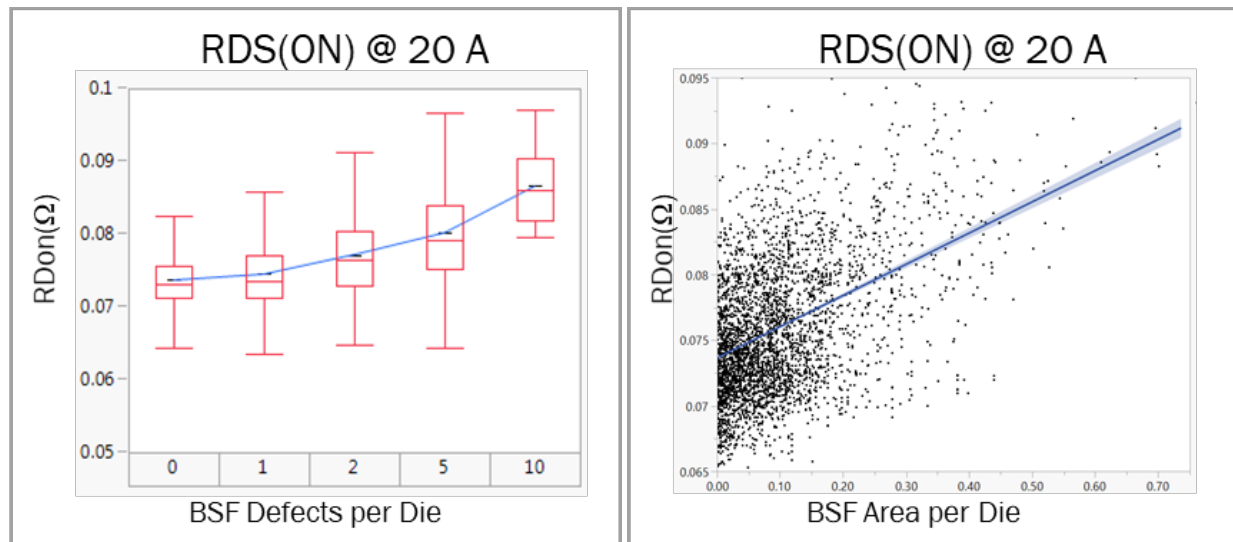


Figure 4. Shows the sensitivity of $R_{DS(on)}$ on the presence of BSF density in MOSFETs. The actual BSF defective area per die is also calculated and this shows a stronger trend on $R_{DS(on)}$. This effect is not seen in Diodes.

Most extended defects nucleated in the epi are of similar size given the same thickness of the layer. As a result, the defect count can be a good proxy for the defective area. However, for some propagated defects like Bar Stacking Faults (BSF), the actual defect area in the die reflects the reality more accurately. Fig. 4 shows how the on-state resistance of a MOSFET ($R_{DS(on)}$) is affected by the presence of BSFs. It is important to also note that the scatter and variations around the secular trends are due to local variations in epi doping/thickness and lot/wafer fabrication variations. Accounting for those on the die level further tightens up the data.

The ability to selectively identify and pick die is very useful for testing the influence of defects on reliability. BPDs have triggered bipolar degradation in SiC MOSFETs, which is well documented in the literature [6,7]. Applying our targeted defect localization approach on epi wafers grown with high BPDs, chips were separated by the number of BPD's per chip among 1200V and 1700V rated devices with comparable die size. Body diode stress was applied in DC-mode with $60\text{A}/\text{cm}^2$ over multiple days. While threshold voltage remained stable throughout the stress, $R_{DS(on)}$ increases, depending on the number of BPD's and the drift layer thickness. This effect is more prominent for 1700V devices. The graphical result is shown in Fig. 5. Further details and results are to be published in [5].

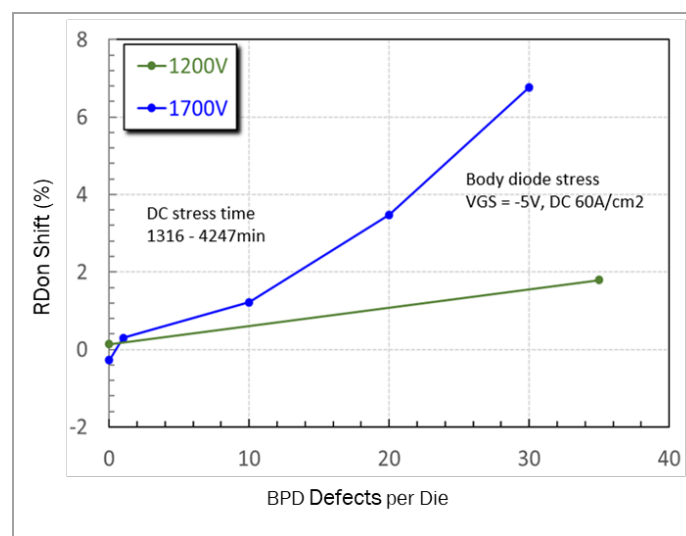


Figure 5. $R_{DS(on)}$ shift in percentage after body diode stress for MOSFETs in dependence of voltage class and BPDs per die. Bias and stress conditions are provided. Stress time varies depending on the time needed for $R_{DS(on)}$ drift to saturate. Similar trend is seen in Pulsed stress tests.

Summary

In summary, this work demonstrates the accurate identification of defective areas of extended defects in SiC epitaxial layers and their alignment and localization to product die. This enables very powerful techniques to gauge the effect of defective area density on device performance and reliability. This allows a deeper assessment of the impact the crystal and extended defects have on the devices as well as quantifies the impact of higher NKD density per die. This also provides for targeting of specific die for reliability to quantify potential failure thresholds and amount of parametric drifts.

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